With Great Power Comes Great Responsibility

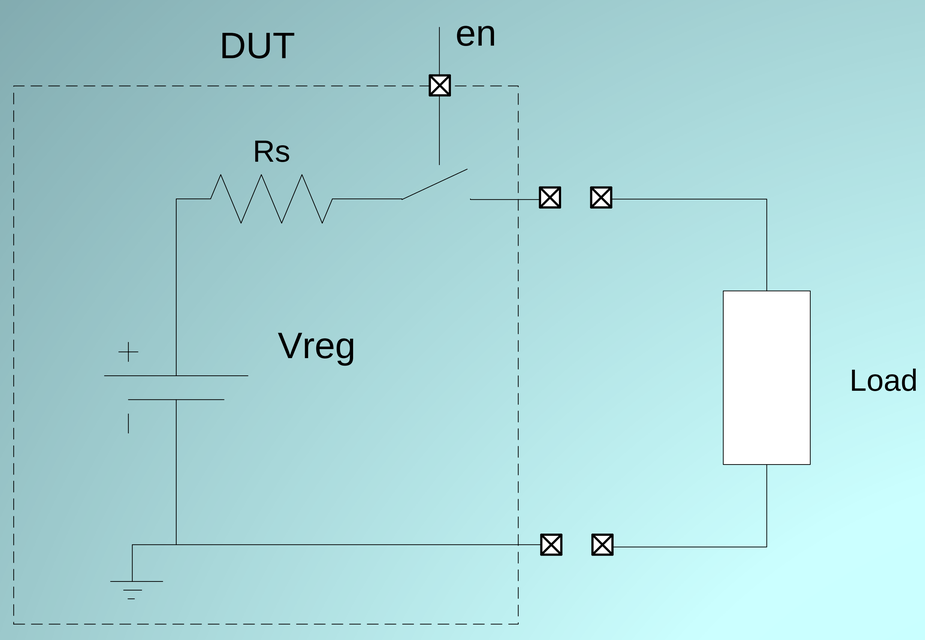
A method to verify PMICs with UVM-MS

Dor Spigel
dspigel@microsemi.com

Moshik Hershcovitch
mhershcovitch@microsemi.com

Introduction

A silicon proven modelling methodology for Mixed Signal powering circuits using UVM.



Voltage regulator simplified example

Main Challenge

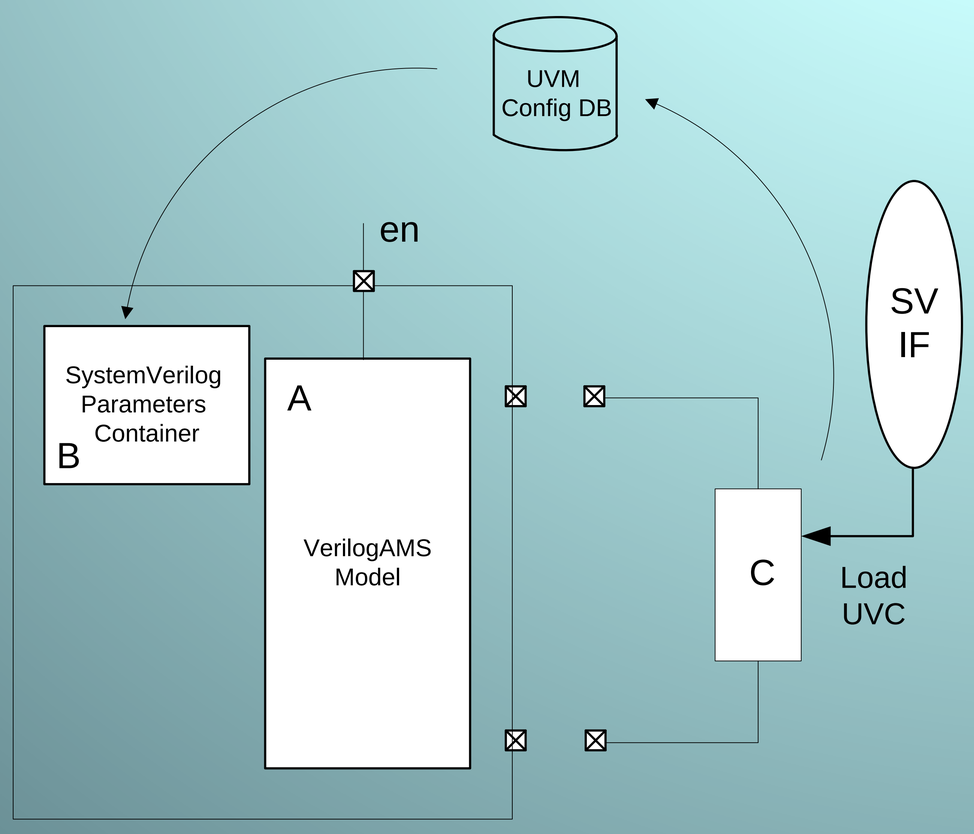
A design block must meet three assumptions so that its I/O's may be represented with event driven real numbers:

- The concept behind the electrical signal can be described as data flow between components.
- The output impedance should be zero and accordingly the input impedance should be infinite.
- The transfer function must be known explicitly.

The first and second criteria cannot be applied because most of the simulations are meant to test how the power supplier deals with overloads and under-loads.

Proposed Solution

Solving the non ideal impedance relations between different components is done by applying the use of the UVM configuration database. This allows the drivers to get load information from an external test component in a way that is reusable and scalable.



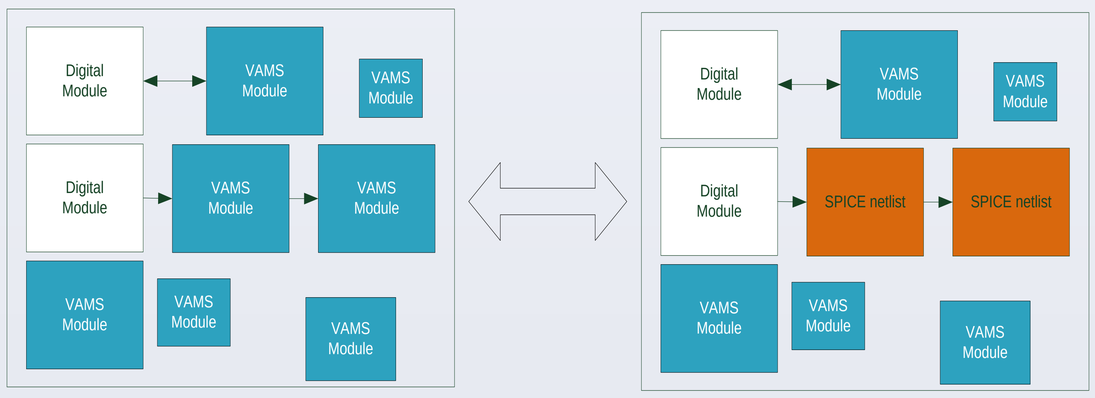
Voltage regulator model block architecture using 'Real Number Models'

Benefits

- Reduced Re-Spins.
- Simulates any load behavior.
- Easier AMS scenario generation.
- Integrates with UVM.
- Better Coverage.
- Silicon Proven.

Up to 100,000 Times Faster!

- Checking analog design blocks from a system perspective by using a combination of models and schematics.

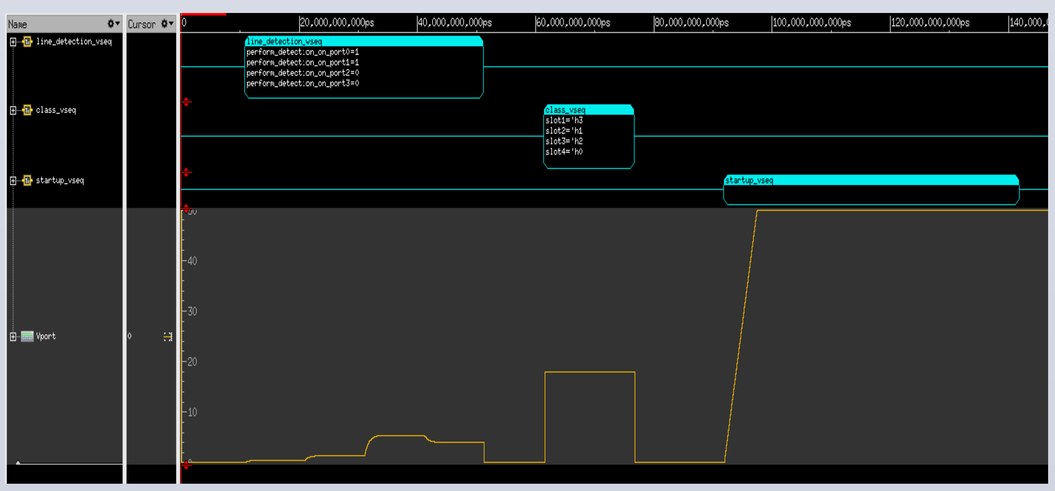


Benchmark

Actual Schematics in the DUT*	Runtime
Full Chip	1.5 weeks
Fully Modeled Design with 3 Cells as schematic	24 hours
Fully Modeled Design with 1 Cell (Large) as schematic	5 hours
Fully Modeled Design with 1 Cell (small) as schematic	20 minutes
Fully Modeled	8 seconds

* Results taken from our 6th generation POE chips. Design contains about 15 analog blocks at the top level.

Simulation Results



Simulation results of a real POE controller chip.

Yellow trace is the port voltage during the POE detection phase

Turquoise boxes are UVM sequences