

Wave Digital Filter Modeling for Complex Automotive Sensor Load Case Verification

Andrei-Daniel Basa, Infineon Technologies Romania, Bucharest (Andrei-Daniel.Basa@infineon.com)

Thang Nguyen, Infineon Technologies Austria, Villach (Thang.Nguyen@infineon.com)

Dirk Hammerschmidt, Infineon Technologies Austria, Villach (Dirk. Hammerschmidt@infineon.com)

Abstract—This paper presents a novel modeling approach based on Wave Digital Filter theory. The new approach allows modeling the behavior of R, L, and C element/network in form of digital wave propagation. This significantly reduces the simulation speed while maintaining the simulation accuracy. The approach enables the verification of complex automotive SoC device - with high number analogue hardware interfaces - in its application circuit context at an early stage. Not only chip designer at Tier-2 supplier can verify the chip behavior but also system integrator at Tier-1 can validate different application scenarios of the chip.

Keywords— automotive, PSI5, DSI3, real-number modeling, Wave Digital Filters, event-based simulation

I. MOTIVATION AND PAPER CONTRIBUTION

A. Introduction and Motivation

An effective utilization of modeling and simulation has proven to be one of the key factors that can significantly help designers with nowadays complex mixed-signal design challenges [1]. This is especially true for the development of the new airbag System-on-Chip (SoC) device. Integrating an automotive airbag electronic system into a single System-on-Chip (SoC) controlled by a main micro-controller (uC) makes the airbag SoC chip a very complex device. The functionalities of the chip include supply management unit, satellite sensors (crash, rotational sensor) interfacing, airbag deployment and many more other functionalities.

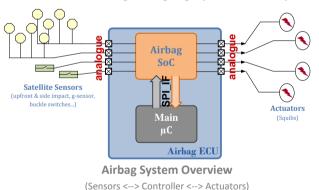


Figure 1: Modern Airbag System from a bird view

In addition to that, the requirement to implement complex signal processing functions and/or sophisticate control-decisional algorithms by digital hardware, together with the high degree of re-usability of digital logic and its capability of scaling down with the technology, led to an increase of the complexity of the digital core logic in SoC systems. Figure 1 illustrates a modern airbag system from a bird view while Figure 2 describes a conceptual block diagram of the airbag sensor interfaces using PSI5 or DSI3 protocol [2],[3]. Physically, these sensors interface with the airbag ECU Electronic Controller Unit with two wires. The first wire is for both power supply to the sensors and for data transmission from the sensors, while the second wire is the connection to ground. Therefore, as illustrated in Figure 2, regulating the bus voltage level is one of the key functionalities of the sensor interface. This is to guarantee a stable power supply to the sensor network. In such system design context, the system stabilization is highly depending on the connected load to the voltage regulator, e.g.: the wiring harness topology, the sensor network, the noise filtering circuits. As shown in Figure 3, combination of different parametric evaluation at the physical layer of a protocol results in a relative high number of verification scenarios.



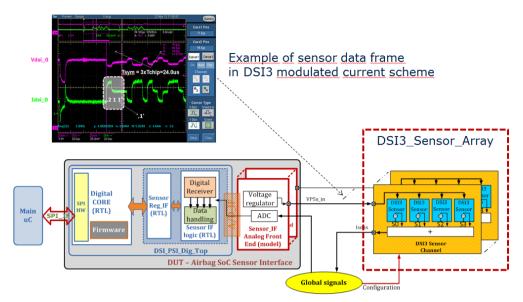


Figure 2: A typical setup for airbag SoC sensor interface functional verification - DSI3 sensor interface

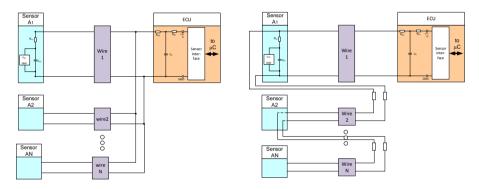


Figure 3: Example of airbag sensor load cases configuration: Parallel vs. Daisy Chain harness topology

Although designers may rely on mixed-signals simulation to perform the last task, debugging of the digital core logic becomes a very complex and time consuming process especially due to the long simulation time required by mixed-signal simulations. With the typical setup shown in Figure 2, a load case mixed-signal simulation would take normally 2-3 days. Therefore,

- a) Event-driven simulation is selected as a strategy for functional verification of the airbag SoC system application.
- b) A modeling approach for event-driven simulation to effectively (simple but accurate and fast simulation speed) model the sensor load cases for the complex airbag SoC system application needs to be researched, developed and implemented.

B. Paper Contribution

In the above described context, this paper proposes a novel modeling approach based on Wave Digital Filter (WDF) theory for the modeling of the connected load of the sensor interface. When using wave propagation concept, the WDF modeling helps not only to simplify the modeling of R,L,C components but also enables digital modeling of these elements for event driven simulator. Thus, it contributes to improve the overall verification effort of mixed-signal modules integrated in airbag SoC. The sensor bus of an airbag SoC system is taken as case study example of mixed-signal for the validation of the WDF modeling concept and implementation. In summary, the main contributions of the paper are as follows:

- The WDF modeling approach is presented, including a short review of WDF theory.
- A full airbag sensor bus model is proposed for the in-application verification of complex modern airbag SoC satellite sensor interfaces.
- Realization of the full airbag sensor bus model based on WDF modeling approach is presented.



This paper is structured as follows: in Section II the automotive airbag sensor interface with PSI5/DSI3 protocol is introduced, the WDF modeling approach and the realization of the bus model is then presented in Section III. Eventually experimental results are presented in Section IV.

II. AUTOMOTIVE AIRBAG SENSOR INTERFACES

A. The Airbag Sensor Interface

Functionally, the airbag sensor interface has the purpose to acquire data reporting the operating condition of the vehicle, data on which the decision for the airbag deployment is taken. As shown in Figure 1 and Figure 2, during operation the sensors, such as accelerometers or pressure sensors, mounted in key locations of the vehicle, continuously measure the positions of impact, the severity of the collision and other variables. This information is provided to the airbag SoC chipset in form of modulated current. The airbag SoC chipset translates the analogue sensor signals into digital words. The translated digital sensor data is reported to the main uC via the SPI (Serial Peripheral Interface) communication. Based on this information the airbag main uC decides *if*, *where* (location) and *when* the airbag (e.g. actuators) is deployed. Failure of the hardware implemented for the reception, decoding and processing of sensor data in the airbag ECU can therefore originate unexpected firing events of the airbag system putting into danger human life.

Both PSI5 and DSI3 are used as protocol for airbag sensor interface. One of the main purposes of these protocols is to define a synchronization scheme between a master (i.e. airbag controller) and multiple slaves (i.e. sensors that are connected to the master via a twisted pair transmission line) for data exchange. The use of a Time Division Multiple Access (TDMA) scheme allows the PSI5 or DSI3 interface to receive data from up to four sensors in all operation modes. Communication between the airbag main micro-controller (master) and peripheral sensors (slaves) occurs by mean of a synchronization signal (Periodic Data Collection Mode-PDCM in DSI3 case or Synchronous mode in PSI5 case) or by mean of a command (Command and Response Mode-CRM in DSI3 case) which defines a common temporal framework between sensors and airbag controller. After detecting a synchronization pulse or the end of the command each sensor transmits data within a well-defined time interval (time slot). Sensor data are transmitted to the airbag controller by modulating the current drawn from the airbag SoC. The modulation is done in respect to a multi-level source coded approach for DIS3 while Manchester modulation scheme is used in PSI5 case. For the paper demonstration purpose, the DSI3, described by the DSI3 consortium in [2], is used as a case study. An example of DSI3 sensor data with three discrete current levels is also illustrated in Figure 2.

B. The Sensor Interface Load Model and its requirement

One of the important requirements in verifying the sensor interface is to evaluate the behavior of the built in transceiver in the airbag SoC under different application and load conditions. As illustrated in Figure 4, primarily, the sensor interface load include the noise filtering circuit, the wiring harness (between the airbag ECU and the sensor network) and the sensor network (the system supports up to 32 different sensors) itself. In particular, PSI5/DSI3 sensors are modeled as an equivalent current source with its output impedance, represented by an equivalent resistance Rs and an equivalent capacitance Cs seen at the sensor input port. The value of the resistance Rs is included to draw the desired DC current and, together with the capacitance Cs, performs a low pass filter action on the current output by current source. The harness is modeled using a T model where the equivalent inductance of the harness (LL), the coupling between the two lines (CL) and the attenuation due to the length of the line (RL) are considered.

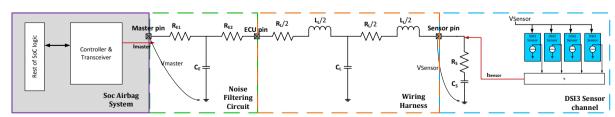


Figure 4: Automotive sensor bus interface model overview

As a result, the regulation behavior of the controller at the pin $Master_pin$ (voltage V_{master}) is carried out by means of the current I_{master} that charges or discharges the equivalent capacitance seen at the pin with the target to keep the voltage V_{master} constant to the desired nominal value. This voltage is propagated to the sensor pin via the harness and constitutes the supply voltage of the peripheral sensors.



III. WDF MODELLING APPROACH & REALIZATION OF THE DSI3 BUS MODEL

A. Load Modeling Approach State-of-the-Art Review

State of the art techniques for modelling of RLC structure networks [4],[5], like in DSI3 case in Figure 4, are considering as reactive elements. This means inductors and capacitors are treated as state variables and the relationships between current flowing through each of the single element as well as voltage originated across the element itself are carried out in the continuous time domain by means of the Laplace transform. Additionally, derivation of the Kirchhoff law for the currents at each node of the load describes how the elements are interconnected together. Mapping from the continuous time domain (S domain) to the discrete time domain (Z-domain) is achieved by means the Euler Backward transformation $s = \frac{1-z^{-1}}{T}$ where T is the sampling frequency used to perform the mapping.

In the case where the system includes multiple dynamic effects that interact with each other like a regulator on the SoC side and the RLC combination on the load side, the state of the art weakness appears. In such situation, the discrete time model requires to break delay loops by introduction of additional delays which of course will cause deviation from the timing behaviour of the real load. The proposed methodology consists in describing the load as a Wave Digital Filter, case when the dynamic behaviour is guaranteed to be fitted as good as possible, providing one-to-one mapping from physical component to the filter state variable.

B. Wave Digital Filters Theory Review

In WDF theory, the so-called wave quantities are used instead of voltages and currents thereby solving the delay free loop issue [6][7]. If v denotes the voltage and i the current at a port, the wave travelling in the forward and backward directions are defined by: a = v + Ri and b = v - Ri where R is a constant value, the so-called port resistance. In order to simulate passive elements using WDF, the port resistance and interconnection between elements has to be derived. In [6], it is described how to derive the WDF elements, this paper describes only the elements which are relevant for the presented implementation. Thus, in Figure 5 capacitors are converted into delay elements, inductors are converted into inverted delays while the resistors are ideal terminations of the lossless transmission line (forward wave is dumped).

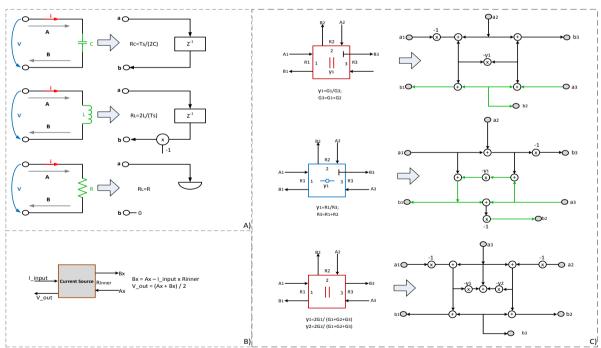


Figure 5: A) Basic WDF elements; B) Current Source with Inner resistance symbol and equations; C) Parallel (matched and not matched) and Series Adaptors symbols and implementation schemes

In order to emulate the interconnections from the reference filters the so-called adaptors have to be introduced. Adaptors define how a forward wave at one port contributes to waves at the other port. These are nport blocks composed of adders and multipliers. An n-port parallel adaptor is used to simulate a parallel connection of n ports, and an n-port series adaptor to simulate a series connection. In Figure 5 a parallel and a series structure is detailed. For ports connecting two adaptors the wave resistance can be matched to one of both to avoid reflections. In Figure 5 it is also described how to convert the input load current (I_{sensor}) into the



correspondent reflected waves and how to compute the voltage based on the incident and forwarded wave respectively.

C. Load Model Realization using WDF Modeling Approach

Using the basic WDF elements and interconnection adaptors, the sensor load network (Figure 6 A) can be converted into the wave flow model depicted in Figure 6 B. Since the SoC master is using in this case a current source (high impedance) to drive the *Master pin* output, the wave digital structure is stimulated with a current source on the left hand side which performs the current to wave conversion and also computes the resulting voltage $V_{out} = \frac{Ax + Bx}{2}$ based on the wave information $Bx = R_{inner} * I_{sensor}$. On the right hand side, the sensor monitors the voltage *Vsensor* and provides the current *Isensor*. Next, all R-L-C and interconnection between elements are replaced with their correspondent wave structure. For example, the series resistor-capacitor (R_s - C_s) in the reference circuit is replaced by the series and parallel adaptors (9) and (10) in Figure 6 B. The wave impedances at ports 1 and 2 for the adaptor 10 are: R1 = Rs, $R2 = \frac{T_s}{2} * Cs$ and the capacitor is replaced by a delay element. The wave flow model has been implemented in VHDL language considering all the WDF parameters as real numbers.

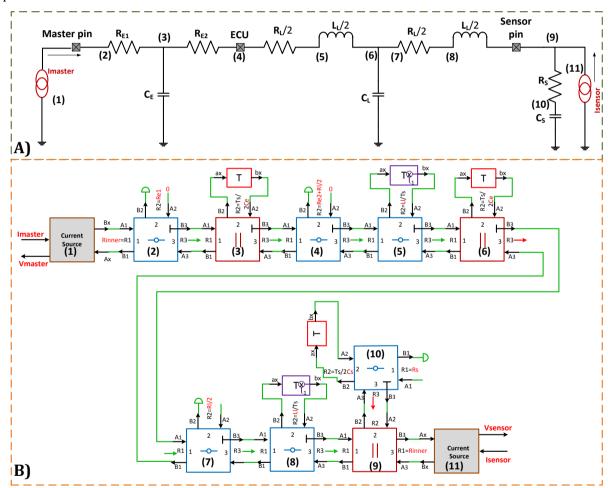


Figure 6: A) Electrical circuit of Sensor bus channel B) Wave digital structure equivalent for the Sensor bus network

IV. VALIDATION OF THE WDF WIRING HARNESS MODEL

A. The validation setup

In context of the airbag DSI3 sensor interface, the WDF harness model was validated: simulation against real lab measurement. As described in Figure 7, the harness model realized in Figure 6, has been used to verify the functionality and stability of the digital core of the airbag SoC system implementing several DSI3 channels, where each channel is connected to a set of DSI3 sensors as described in Figure 4. The test sequence consists in a complete DSI3 communication scenario, including Discovery phase, Command and Response mode and Periodic Data Collection mode respectively. Four sensors are connected to the DSI3 channel having a chip rate frequency for current modulation set to 333 kbps (Tchip=3 µs) while the master command is transferred with a



standard rate of 125 kbps (Tbit=8 μ s). For the simulation results in Figure 8 the following values for the load have been used: RE1 = 8Ω , RE2 = 0Ω , CE = 15nF, RL = 0.5Ω , LL = 731.667nH, CL = 50pF, RS = 2.5Ω , CS = 1nF. The defined harness values are equivalent to 1 meter long cable. The quiescent current per sensor was configured to 10 mA and the response level to 12 mA.

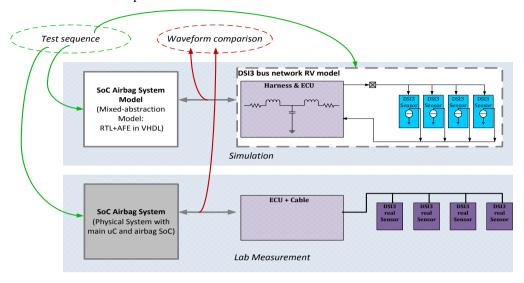


Figure 7: Model performance evaluation set-up

B. Comparision between simulation and real measurement

The DSI3 master pin is evaluated in terms of voltage and current for each mode and a comparison between the real-life measurements and simulation waveforms with the real-value model is given in Figure 8. The CRM mode from master to slave command is highlighted in Figure 8A section, while the Sensor response in B section. The PDCM frame has been configured to 16 bits of payload data and 8 bits of CRC. This can be found in Figure 8C section. In Figure 8 D the Sensor Discovery protocol is highlighted where every sensor signaled its presence in the chain within a defined synchronization timeframe.

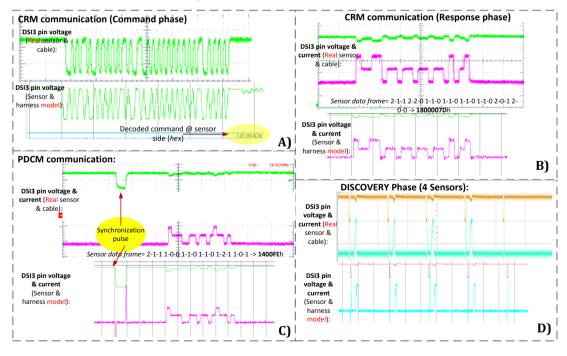


Figure 8: Comparison between real-life measurement and simulation results for the DSI3 Sensor interface

Comparison of the waveform between simulation and measurement shows a very good matching. The comparison was carried out also on the system at different modes. The received digital sensor data frame at the SPI interface was checked against the analogue transmitted sensor data on the wiring harness. This indicates that



the WDF wiring harness model is accurate and fit very well to the overall airbag system model. On the other hand, the full system simulation with the WDF wiring harness is now reduced to a few hours.

Further checkers in terms of sensor signal distortions and slope time effect in current modulated data are performed with respect to different harness length and ECU capacitor. The distortion is caused by the interaction of the line inductance L_L with the sensor equivalent capacitance C_S and the ECU capacitor C_E , resulting in a resonant effect where some of the frequencies of the sensor signal are amplified. Increasing the harness length will make the distortions more obvious as in Figure 9A and Figure 9C. The slope time effect can be seen by varying the ECU capacitor C_E . In Figure 9D, for example, increasing the ECU capacitance C_E will make the signal slower compared to Figure 9B. Running simulations by having the opportunity to configure on the fly these parameters is very important for checking the controller stability and decoder performances over all possible cases.

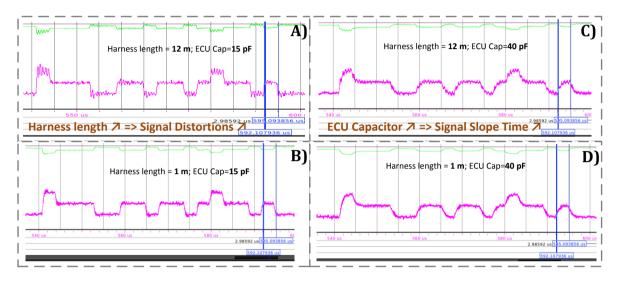


Figure 9: Waveforms showing the voltage and the current at the DSI3 master in different load scenarios

V. CONCLUSION AND OUTLOOK

The WDF modeling approach presented in this paper allows simplifying the modeling of R, L, C components with the wave propagation concept. This result in the fact that the wiring harness and the termination circuits are possible to be digitally modeled, e.g.: VHDL with real modeling. Despite the modeling simplicity, the accuracy is still guaranteed while the simulation time of complex automotive system could be achieved in the range of several hours. In this paper, the WDF model of R, L, C is used to model the harness of the DSI3 sensor wiring harness and its noise filtering circuits. One can also use the approach for other harness modeling and load cases evaluation in automotive such as CAN or FlexRay. This is even more important as at such high speed transmission rate of CAN or FlexRay, the signal integrity at the physical layer needs to be carefully checked to guarantee a successful communication at higher layer of the protocol.

In addition, with the modeling approach presented in the paper, synthesized the R, L and C WDF models into an FPGA shall be enabled, allowing in-circuit real-time validation. If successfully synthesized, it would significantly improve the effectiveness of lab evaluation for both hardware component supplier but also system integrator as effort of preparing different wiring harness/cable tree configuration could be done now with an emulator. This is being carried out as the next steps of this paper.

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