Virtual Test: Simulating ATE Vectors in a SystemVerilog Testbench for Faster Time to Market

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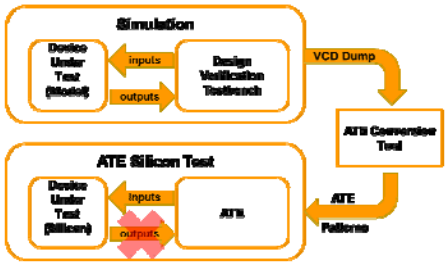
Problem Statement

During first silicon bring-up on the ATE, critical time is often wasted debugging test patterns and timing.

Common verification practices can render a testcase unusable in silicon.

For Example:
- Testbench force commands
- Memory model preload
- Artificially accelerated operations (flash erase, program)
- Testbench pullups/downs that will not exist in application

This problem is often undetected until patterns are run in silicon and the outputs do not match expected values



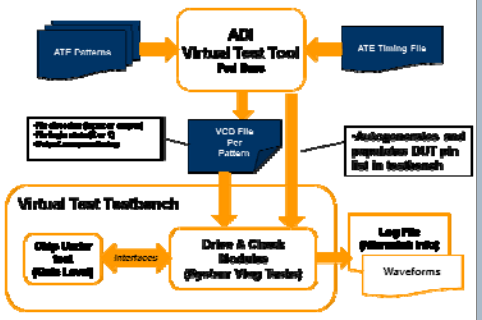
A methodology is required to validate ATE testcases across Process, Voltage, and Temperature (PVT) before silicon arrives.

Solution

Verification and product test engineers at Analog Devices, Inc. (ADI) have developed a Virtual Test Framework which enables simulation of ATE patterns in a SystemVerilog testbench to identify test-related functional or timing issues before first silicon arrives.

The Virtual Test Framework features:
- Support for both scan and functional test
- Low cost
- Very small learning curve
- Easy re-use from project to project
- Fast vector processing throughput

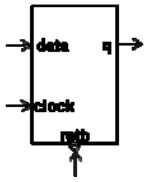
Overview: Virtual Test Framework



Part 1: The Virtual Test Tool (Perl Script)

- Generates test pattern VCD file from ATE pattern and timing files
- One VCD file per ATE pattern
- Contains 3 pieces of information per pin:
  - Pin state (1, 0, or X)
  - Pin direction (output or input)
  - Pin output strobe timing (timing matches ATE strobe)

Simple Example



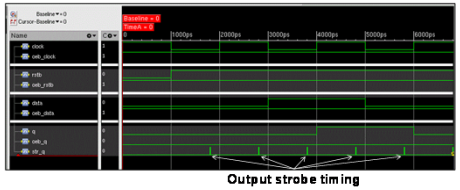
Simple DUT (D-type FF)

rstb	clock	data	q
1	0	0	L
1	0	0	L
1	1	0	L
1	0	1	L
1	1	1	H
1	0	0	H
1	1	0	L

Test Pattern

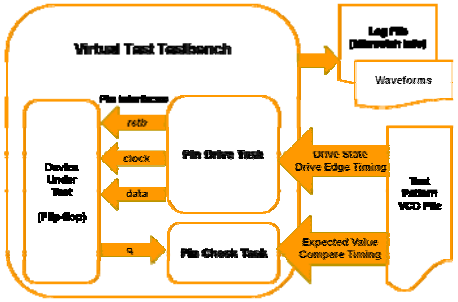
ATE Timing File → ADI Virtual Test Tool

VCD Output (Shown in viewer)

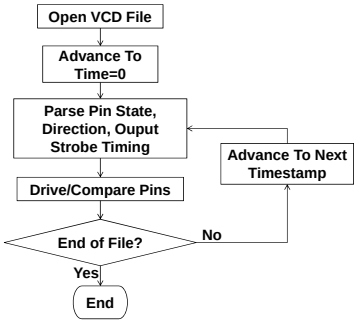


Output strobe timing

Part 2: The Virtual Test Testbench

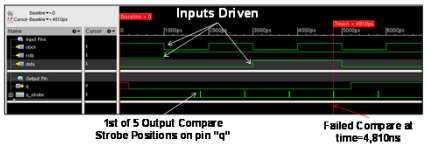


Virtual Test Flow Diagram



Simple Example: Output Delay Fault Inserted

```
ncsim> run
NOTE :: Found Initilization Section
NOTE :: Finished Initilization Section
COMPARE :: Pin q:  Expected 0 Observed 0 at time          1810
COMPARE :: Pin q:  Expected 0 Observed 0 at time          2810
COMPARE :: Pin q:  Expected 0 Observed 0 at time          3810
ERROR :: Compare of q at          4810 failed
         Expected 1 Observed 0
COMPARE :: Pin q:  Expected 1 Observed 1 at time          5810
NOTE :: END OF VCD at line 151
Simulation complete via $finish(1) at time 6810 PS + 0
```



Benchmarks And Results

Benchmarks: Processing a single test pattern

Project Type	Transistor Count	Pin Count	VCD Generation (vectors/sec)	Testbench Sim Time (vectors/sec)
Analog/Mixed	650K	32	1,200	2,100
Large SOC	100M	184	373[1]	40[1]

[1]Stuck-at-fault scan test pattern of 28k vector length. This results in a vcd generation time of 40s and testbench simulation time of 714s.

Issues Detected Prior to Tapeout

Silicon Bugs: prevented mask set revision
Clock mux bug caused glitching, resulted in non-deterministic functional tests
Race condition in scan pattern at cold, FF silicon, high voltage
Major Pattern Issues: required regeneration of ALL patterns
Scan patterns fail because a bond option was included in ATPG constraints
Start up sequence wrong
Invalid external pin pulldown in testbench
Test clock period not integer multiple of tester period
Inaccurate modeling of oscillator startup delay
Minor Test Issues: saved debug time
Inputs floated in port testmode
"Quick Sim" flash timing parameters not valid for silicon
Longer than expected pad delays identified – adjusted tester output delay timing specs
Communication port input timing needed adjustment

Conclusions

Successfully used on 3 projects at ADI to date
- Will be used for all ATE-tested projects going forward
- Easily re-usable across projects

Increased collaboration among design and product test:
- Minimal Learning Curve
- SystemVerilog environment
- Standard simulators & waveform viewers

Faster ATE silicon bring-up effort results in:
- Reduced Time-To-Market (TTM)
- Increased lifetime product revenue
- Lower product development costs.

Acknowledgments

The authors wish to acknowledge the following Analog Devices employees for their thoughtful comments and contributions during the writing of this paper: Todd Honan, Steven Pesut, and Roberta Myers