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Virtual Prototyping of Power Converter Systems based on AURIX™ using SystemC AMS

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***Abstract*— During the development process of electrical power converters, system integrators and concept verification engineers, are facing the challenge that the physical hardware (HW) and software (SW) are usually available at the late stages of their projects. Additionally, the interactions between the power electronics and electronic control unit (ECU), as well as interfacing of low-level drivers and the e.g., AUTOSAR [8] based software components and application software, is very complex and thus error prone. Due to the high-power and high-current rates, any malfunctions in operating HW and SW might lead to the physical destruction of the HW and laboratory equipment as well as could be potentially dangerous for the staff involved.**

To ease system ramp-up challenges, virtual prototyping and model-based design (MBD) is a very cost-effective and promising method. The goal is to provide a virtual prototype, which allows at one side an early start of the SW development to shorten the development cycle and to ensure to the greatest possible extent the correct and safe function of the system. To enable this, the virtual prototype (VP) must be early available in the design process, must contain all relevant components and run with a simulation performance which permits embedded software development as well as the verification of application scenarios.

This paper presents, how different state-of-the-art simulation and modelling techniques are combined to achieve this goal. Thus, the analog components (power electronics) are modelled with SystemC AMS using different modelling techniques, digital components are modelled with SystemC, and AURIX™ SystemC processor model is integrated via co-simulation interface within Synopsys Virtualizer™ Studio. The overall SystemC / SystemC AMS model is composed and integrated by COSEDA's mix signal system design and verification environment COSIDE®.

Keywords: Power Converter, LLC, Virtual Prototypes, SystemC, SystemC AMS, Control Algorithm Validation

I. INTRODUCTION

Electrical power converters HW/SW integration engineers are facing several challenges in dealing with multiple physical domains (electrical, mechanical, thermal) during the development and the ramp-up of those devices within given application scenarios.

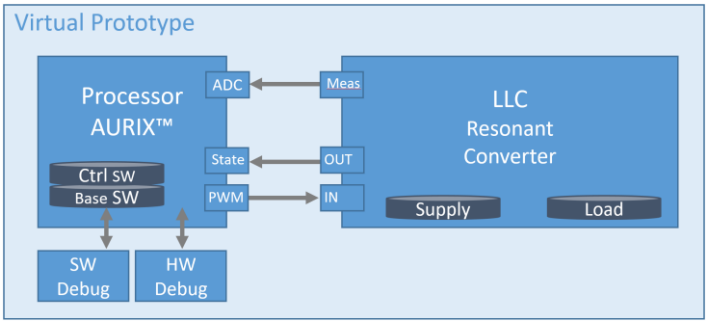

Figure 1 Overview – Virtual Prototype

The overall system (Figure 1) typically consists of the electrical power converter itself, operated by a control algorithm which is implemented as software running on an embedded processor, possibly including several safety aspects next to its main function (control of energy flow).

The system behavior is determined by a tight coupled interactions between closed loop control software (executed on the processor) that generates the required Pulse-frequency modulation (PFM) output on one side, and plant implemented as a LLC DC/DC power converter circuit on other side.
Thus, the development of productive SW like low level drivers, AUTOSAR components as well as application layer software is very challenging, due all these developments require a closed loop scenario.
Also providing in a cost-effective approach answers on questions such as what is a proper AURIX™ device for the given application by estimating CPU load, exploring different plant topologies as well as tuning and debugging of control algorithm (full hierarchical traceability over process internal variables) are challenges in early stages of a project.

To enable SW development as well as functional verification based on a virtual prototype all the described components have to be modelled. Furthermore, especially the SW development use case requires a very responsive reaction of the model. Additionally, the verification of application scenarios requires the simulation of long time intervals. Thus, the requirement for the simulation performance is very high. At the other side, also the required timing accuracy of the model including the software execution is high, due a closed loop behavior is very sensitive to timing variations.
To meet the requirements, different abstract modelling techniques has to be combined.
In this paper we will show, that the co-simulation of analog components will not limit the simulation performance, when abstract modelling techniques like supported by SystemC AMS are used. At the other side, the paper will demonstrate, that a sufficient timing accuracy is achievable with fast simulating processor models like provided by Infineon/Synopsys. This paper will also show how the models of different domains and the application SW can be combined within one overall system level virtual prototype.

II. PLANT MODEL DESCRIPTION

A. Plant system

Isolated DC/DC power converters implemented as one of the variants of resonant topologies are often used in automotive industry since they are relatively easy to control and considered to be simple from electronic active/passive components point of view and. Drawback of such power converters is sub-optimal efficiency in overall operating range (efficiency can be optimized just for one, usually nominal operating point) - also significant experience in definition and selection of HF transformer (as converter crucial component) should not be neglected. In this paper a unidirectional series-parallel resonant LLC DC/DC topology is discussed as shown on Figure 2. The implemented LLC DC/DC converter is part of an On-Board Charger (OBC) and as such it's designed for power and voltage ratings that are shown in Table 1. DC Bus Voltage and Battery Voltage in Table 1 are referred as V_1 (voltage - primary side) and V_2 (voltage - secondary side) in Figure 2 respectively. On both, primary and secondary side as a power switches are used Infineon Technologies (IFX) well established CoolMOS™ 650 V MOSFETs in implemented Easy1B package as H-bridge module (F4-50MR07W1CFD7A_B11A). On primary side, as gate drivers are used IFX AUIRS2191 half-bridge gate drivers. On the secondary side, in order to operate MOSFET's as diodes the AUIRS1170S high speed synchronous rectifier control IC's are used to do both: drive low side MOSFETs (depicted as D_1 and D_3 on Figure 2) and control high side gate driver IC's AUIRS2123S that are in turn then driving secondary high side MOSFETs (depicted as D_2 and D_4 on Figure 2).

	Nominal	Minimum	Maximum
DC Bus Voltage [V]	380	360	400
Battery Voltage [V]	280	250	420
Load Power [W]	3300	400	3700

Table 1 Power and Voltage Ratings

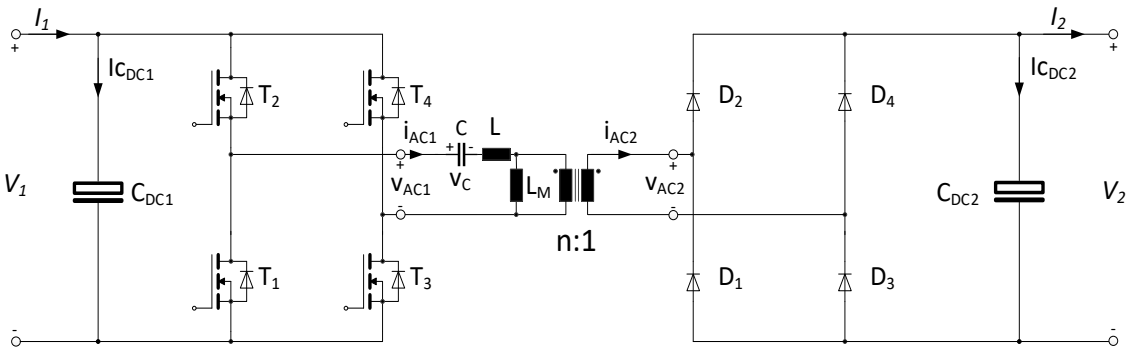

Figure 2 Principle Schematics of Isolated Unidirectional DC/DC Converter

Nominal operating point of DC/DC determines components selection of resonant network on primary side of dual bridge consisting of capacitor C, inductor L and HF transformer magnetization inductance L_M. Depending on the construction of HF transformer there are 2 options: as a resonant inductance L is used either externally added inductor or stray inductance of HF transformer itself. Each of those options influences the operation (resonant frequency, ratio between transformer magnetization and primary current) of power converter and has some advantages and drawbacks, but discussion of those is out of scope of this paper and can be found in [3][4].
The algorithm to control the T_x transistors are described in the control algorithm section.

B. Plant Model

The plant is modelled straight forward using SystemC AMS Electrical Linear Networks (ELN) Model of Computation (MoC) (see Figure 3). For the first attempt the MOSFETs on LLC primary side are abstracted as switches (ON/OFF resistance), on the secondary side, rectifier MOSFETs are operated as diodes, thus they are modelled as diodes using Piece Wise Linear (PWL) techniques. To enable further improving and upgrading of simulation models of the power switches and the transformer are implemented as hierarchical macro models. Using this approach, it is comfortable to add new model features and effects, without overloading the top-level structure of the LLC model.

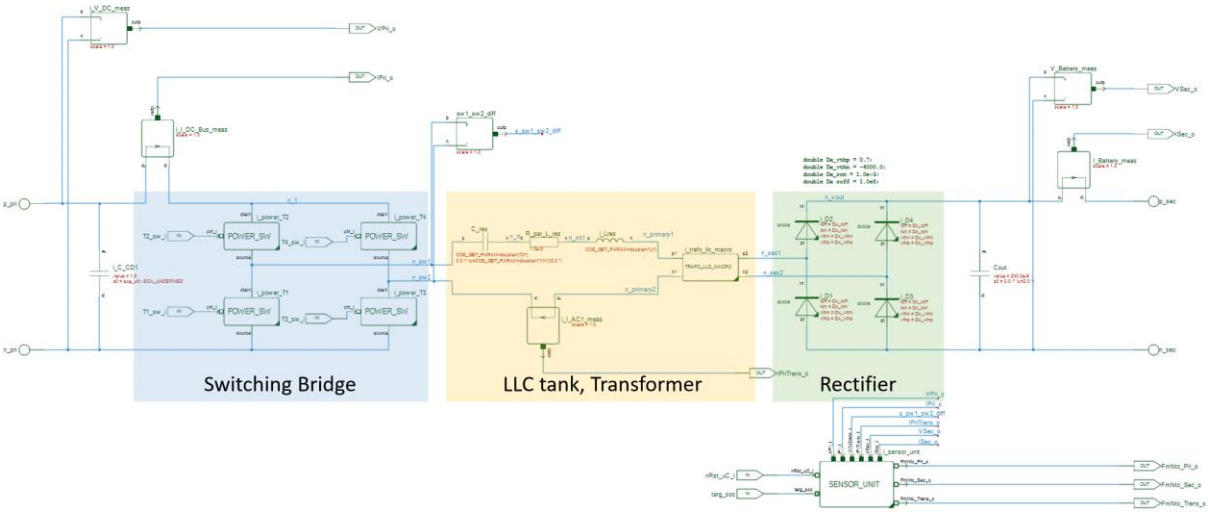

Figure 3: Plant Model

The idea of this approach is to start simple with the minimal number of modeled effects - to be fast in simulation but still precise enough to model the LLC behavior in the desired manner. The correct behavior of modeled plant was confirmed by open-loop simulation using another analog simulator, and it was proven that the controlled variables on secondary side (voltages and currents) reached a certain value for given conditions of PFM, primary side voltage and load.

The sensor unit contains a thermal network that models self-heating of the power switches during operation, that might be used for checking the fail-safety mechanism in control SW. The internal details of this subsystem are out of scope and will not be explained further in this paper.

III. AURIX™ PROCESSOR MODEL

A. Infineon/Synopsys AURIX™ Processor Model

The Virtual Prototype (VP) is simulation platform of complete System on Chip (SoC) that is capable of executing application software without any changes. The VP is available early in product life cycle as early as a year before Early Engineering Samples (EES) enabling SW development to be front loaded and hence enabling Time to Market. The VP offers a rich set of debugging, tracing and analysis features enabling co-debugging of hardware and software and thus reducing time and effort needed for fixing complex failures. As VP is a software model, every bit, register, state variable and internal signal can be manipulated through external scripts to inject any error scenario. This helps to improve the test coverage of software and to enhance its quality and safety aspects.

Traditionally the usage of VP is limited to only pre silicon software validation across various industries. However in Automotive, the trend of using simulation based validation in post-silicon phase is evolving across Tier1s and OEMs primarily as it helps to reduce to overall cost by replacing Hardware-in-Loop setup by virtual Hardware-in-Loop.

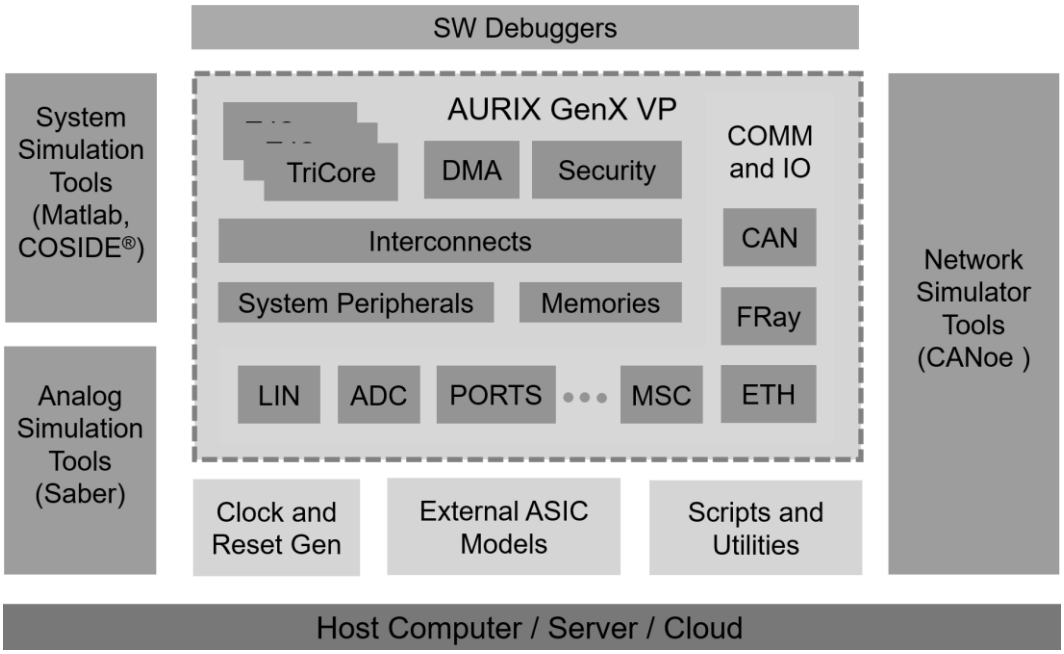

Figure 4 AURIX™ Virtual Prototype in Product to System Context

Figure 4 shows the integration of AURIX™ VP in system context. The various functional blocks of the AURIX™ are modelled using SystemC/TLM2.0 and the complete virtual prototype is integrated using Synopsys Virtualizer® tool suite. The AURIX™ VP is calibrated to offer more than 90% cycle timing accuracy. The AURIX™ VP can be integrated with models of power supply and other ASICs making it a virtual ECU. The AURIX™ VP supports interface to traditional SW debuggers to enable debugging of SW that are executed on simulated cores in the VP. It also supports interface to co-simulate with third party tools including COSEDA/COSIDE®.

B. Integration of Processor Model

To integrate the AURIX™ VP into the overall system model, a shared memory based co-simulation interface is used. Therefore it contains a SystemC model (see Figure 5) which implements the co-simulation interface and maps the AURIX™ VP in/outputs to its entity, so the data can be transferred from the plant to the AURIX™ VP and vice versa.

```
////////////////////////////////////////////
// method called by constructor           //
////////////////////////////////////////////
void aurix_tc39x::construct()
{
    s.i_aurix_c->register_port(VPri_i, "VPri_i", "IOStubs/Analog/AN6");
    s.i_aurix_c->register_port(IPri_i, "IPri_i", "IOStubs/Analog/AN30");
    s.i_aurix_c->register_port(VSec_i, "VSec_i", "IOStubs/Analog/AN14");
    s.i_aurix_c->register_port(ISec_i, "ISec_i", "IOStubs/Analog/AN22");
    s.i_aurix_c->register_port(G4G1_o, "G4G1_o", "GPIO/IO_P00_2");
    s.i_aurix_c->register_port(G2G3_o, "G2G3_o", "GPIO/IO_P32_3");
    s.i_aurix_c->register_port(FmNtc_Pri_i, "FmNtc_Pri_i", "GPIO/IO_P11_13");
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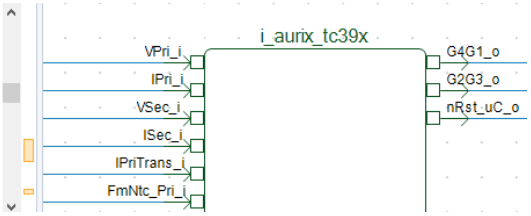
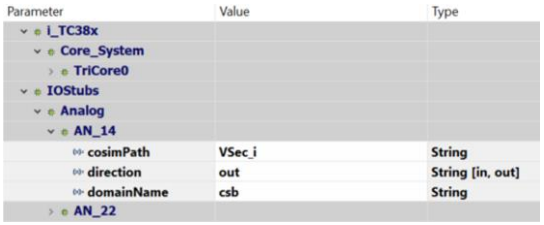


Figure 5: COSIDE® - SystemC model with co-simulation interface

For example the secondary side voltage ("VSec_i") is registered in the AURIX™ VP configuration (see Figure 6) to the analog pin AN_14 which corresponds to the SystemC model entity within the overall system level model in COSIDE® (see Figure 5).



Parameter	Value	Type
i_TC38x		
Core_System		
TriCore0		
IOStubs		
Analog		
AN_14		
cosimPath	VSec_i	String
direction	out	String [in, out]
domainName	csb	String
AN_22		

Figure 6: Synopsys Virtualizer – configured VP for co-simulation

IV. CONTROL ALGORITHM (SOFTWARE)

The C-code of LLC control algorithm is merged with the low level drivers, compiled, downloaded and executed on AURIX™ virtual prototype in order to operate the connected LLC converter model: PFM outputs of AURIX™ are directly driving gates of primary side switches of LLC, whereas voltage and current sensors in LLC model generate feedback signals for closed loop control.

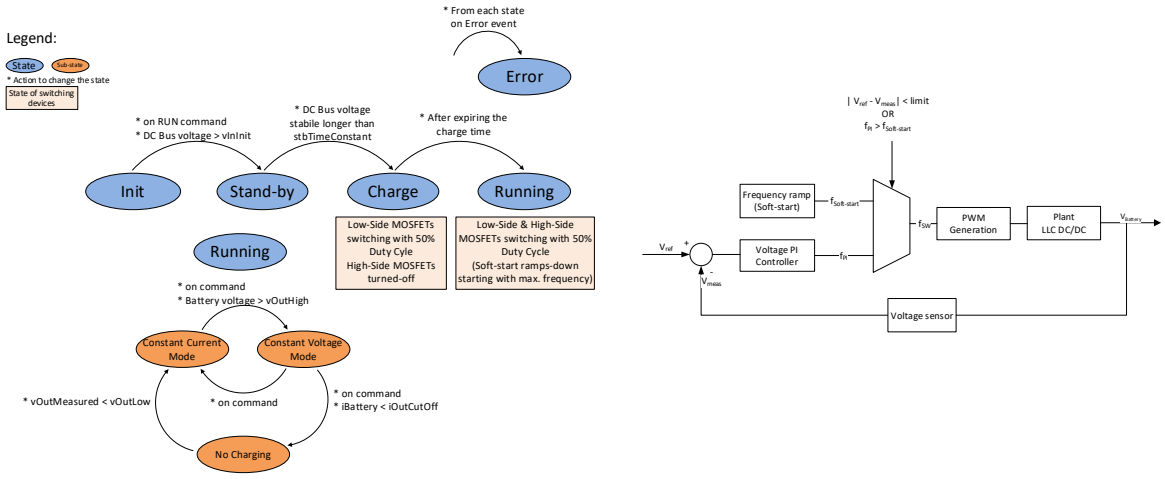


Figure 7: State Machine – Overview and soft-start procedure

The control of output voltage/current of LLC unidirectional DC/DC converter is based on PFM implemented in Infineon's AURIX™ microcontroller by means of PI controller. Principal functionality of converter state machine is shown on Figure 7. As it can be seen on state-machine flow, after the charging stage is finished (to enable the bootstrapping of the gate driver capacitors), the soft-start procedure is triggered. During the soft-start the switching frequency is being ramped-down, starting from maximal allowed switching frequency – the soft-start is finished

when either the switching frequency calculated by PI controller becomes higher than ramped-down frequency or when the difference between battery voltage reference and measurement is below certain limit.

V. MODEL INTEGRATION

The overall system model contains of two main parts: the AURIX™ virtual prototype and SystemC-AMS model of LLC DC/DC converter (represented on Figure 8 by blocks named "AURIX_TC39X_TOP" and "LLC_TOP"

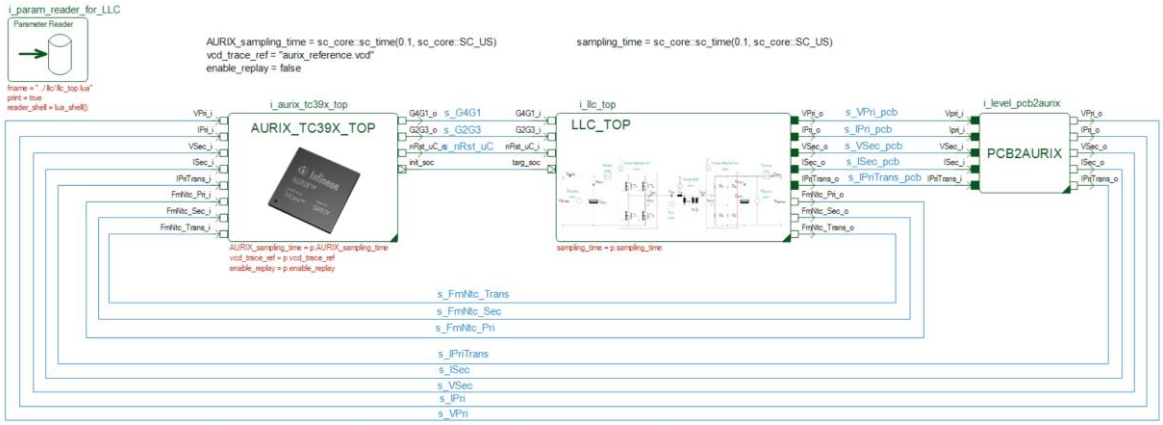


Figure 8 Toplevel: System Model – AURIX™ with LLC Converter

respective). LLC model includes all active/passive electronic components including sensing of voltages, currents and temperatures in order to enable closed loop control and some safety mechanisms (like overvoltage/overcurrent or overheating protection).
The AURIX™ co-simulation interface and the LLC model is connected via SystemC boolean signals in case of driving the gates of the switching bridge. The measured feedback signals are scaled by the "PCB2AURIX" model to meet the AURIX™ VP ADC range of 0 to 5V. The temperature sensing outputs and some LLC internal failure registers are connected as well.
The parametrization of the overall model is ensured by a parameter file reader model which is able to execute parameter calculations in a scripting shell. These parameter are symbolical accessible in the subhierarchies.
Compiling the overall system level model a single executable is created. Executing this binary the model gets elaborated and waits for the AURIX™ VP to connect as already described.

RESULTS

A. *Example scenarios*

To depict operation of power converter, two scenarios simulated, in both cases, the primary side was supplied with input voltage of 360V and load on the secondary (output of LLC) was 3700W. In the first scenario the reference of output voltage was set to be 420V (Figure 9/l.) – in the second scenario (Figure 9/r.) reference of output voltage was set to be 240V.

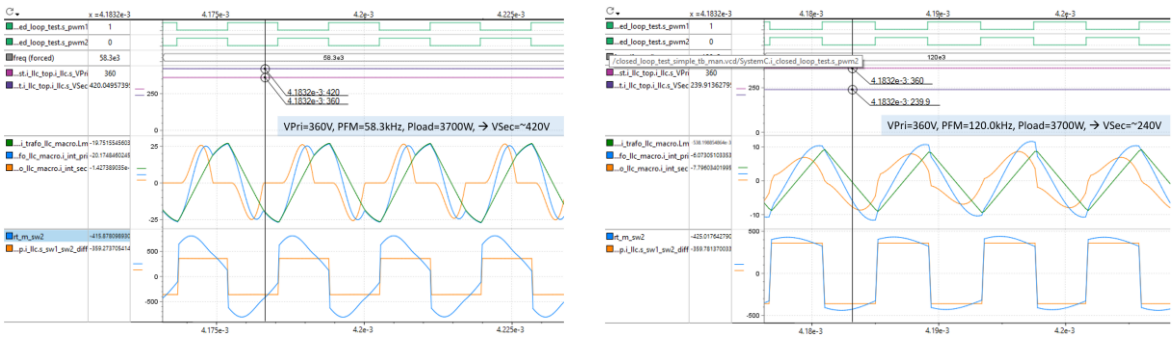


Figure 9: Simulation result: 58.3kHz → VSec=~420V (l.), 120kHz → VSec=~240V (r.)

The expected PFM frequencies are reached by the control algorithm as expected. Further investigations like dynamic supply and load changes as well as fault injection can be applied to this overall system. This becomes of special interest if the fail-save mechanism of the software as well as the temperature monitoring should be tested.

B. Software Debug / Development

One of the main advantages of an overall system simulation is the ability to debug every corner of the design, since internals are visible via tracing or via a debugger. On the AURIX™ VP side an e.g. Lauterbach or PLS debugger can be attached to be able to debug the control algorithm software (Figure 10). In conjunction to the processor, the plant can be analyzed using a mixed signal wave viewer where the analog traces of the LLC and the PFM signals can be displayed. Furthermore another debugger can be hooked to the overall system level model to get further insights in case of an error prone behavior.

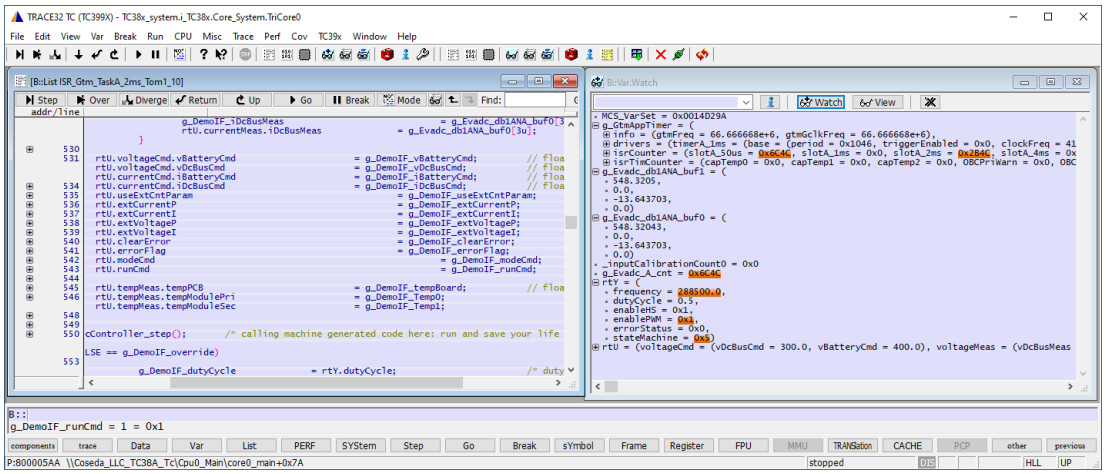


Figure 10: AURIX™ VP attached Lauterbach Debugger

VI. SUMMARY

The usage of virtual prototyping in the area of power converter system holds new challenges since plain digital VP's are not sufficient in this area, where the plant model and its dynamic feedback plays a significant role in the overall system. Especially the control algorithm bring-up introduces this challenge, since it can be implemented and debugged more efficient in a closed loop scenario. For using such a mixed-signal system level VP for control software development, it is essential to have fast turnaround times enabling algorithm adaptions and re-running the overall simulation.

Dealing with power converters with high power rates emphasized importance of the safety aspects, because system operating malfunctions can cause physical damage of the laboratory equipment as well it can be dangerous for the staff operating that equipment.

Connecting different HW components, like the AURIX™ controller board with the LLC PCB, the battery and some load emulations in the laboratory is as well quite challenging, since a connectivity issue including broken wire etc. complicates the reproducibility of some measurements, not to mentioned error injection scenarios.

Beside these advantages of a mixed signal VP, there is a time-to-market aspect as well. VP's are typically already available much earlier before the first system level HW setup is available. Thus customers are able to setup and implement their applications much earlier in their design cycle.

Furthermore, the customers can give valuable feedback on the next generation AURIX™ features, since they can analyze the HW/SW performance, explore power converter topologies and certain functionalities in their application scenarios.

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