2021 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION CHINA
SHANGHAI | MAY 26, 2021

accellera SYSTEMS INITIATIVE

SIEMENS

Veloce HYCON Software Enabled SoC Verification and Validation on Day 1

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Agenda

- Market Trends
- Veloce HYCON Overview
- Veloce HYCON Use Cases
- Veloce HYCON Case Studies
- Summary

Market trends: SW-enabled verification and validation

Percentage of SoC costs spent on SW design & verification increasing

- IP integration costs in SoC design & verification rising

SoC verification and validation drive product schedule

- SW workloads driving silicon success

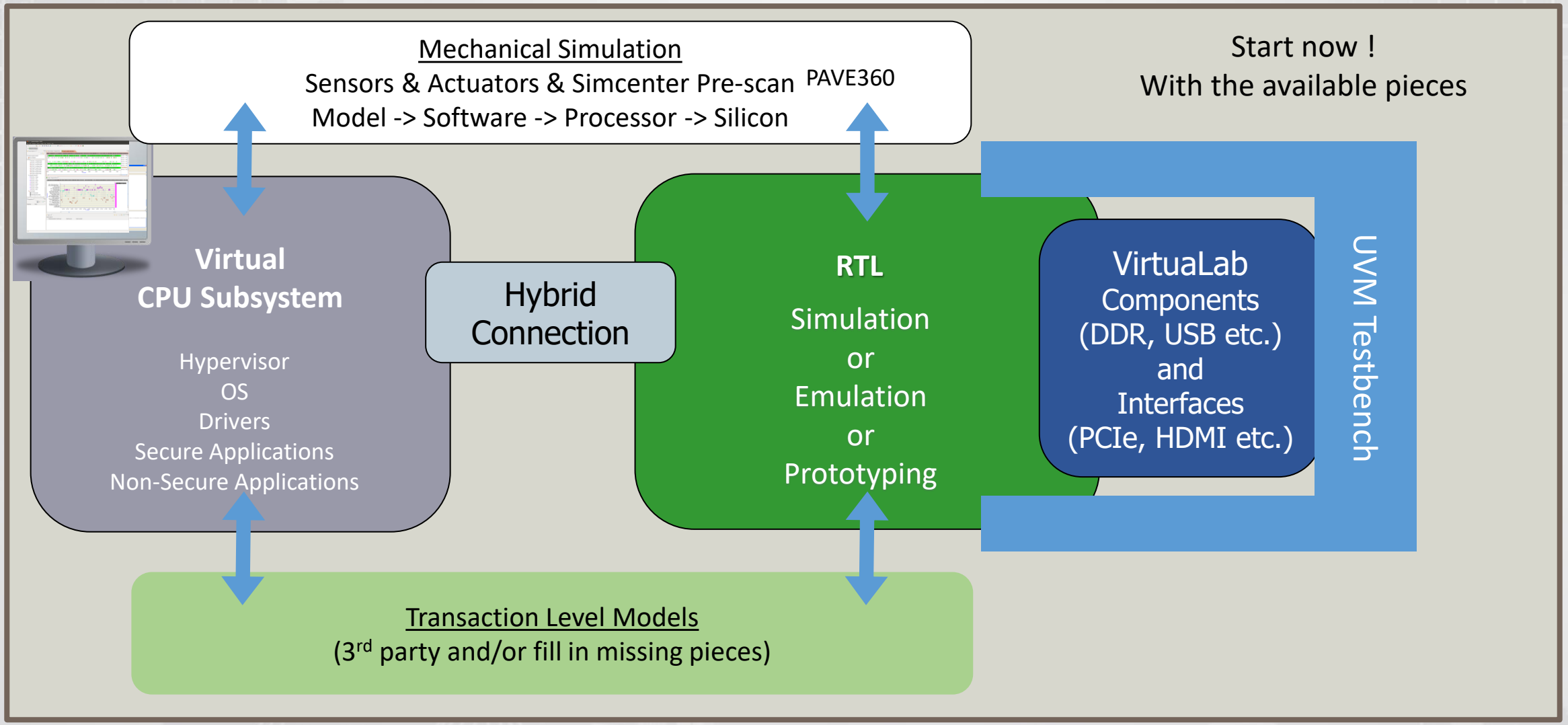
Significant complexity of creation of an end-to-end solution

- Demand for improved verification efficiency/productivity

Use cases drive need for better SoC verification solution

- SW developers require performance & HW use cases require accuracy

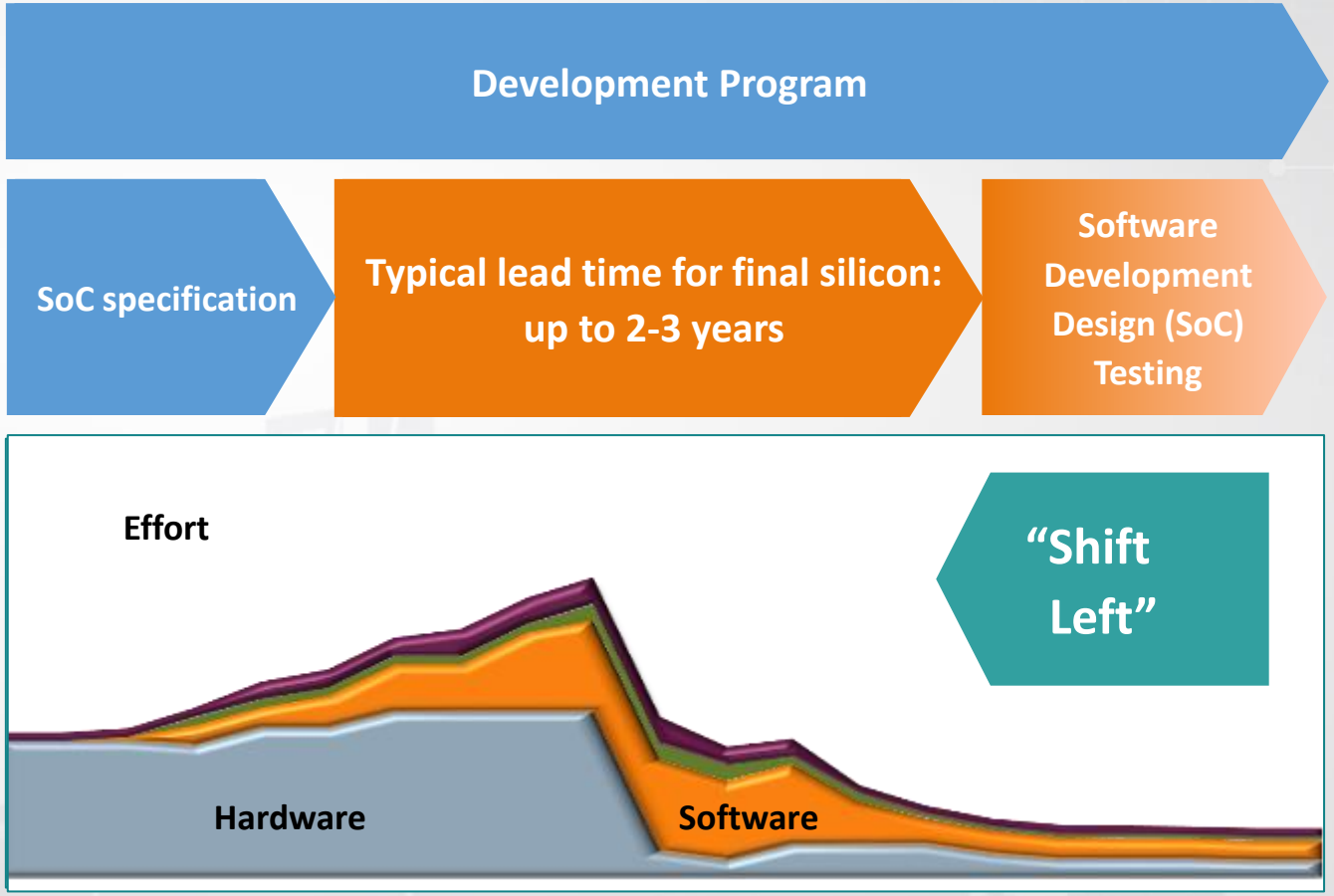
Siemens EDA: Accelerate the development experience



Pre-Silicon SW verification and validation

Pre-silicon view of SoC, including software workload validation and characterization

- SW verification and validation increasingly drive product and schedule risk
- Ability to start early with pieces of SoC building up to SoC enables virtual build-up of functionality and SW
- Ability to analyze workload and impact on SoC power and performance critical in key markets – e.g datacenter, gaming, mobile, AI/ML
- High-fidelity simulated and emulated representations of SoCs allow a ‘shift left’ in SW validation
- Enabling pre-silicon
  - SW workload analysis
  - Power and performance analysis

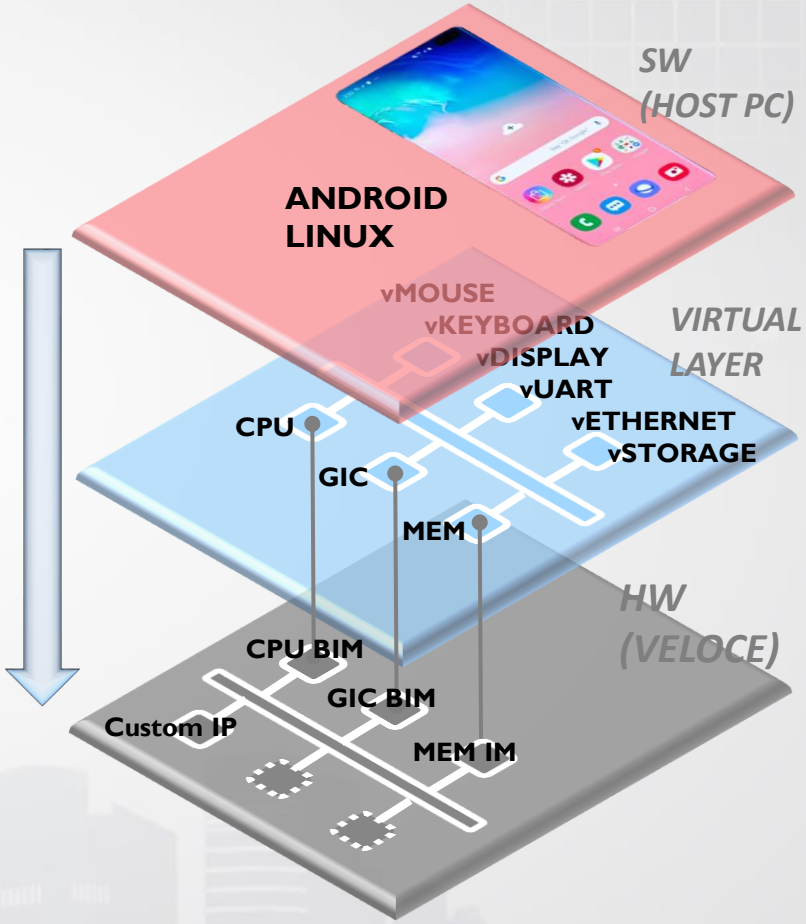


Veloce HYCON: Configurable Virtual Platform + Hybrid + SW Stack

- **HW: Configurable DUT**
  - Includes: CPU, GIC and Memory BIM (Bus Interface Model) connections
  - Connect basic IP on day 1
  - Incrementally verify RTL components while keeping rest of platform at TLM level

- **SW: Begin SW development immediately**
  - Reference software stack available from ***day 1***
  - Flexibility to add new drivers and applications

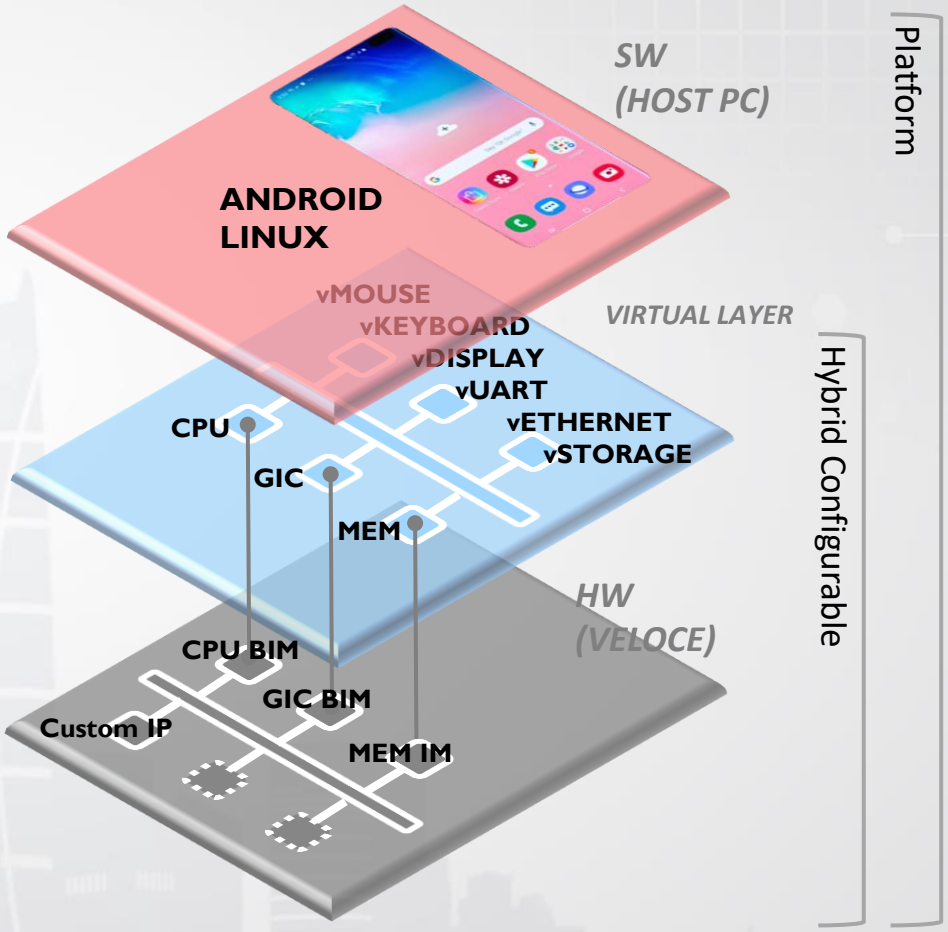
- **Run Fast – Run Accurate**
  - Boot SW in virtual machine
  - Transfer CPU+GIC+Memory state to full SOC RTL
  - (Optionally) Continue to use virtual devices in VM, via transactor



Veloce HYCON provides a skeleton SOC reference platform, that customers incrementally add custom hardware and custom software, to transform it into their SoC

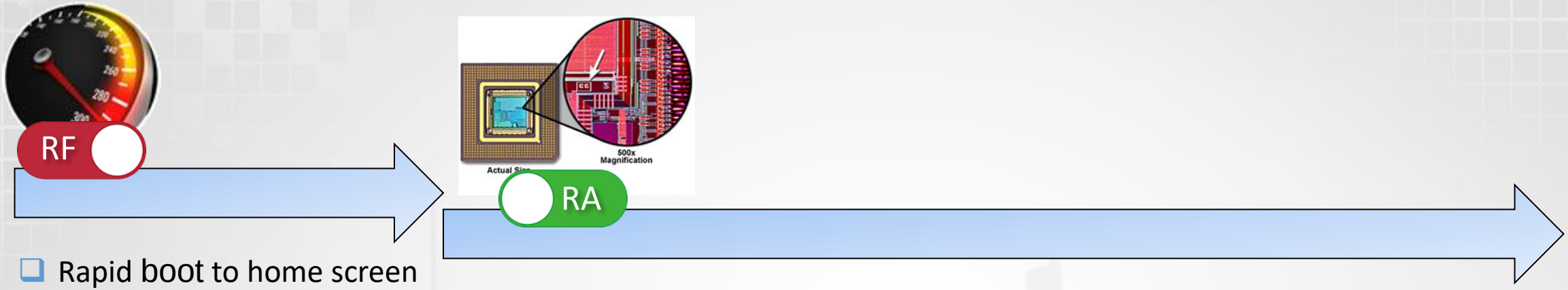
Veloce HYCON: Configurable Virtual Platform + Hybrid + SW Stack

- **Reference platform booting OS – Arm V8 and Arm V9**
  - Boots Linux in Seconds
  - Boots Android in Minutes
  - Decouples SW Dependencies on HW teams
- **Platforms are enabled with critical features**
  - Dropbox; networking; Virtio; etc
- **Enables SW driven design methodology**
  - SW enabled IP validation begins immediately
  - Run End-User Applications, Tests, Diagnostics & Benchmark
- **Methodology support for power and performance analysis**
- **Unique ability to checkpoint HW & SW environments and replay it**
- **Support for IP integration and SoC usage modes**



Veloce HYCON customers validate their designs months earlier than previously allowed

Veloce HYCON RFRA (Run Fast, Run Accurate)



- Rapid boot to home screen
- Rapid application test, driver development
- Virtual Peripherals with no SoC alteration
- Switch at customer area of interest

- Accurate bus, and cache performance metrics
- Power consumption and system level bottlenecks
- Continue to use Virtual Peripherals

Performance when you want it, accuracy when you need it

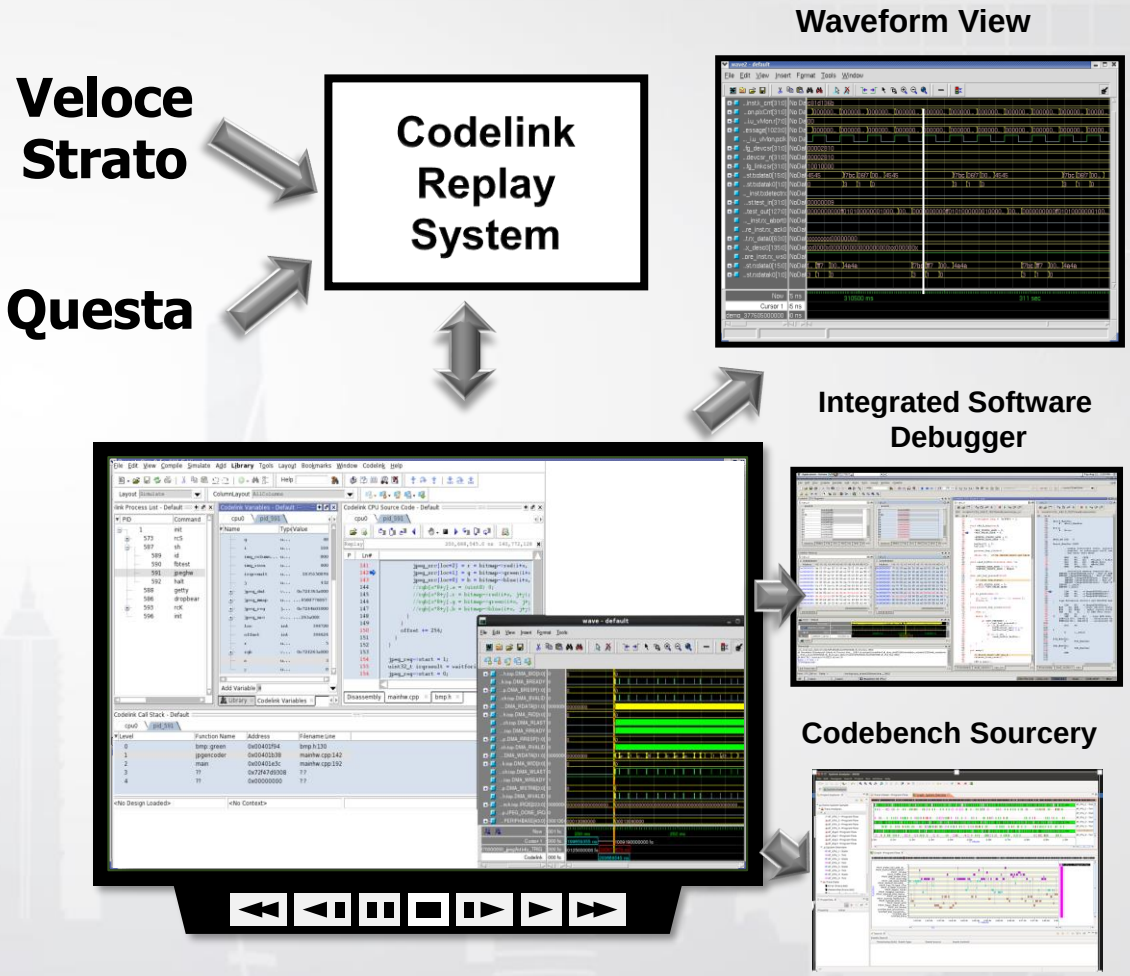
Allowing users to execute large amounts of SW quickly, then accurately run the SW they are most interested in

Veloce HYCON Checkpoint

- Save HW and SW state at a certain point
- Replay from this point
- Provides checkpoint capability for HW & SW (callbacks implemented for Veloce save & restore API)
- Uses Veloce record-replay feature as an engine
- Save multiple checkpoints in a single run
- Works in conjunction with RFRA (run fast, run accurate)
- Support for Veloce HYCON SW stack and customized SW

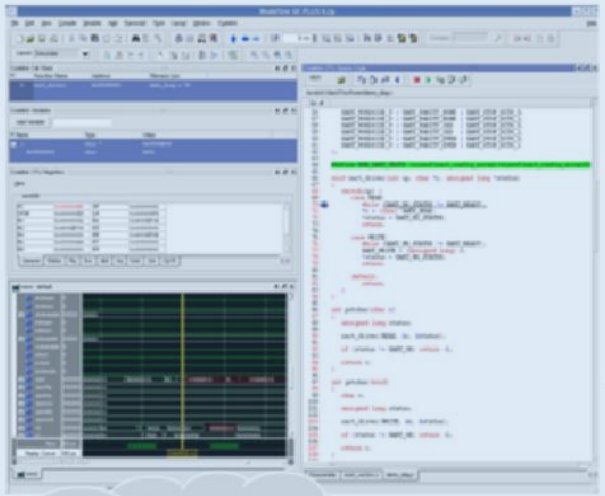
Veloce HYCON and Veloce Codelink integration

- **Offline SW debug with waveform/protocol/power connectivity**
  - Discover what the SoC is doing, and impact on performance
  - Simulation & Emulation Debugging
- **Software is "replayed" after being traced during simulation/emulation run**
- **Debug in reverse is much faster**
  - Starting from the failure work back to the cause
- **Single run to trap the issue**



An integrated solution from Siemens EDA

Software/OS Analysis



Software debug

Coverage

Profiling

Software Stacks

CPU(s)

Virtual Peripheral

Virtual Machine

Hybrid Layer

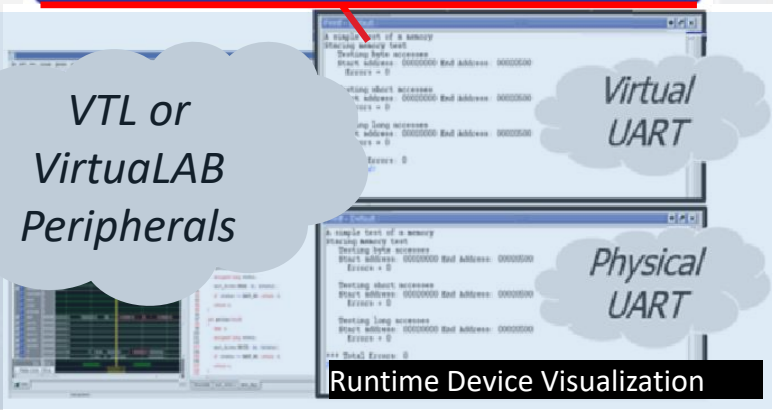
Veloce HYCON Hardware Platform

uCPU

Customer IP(s)

HW I/F

VTL or VirtuaLAB Peripherals



Virtual UART

Physical UART

Runtime Device Visualization

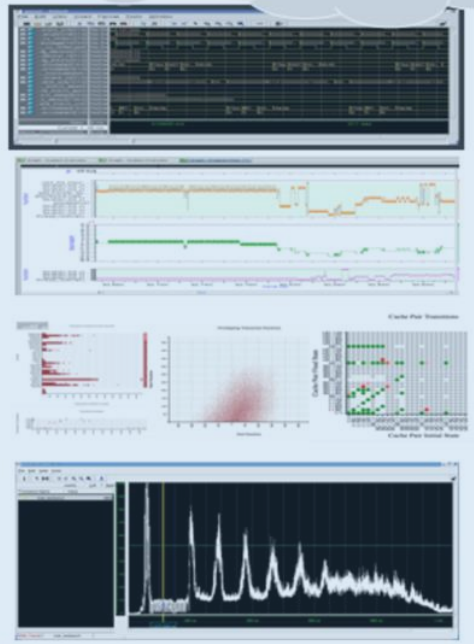
Profile

Power

Wave

Protocol

Interconnect metrics

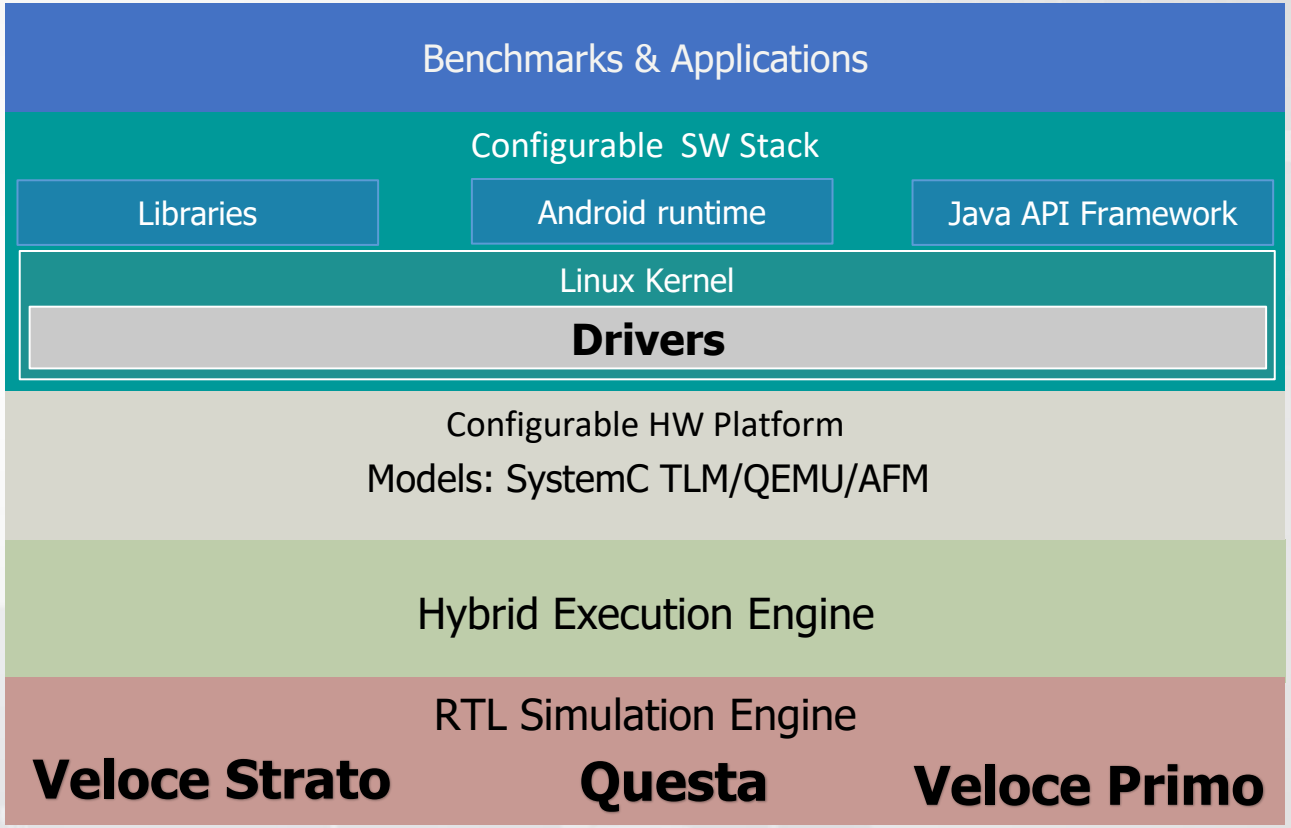


Hardware Analysis

Veloce HYCON use cases

Use Case #1: Device driver validation

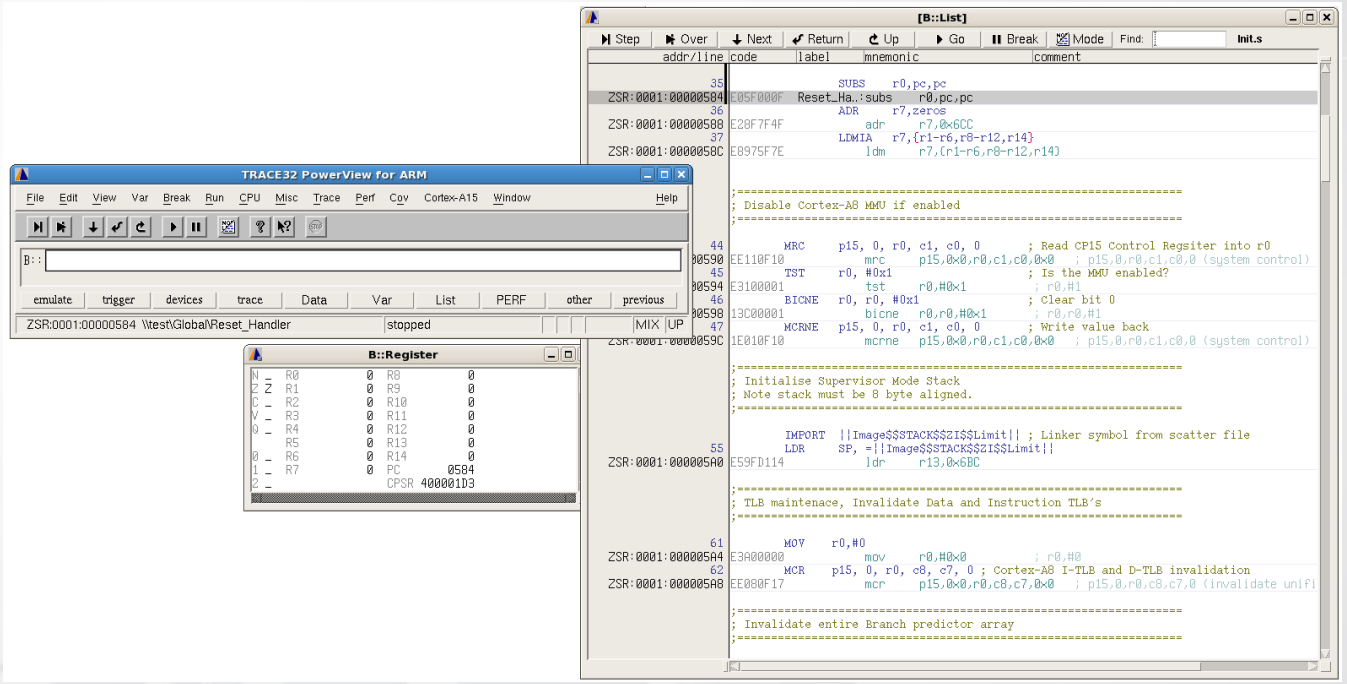
- **Create, debug and validate kernel device drivers**
- **Static and dynamically loaded symbols**
- **Continuous integration and regression testing**
- **Virtual and RTL**
  - Performance vs accuracy
  - Switching between modes
  - Fast OS boot>>>HW Accurate



Use Case #1: Debugging firmware in Veloce HYCON

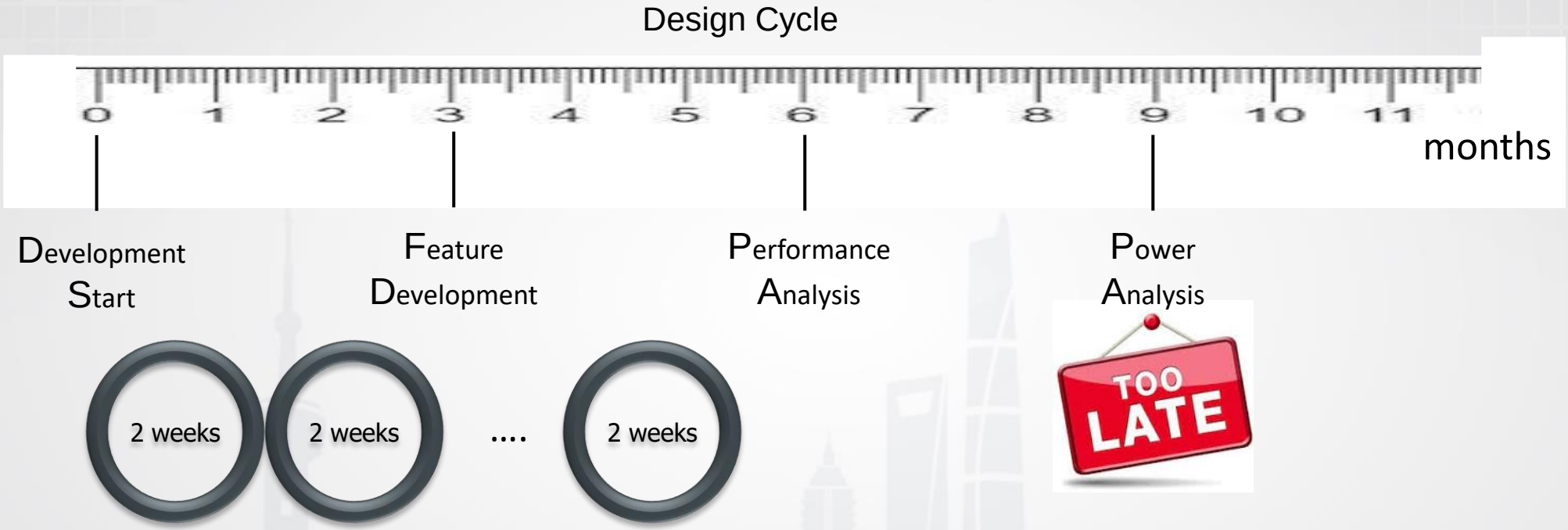
- **Debug is performed ….**
  - Live against the virtual machine, this improves debugger responsiveness against RTL
  - Offline against a recorded execution; able to reversibly debug improves productivity

- **Supported Debuggers**
  - Codelink Native UI
  - Trace32
  - Siemens EDA Codebench
  - DS-5
  - or any other GDB RSP tool (gdb, ddd, …)



Use Case #2: Identifying power anomalies

Challenge



Solution

- Veloce HYCON enables you to run ANY application, identify power and performance areas of interest, compare with previous design runs, starting at feature development – in month 3.

Use Case #2: Power analysis

No waiting for full RTL to be ready,
→ Run Power analysis on incremental developed RTL IPs

Power distribution Visibility Pre-Silicon

Compare Power graphs of design Revisions

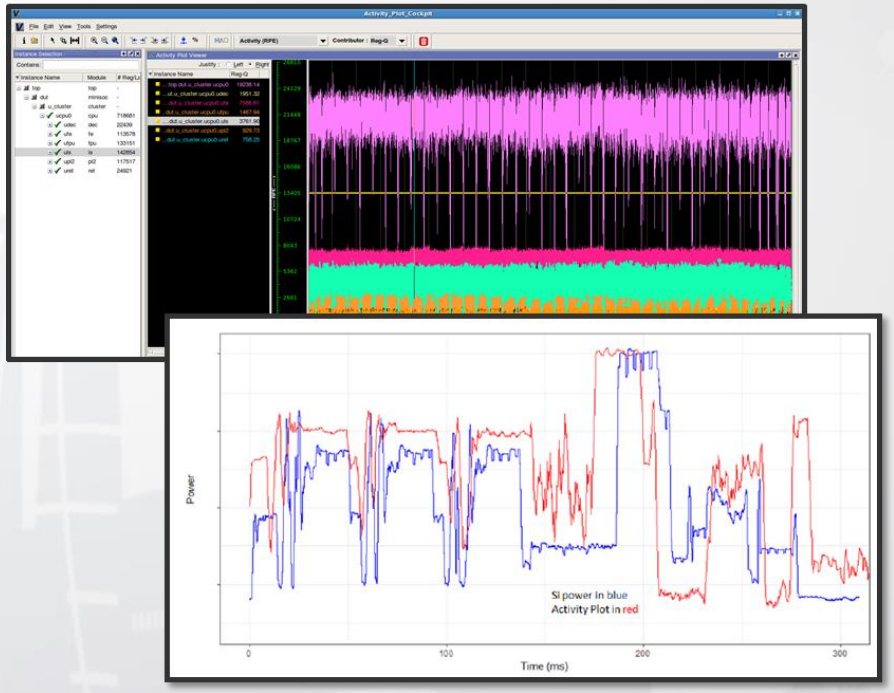
Power

Power Activity Plot

- Per system
- Per sub-system modules
- Per time boundaries

Pre-silicon Power Anomalies detection

Power Distribution



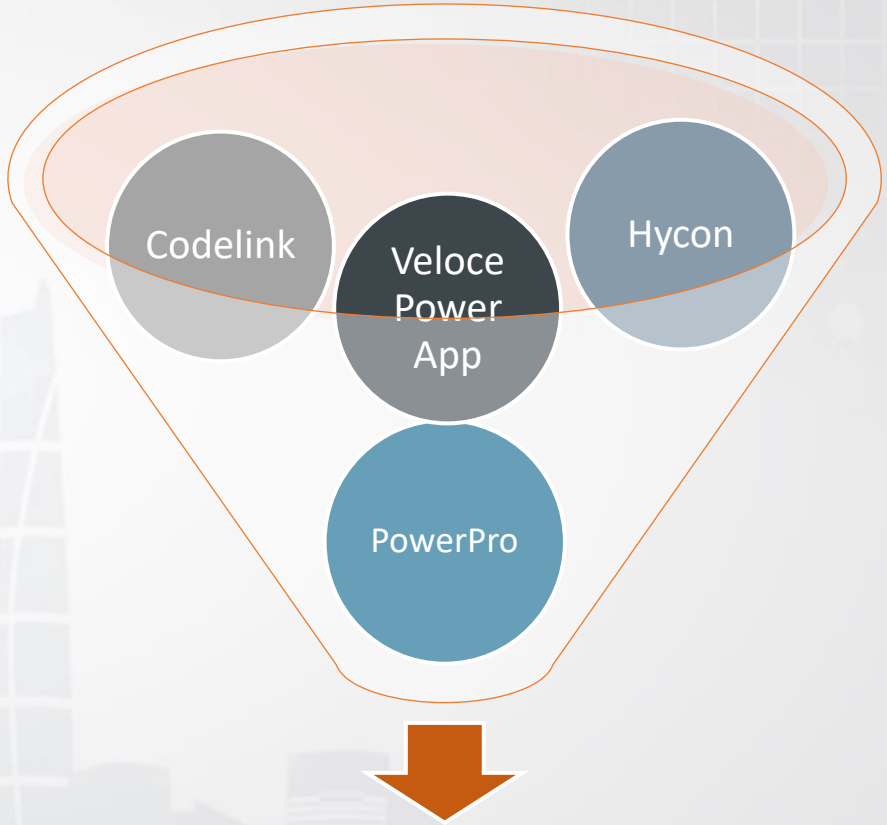
Power Distribution comparison

Use Case #2: Power analysis

- **Execute**
  - Allow selection and execution of relevant **End User App**
- **Extract**
  - Allow extraction of power information in a time-based manner
    - Gross power
      - Too high to shut down the DUT
      - Power threshold: break down point
    - Power anomalies
      - Places where power levels differs from requirement definition
- **Analyze**
  - Allow comparison with previous designs and previous runs
  - Allow correlation between performance and power
- **Optimize**
  - Allow changes to SW and/or RTL to meet power requirements

Siemens EDA power solution

- **Veloce HYCON**
  - Run SW application
  - Debug end-user application
  - Expose HW/SW interactions
- **Veloce Power App**
  - Capture activity plots
  - Convert activity plots into power approximation (RPE)
  - Compare power graphs
  - Incorporate performance graphs
  - Connect to real power in PowerPro
  - Link to SW in Codelink
- **Veloce Codelink**
  - Analyze SW based on power I/Ps
  - Create snippets
  - Process aware
  - OS aware
- **PowerPro**:
  - Extract absolute power from RPE



Analyze & optimize SoC power profile

Siemens EDA power flow high-level view

Customer Benchmark / SW Application

Veloce HYCON

Linux

Angrybirds

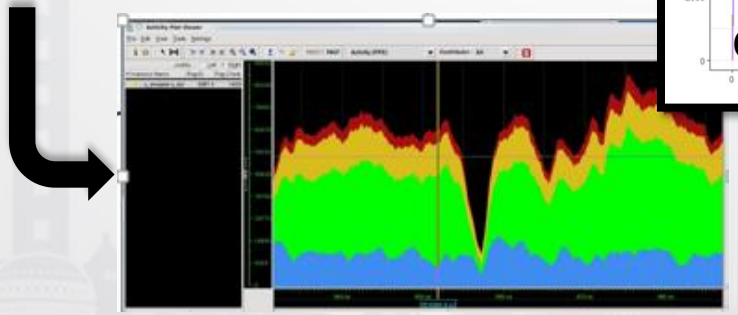
ANDROID

Configurable HW Platform

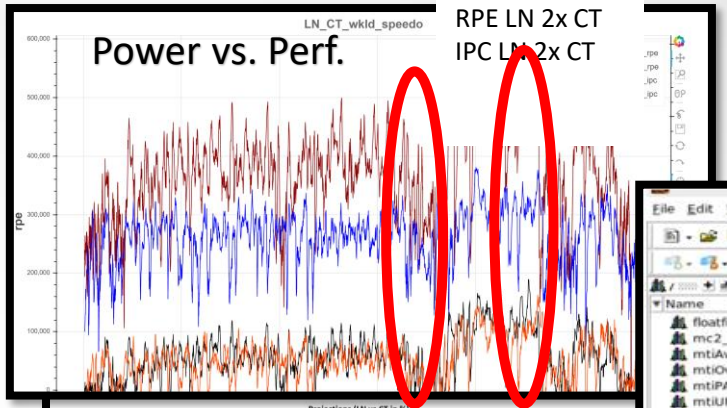
Hybrid Execution Engine

Veloce

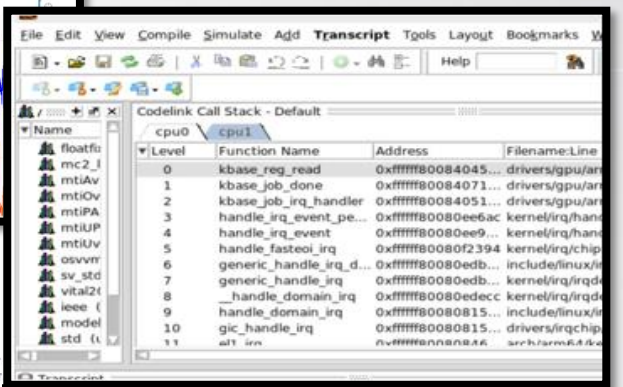
Veloce Power App

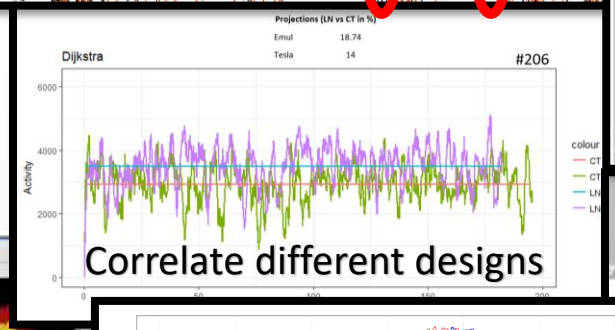


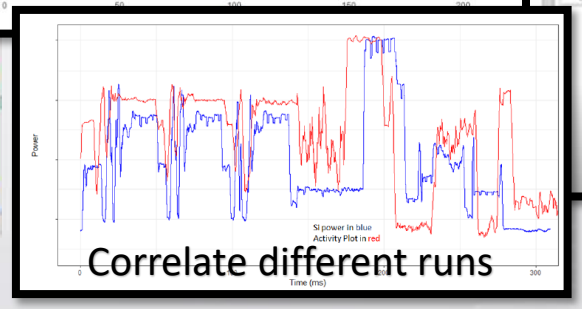
Activity Plot

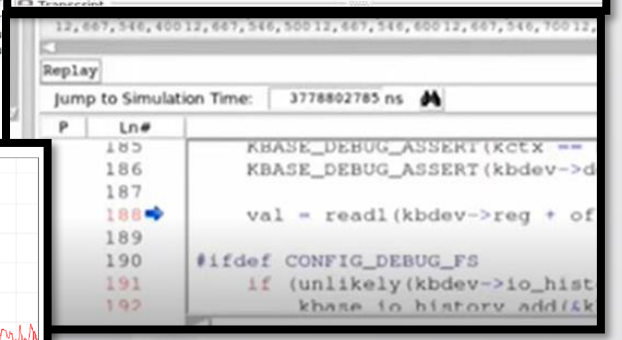


Trace to HW









Trace to SW

Veloce HYCON Case Studies

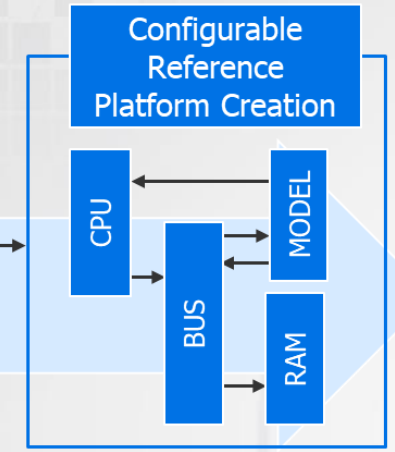
Case Study #1: Power profiling with real workloads

Veloce HYCON

SYSTEMC™ TLM

arm FAST MODELS

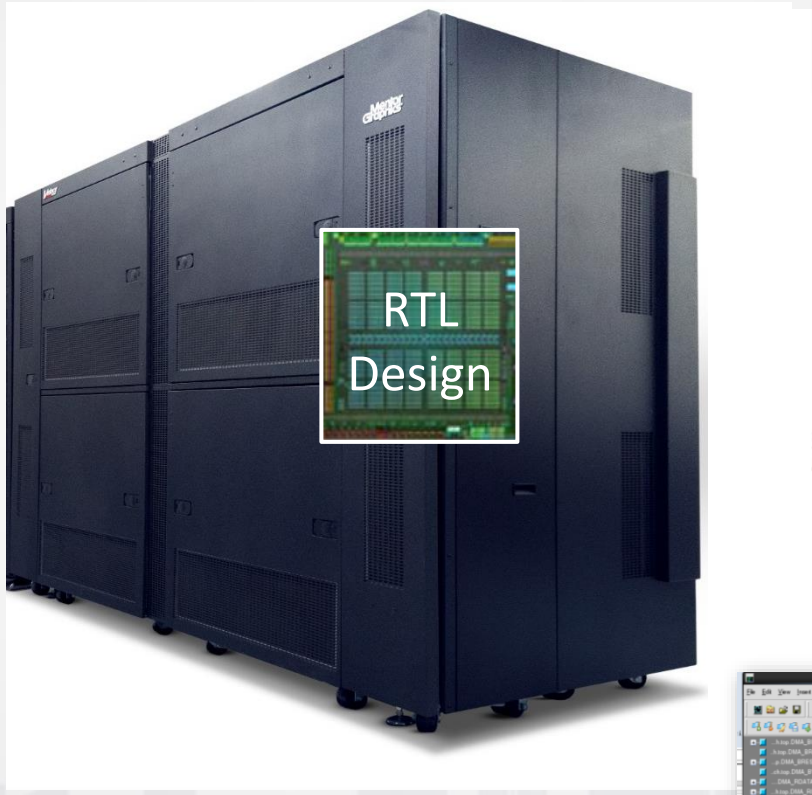
QEMU



Benchmarks running on RTL Design

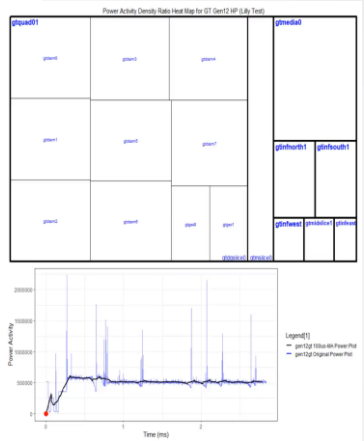
3DMark GFXBench Geekbench AnTuTu

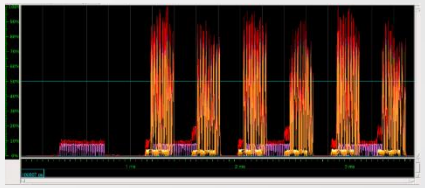
GFXBench 4.0, Car Chase, Kishonti

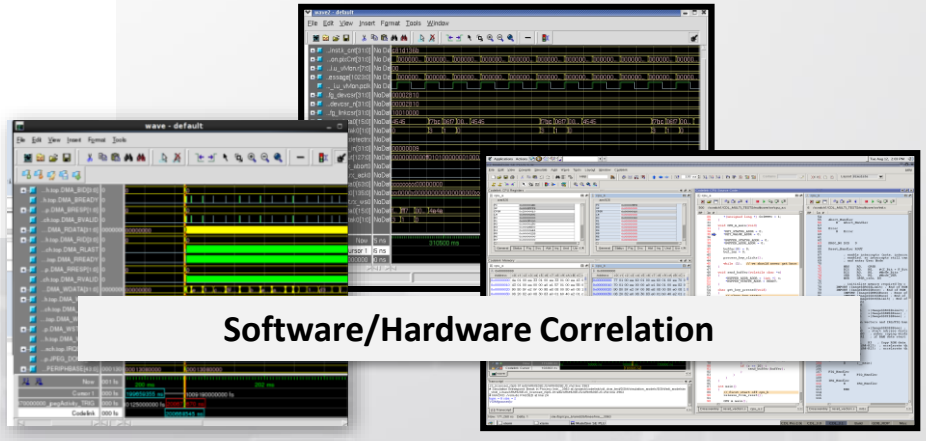


Veloce Strato

Emulation identifies power peaks running real workload benchmarks



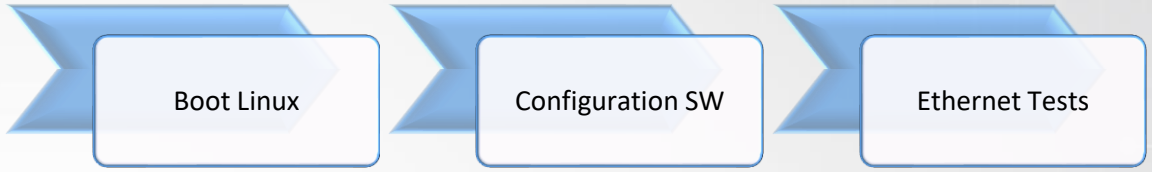


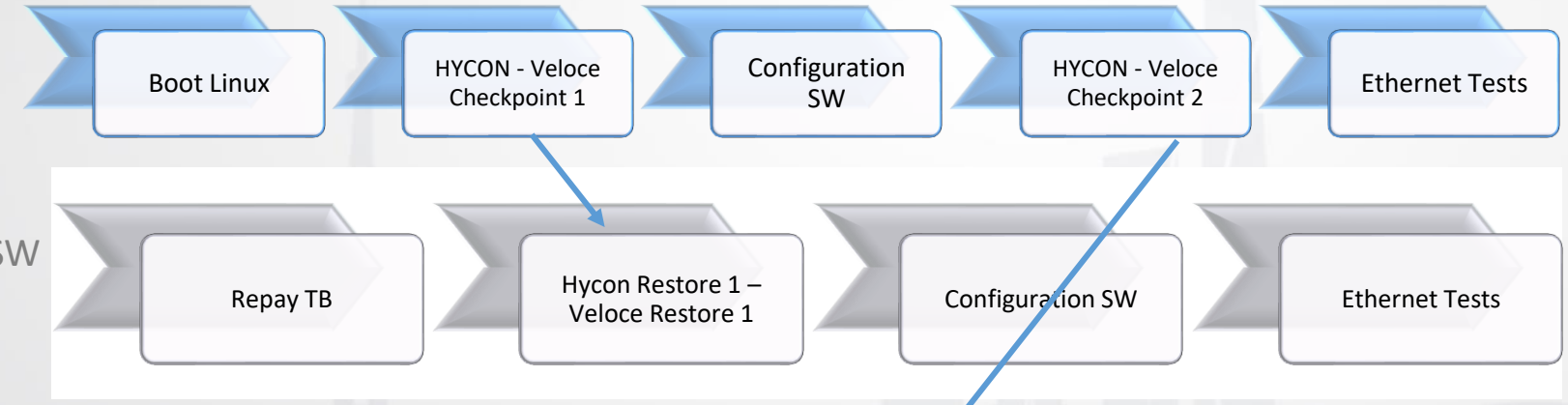


Software/Hardware Correlation

Case Study #2: Networking –
Leveraging Veloce HYCON checkpoint to increase IP verification efficiency

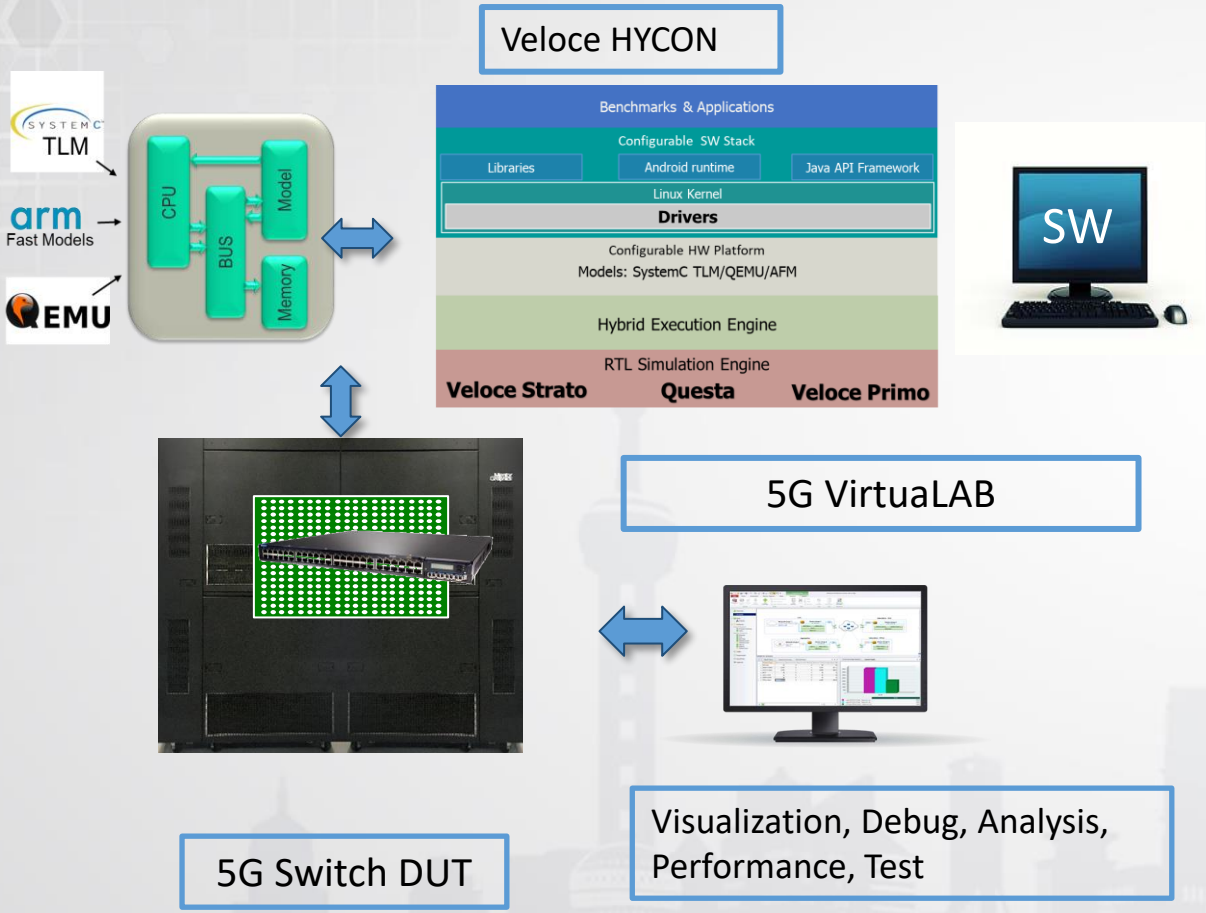
Goals:
1. Looking to save boot and configuration time
2. Validate SW operating correctly for various Ethernet Traffic test scenarios





HYCON Checkpoint
- ❑ Boot custom Linux kernel
- ❑ Checkpoint 1
- ❑ Load Configuration SW
  - ~ 2.5 hours running on Virtualized CPU
- ❑ Checkpoint 2
- ❑ Execute Ethernet traffic test(s)

Case Study #3:
SW-enabled system design with Veloce HYCON and Veloce VirtuaLab 5G



- IP-Subsystem verification
  - SW driver integration, software development and debug
- SoC Validation
  - Veloce HYCON for configuration of the DUT
  - Veloce HYCON running benchmarks
  - VirtuaLab 5G Control User Synchronization Management (CUSM)
  - Real life O-RAN workloads verified HW and SW performance
- Performance analysis w/RFRA
  - Measure latency, BW, utilization
    - Capture point to point & end to end

Value: Customer was allowed to create a pre-silicon verification environment of their full SoC for the first time

Summary

Summary: Veloce HYCON SW-driven verification and validation

- **Enabling a software-driven design methodology**
- **Provides a reference SW and HW platform on day 1**
- **Applications and benchmarks optimize HW and SW together**
- **Delivers on the promise of "Shift Left"**
  - Enables users to produce full-system power estimates and optimizations pre-silicon in the context of real application
  - Gives users the ability to execute and analyze full-system performance benchmarks pre-silicon
- **Bridge the discontinuity between different levels of abstraction**
  Pre-RTL, IP integration, SoC validation

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