UVM based configurable FSM model for System level verification of DDR5 DIMM High end Server Chipset

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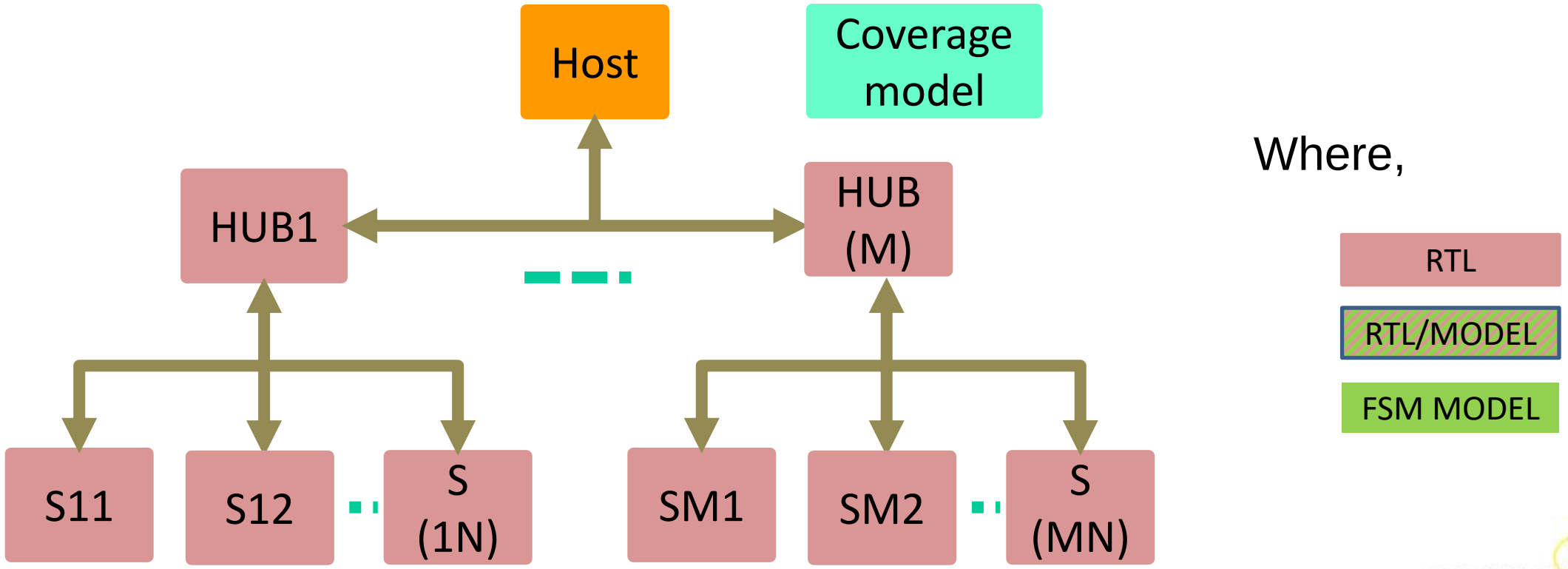
Problem Statement/Introduction

- In a **Server MxN DDR5 DIMM** configuration system, the data from host and DDR5 controller has been transmitted to low-speed interface protocols like **SPD HUB(M) , Temperature sensors(N)** and **high speed DDR5 RCD** devices which runs at **2.8GHz** respectively. Listed down the below problems with previous method,
  - To make the design more robust when targeted slave device responding to Host and while other M-1xN-1 devices are Idle.
  - To configure non-targeted slave devices with illegal state or to create protocol violation while host is targeting any of the M or N devices.
  - To verify the design behaviour with negative scenarios and protocol breaking Illegal scenarios to target device.
  - To verify corner case scenarios of slave devices behind the HUB
  - Time to market

Proposed Methodology/Advantages

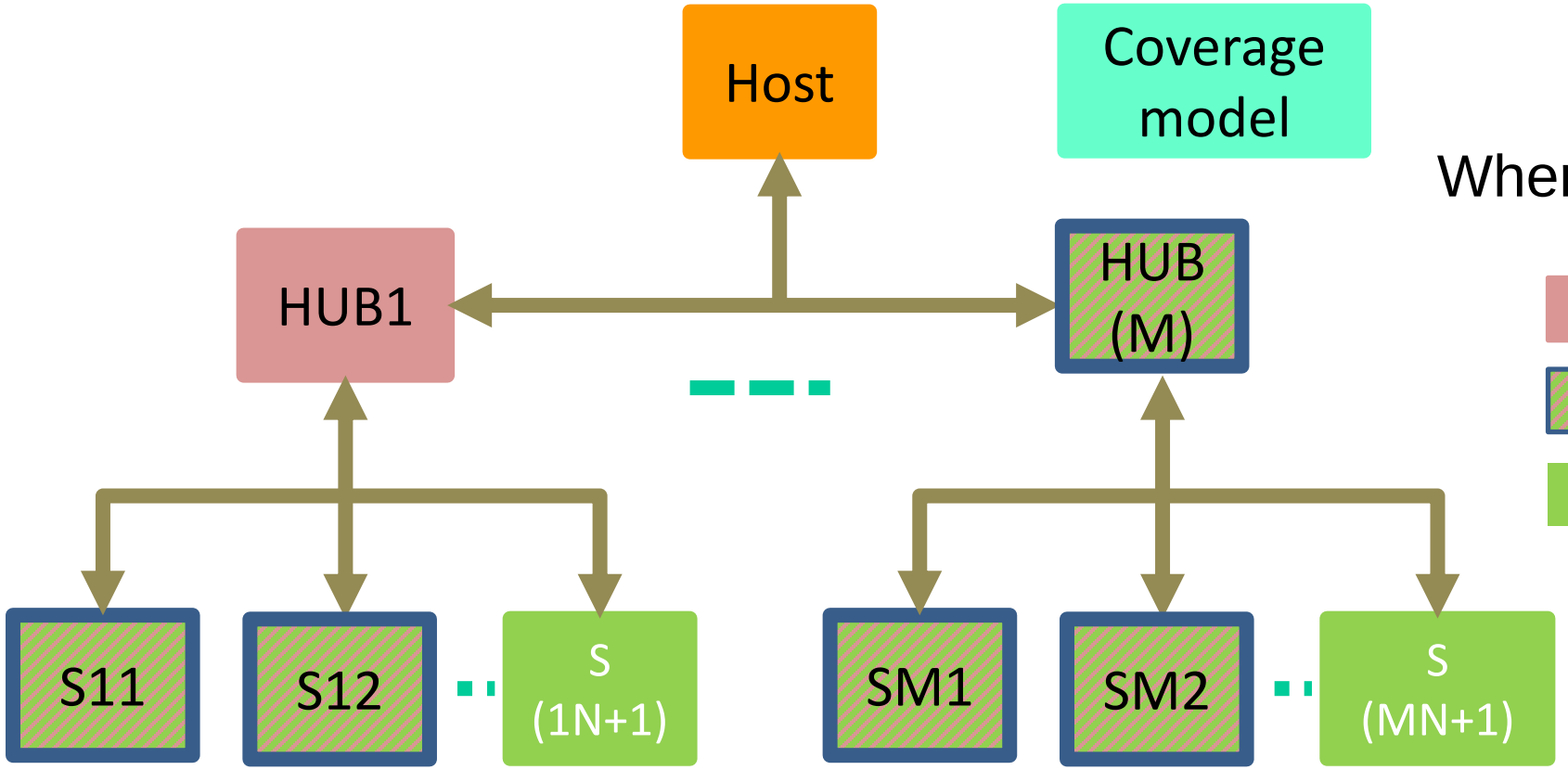
- To make the MxN DIMM system with more robustness, we have proposed and developed **UVM based configurable FSM model** [1][2][3] as per **JEDEC DDR5 standard**. By configuring with device ID, the model can be re-used as N slave devices behind the HUB as well as M instances of HUB.
- The developed FSM model has capability of,
  - Interrupt Arbitration with priority level.(False creation of interrupts)
  - RTL design behaviour/functional violations.
  - Timing violations with worse/best setup and hold time.
  - Protocol violation checks, by introducing intentional error [2].
  - Negative or illegal scenarios, error injection scenarios.
  - Selective M HUB or N Slave model can be configured with non-target mode on the fly irrespective of the entire system works on different mode.

Implementation Details/Diagram - 1

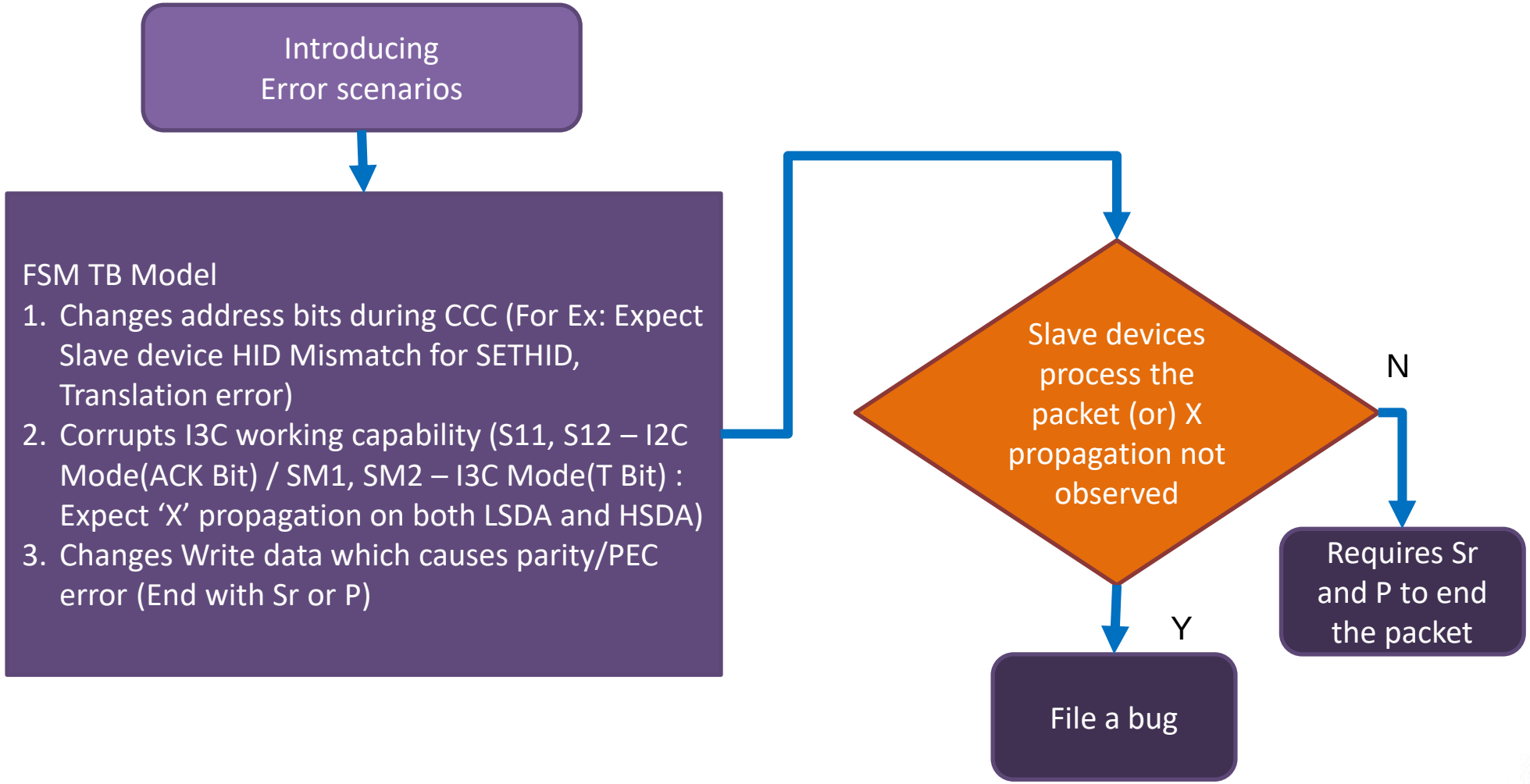


Implementation Details/Diagram - 2

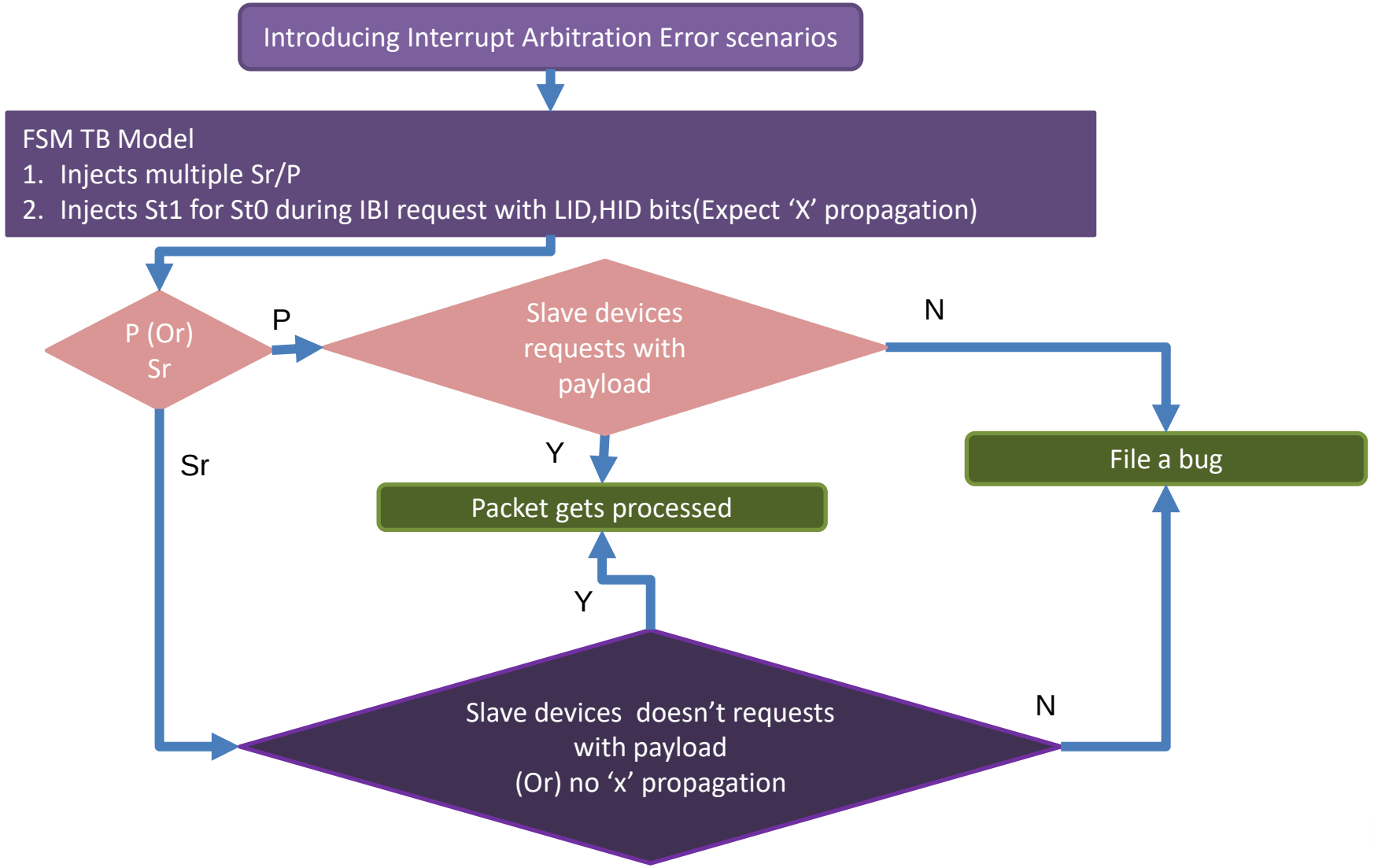
Proposed DDR5 DIMM System TB Architecture



Implementation Details/Flow Chart - 1

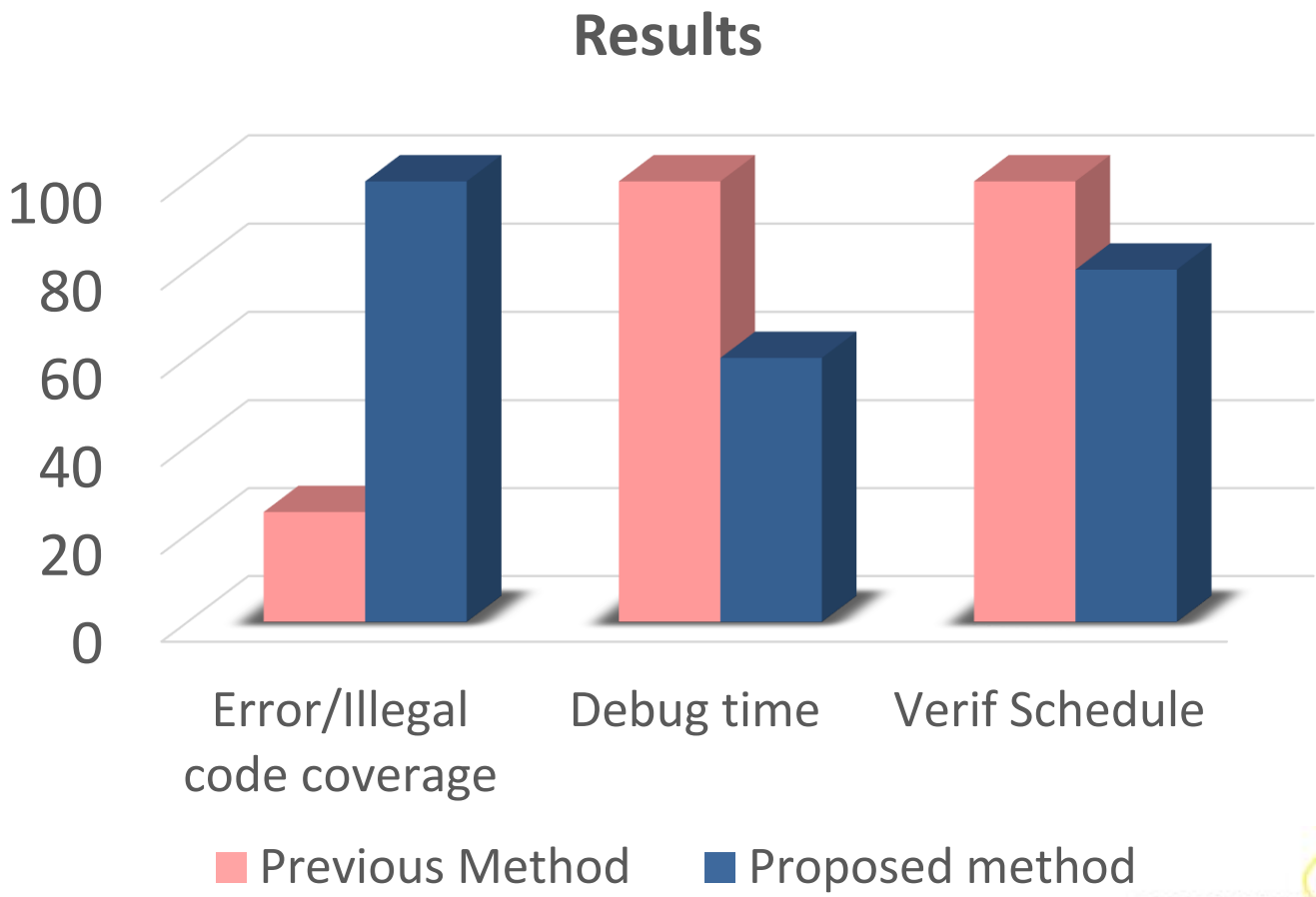


Implementation Details/Flow Chart - 2



Results Table

1. Achieved 100% code and functional coverage on negative and illegal cases, protocol violations.
2. Achieved 40% of better RTL design debug time with model-based approach at system level verification.
3. Saved 20% of Verification schedule with proposed approach.



Conclusion

A UVM based configurable FSM model as per JEDEC DDR5 standard has been proposed to reuse as M instances of HUB and N instances of Slave devices to achieve all error and illegal scenarios. The experimental results show that FSM model has helped in better code coverage on error/ illegal scenarios, efficient debug time and better saving on verification schedule Comparatively.

Questions