UVM based configurable FSM model for System level verification of DDR5 DIMM High end Server Chipset

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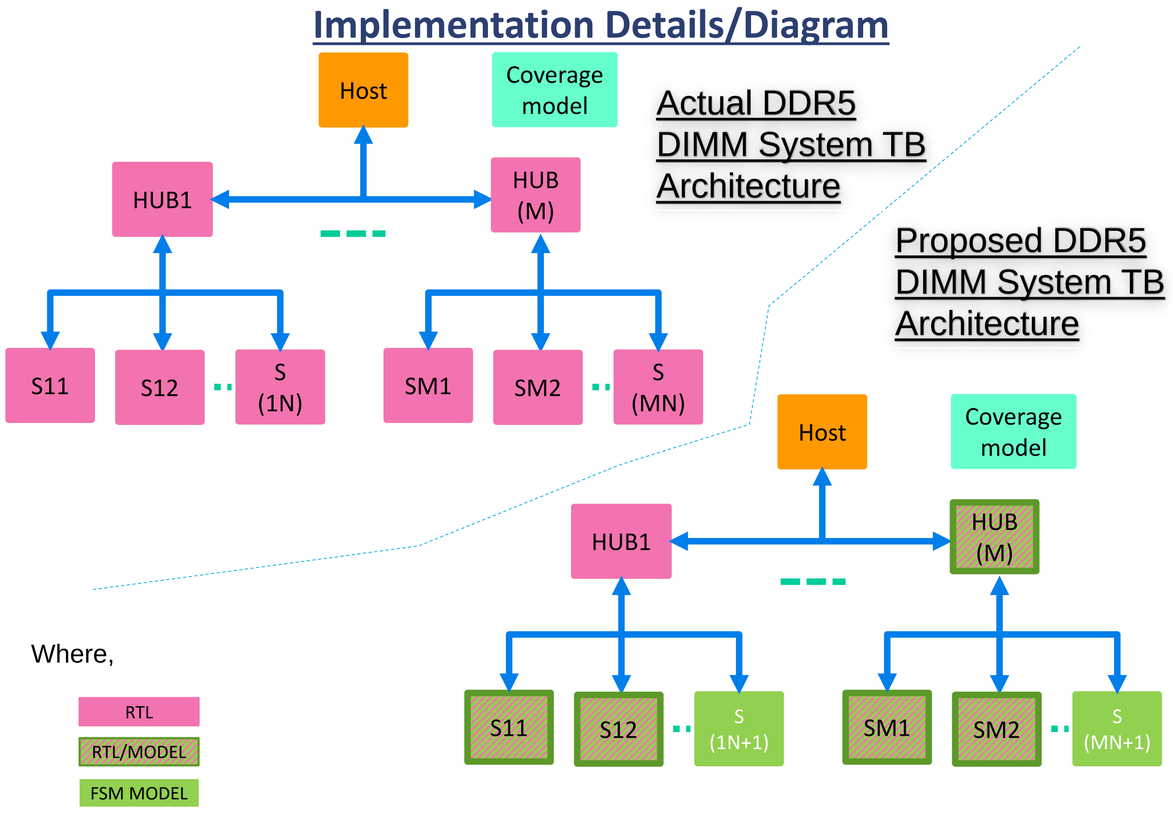
Problem Statement/Introduction

- In a **Server DDR5 DIMM** configuration system, the data from host and DDR5 controller has been transmitted to low-speed interface protocols and high speed DDR5 devices respectively.
- The overall system comprises of **MxN DDR5 DIMM devices** and should be capable of handling the traffic between high speed DDR5 device which runs at 2.8GHz and low speed modules like SPD HUB and Temperature sensors.
- In the MxN DIMM system, host controller is responsible to address all the slave devices behind HUBs and should handle the traffic across all the MxN devices. A single unit of DDR5 DIMM consists of **SPD HUB(M)**, which is followed by **RCD, Temperature Sensors, and other devices (N)**.
- During DDR5 DIMM system level functional verification of a design, we have identified the below problems and it was more challenging for us to create such scenarios as well,
  - To make the design more robust when targeted slave device responding to Host and while other M-1xN-1 devices are Idle.
  - To configure non-targeted slave devices with illegal state or to create protocol violation while host is targeting any of the M or N devices.
  - To verify the design behaviour with negative scenarios and protocol breaking Illegal scenarios to target device.
  - To verify corner case scenarios of slave devices behind the HUB
  - Time to market

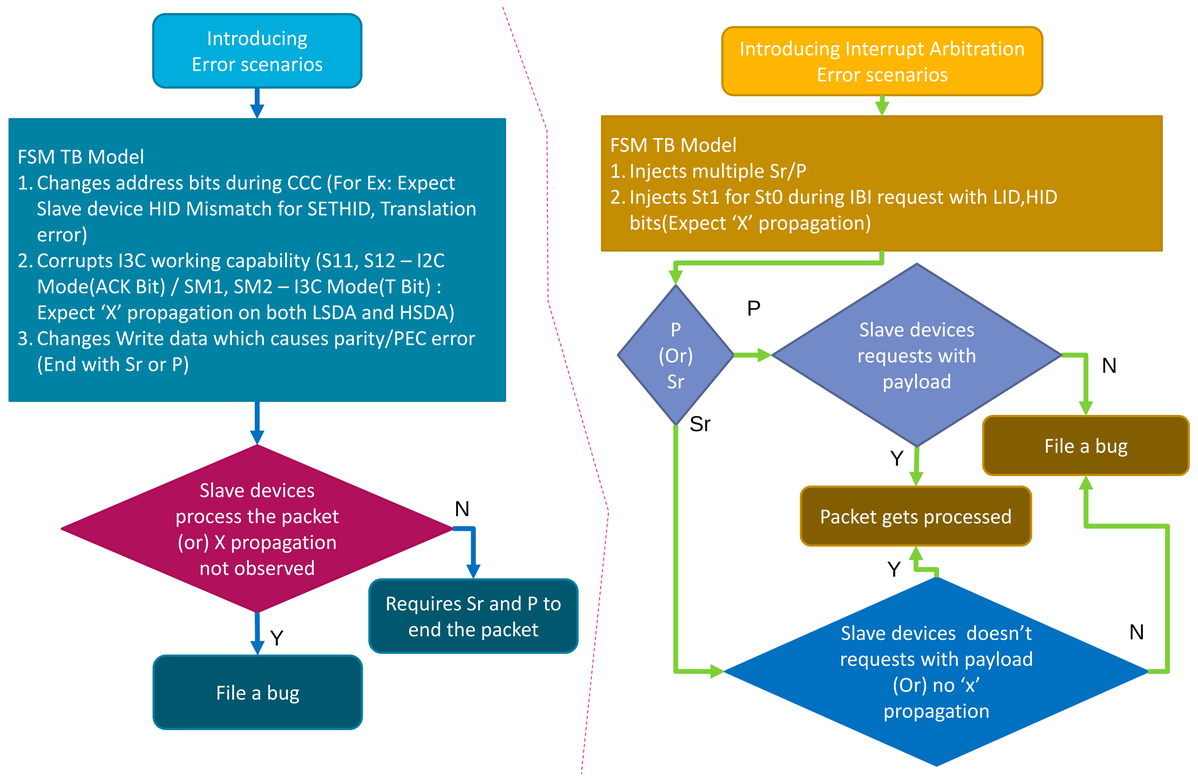
Proposed Methodology/Advantages

- To make the MxN DIMM system with more robustness, we have proposed and developed **UVM based configurable FSM model** [1][2][3] as per **JEDEC DDR5 standard**. By configuring with device ID, the model can be re-used as N slave devices behind the HUB as well as M instances of HUB.
- The **model has incorporated with the functionality of HUB and slave devices**, i.e. the model has developed with a well-defined FSM, such a way that it should handle the common functionality across the MxN devices and also should act as a standalone device for any of the MxN devices.
- The developed FSM model has capability of,
  - Generating and handling Interrupt Arbitration with priority level between MxN devices in the system.
    - Handling of False creation of interrupts from non-target devices
  - Model can be configured to create RTL design behaviour/functional violations.
  - Able to configure and achieve MxN devices with worse and best setup, hold time, by assuming competitor design behaviour.
  - Able to inject error and comprises of error detection and correction.
  - Protocol violation checks, by introducing intentional error [2].
  - Model is flexible in creating Negative or illegal scenarios for any target and non-target devices.
  - Selective M HUB or N Slave model can be configured with non-target mode on the fly irrespective of the entire system works on different mode.

Implementation Details/Diagram



Implementation Details/Flow Chart



Results Table

1. Achieved 100% code and functional coverage on negative and illegal cases, protocol violations.
2. Achieved 40% of better RTL design debug time with model-based approach at system level verification.
3. Saved 20% of Verification schedule with proposed approach.

Conclusion

A UVM based configurable FSM model as per JEDEC DDR5 standard has been proposed to reuse as M instances of HUB and N instances of Slave devices to achieve all error and illegal scenarios. The experimental results show that FSM model has helped in better code coverage on error/ illegal scenarios, efficient debug time and better saving on verification schedule Comparatively.

REFERENCES

[1] C. Spear, "System Verilog for Verification, A Guide to Learning the Testbench Language Features," Springer, 2008G.

[2] "System Verilog 3.1a Language Reference Manual", Accellera, 2004

[3] "UVM 1.2 User guide", Accellera System Initiative, 2015.

[4] "UVM 1.2 Class Reference", Accellera System Initiative, 2014.