In a server DDR5 DIMM configuration system, the data from host and DDR5 controller has been transmitted to low-speed interface protocols and high-speed DDR5 devices respectively.

The overall system comprises of MxN DDR5 DIMM devices and should be capable of handling the traffic between high speed DDR5 device which runs at 2.8GHz and low speed modules like SPD Hub and Temperature sensors.

In the MxN DDR5 system, host controller is responsible to address all the slave devices behind HUBs and should handle the traffic across all the MxN devices. A single unit of DDR5 DIMM consists of SPD Hub(M), which is followed by RCD, Temperature Sensors, and other devices (N).

During DDR5 DIMM system level functional verification of a design, we have identified the below problems and it was more challenging for us to create such scenarios as well,

- To make the design more robust when targeted slave device responding to Host and while other M-1xN-1 devices are idle.
- To configure non-targeted slave devices with illegal state or to create protocol violation while host is targeting any of the M or N devices.
- To verify the design behaviours with negative scenarios and protocol breaking illegal scenarios to target device.
- To verify corner case scenarios of slave devices behind the HUB
- Time to market

**Proposed Methodology/Advantages**

- To make the MxN DDR5 system with more robustness, we have proposed and developed UVM based configurable FSM model [1][2][3] as per JEDEC DDR5 standard. By configuring with device ID, the model can be re-used as N slave devices behind the HUB as well as M instances of HUB.
- The model has incorporated with the functionality of HUB and slave devices, i.e. the model has developed with a well-defined FSM, such a way that it should handle the common functionality across the MxN devices and also should act as a standalone device for any of the MxN devices.
- The developed FSM model has capability of,
  - Generating and handling Interrupt Arbitration with priority level between Mn devices in the system.
  - Handling of False creation of interrupts from non-target devices
  - Model can be configured to create RTL design behaviour/functional violations.
  - Able to configure and achieve Mn devices with worse and best setup, hold time, by assuming competitor design behaviour.
  - Able to inject error and comprises of error detection and correction.
  - Protocol violation checks, by introducing intentional error [2].
  - Model is flexible in creating Negative or illegal scenarios for any target and non-target devices.
  - Selective M HUB or N Slave model can be configured with non-target mode on the fly irrespective of the entire system works on different mode.

**Implementation Details/Diagram**

![Diagram of DDR5 DIMM System TB Architecture](image)

**Implementation Details/Flow Chart**

![Flow Chart of FSM TB Model](image)

**Results Table**

![Graph of Error/Illegal code coverage, Debug time, Verif Schedule](image)

**Conclusion**

A UVM based configurable FSM model as per JEDEC DDR5 standard has been proposed to reuse as M instances of HUB and N instances of Slave devices to achieve all error and illegal scenarios. The experimental results show that FSM model has helped in better code coverage on error/illegal scenarios, efficient debug time and better saving on verification schedule Comparatively.

**References**


© Accellera Systems Initiative