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UVM Acceleration using Hardware Emulator at Pre-silicon Stage

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Agenda

- Motivation
- Simulation Profiling
- Dual Domain Framework
- Simulation Acceleration Flow
- OOMR Signal Handling

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Motivation

- Increase of SOC complexity
- The verification TAT needs to be shorted.
- Verification Environment: UVM
  - has reusability, scalability and interoperability
  - But SLOW
- Target Goal
  - SPEED
  - Automation
  - Current verification vectors should be reused.

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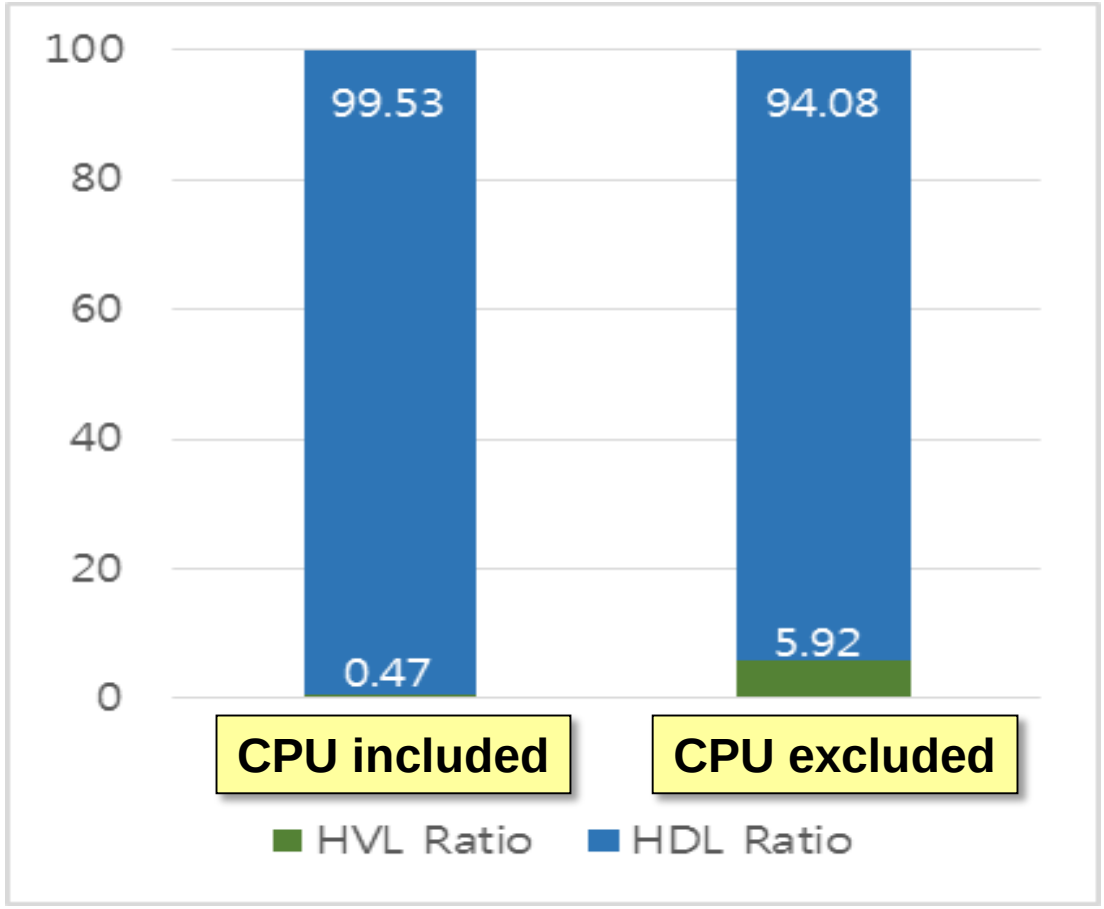
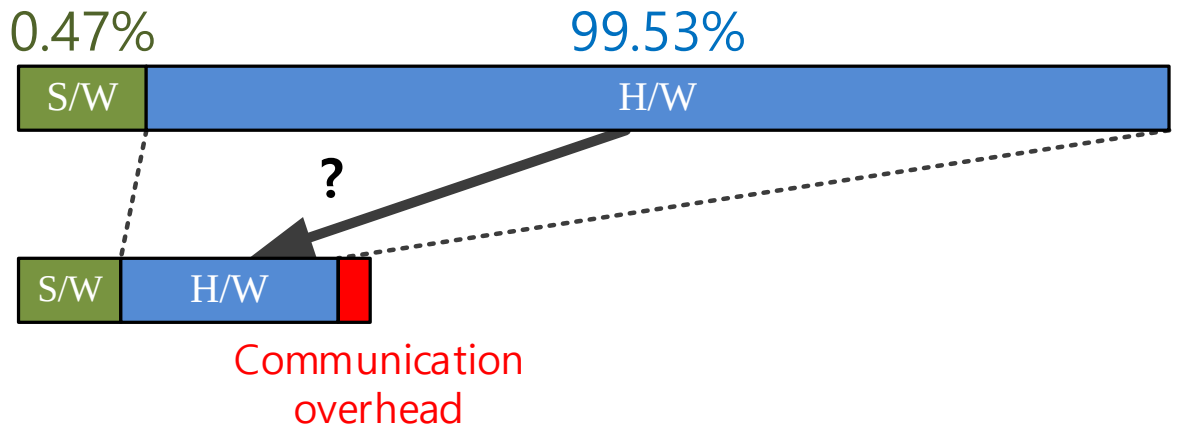
Simulation Profiling and Acceleration Estimation

Signal toggle distribution comparison



Acceleration time estimation



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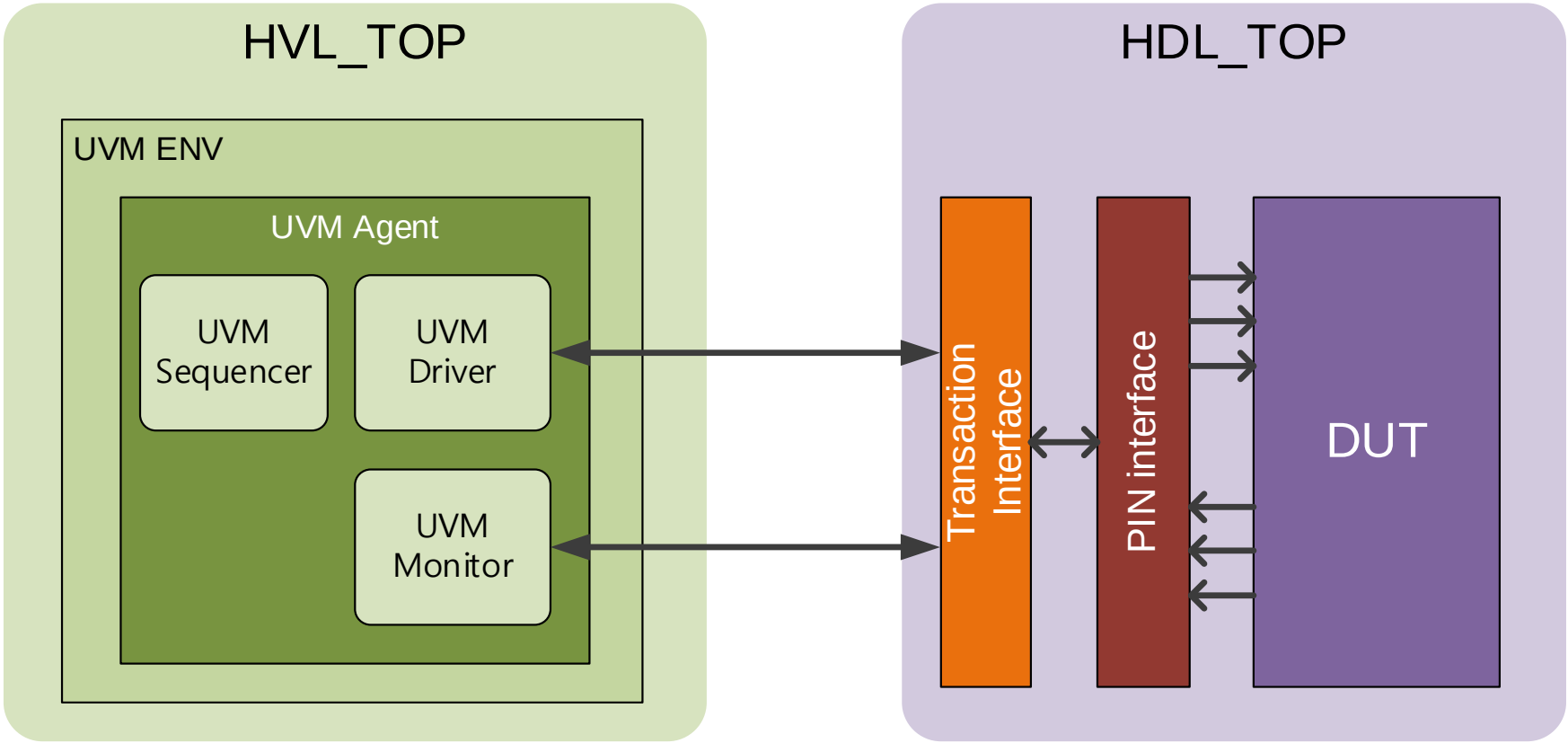
Dual Domain Framework



S. Hemant and H. Schoot, “Bringing Verification and Validation under One Umbrella,” *Verification Academy,* 02 2013.

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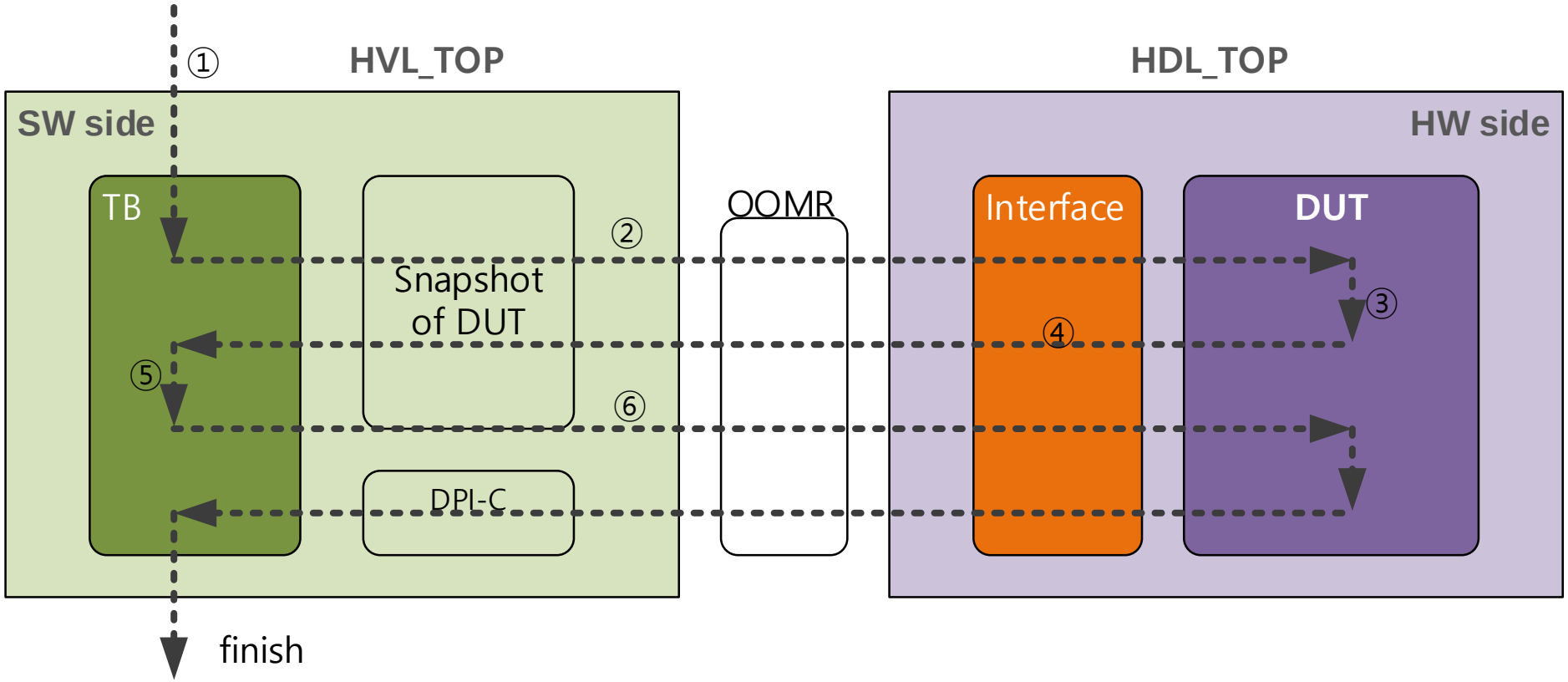
Running flow of UVM Acceleration

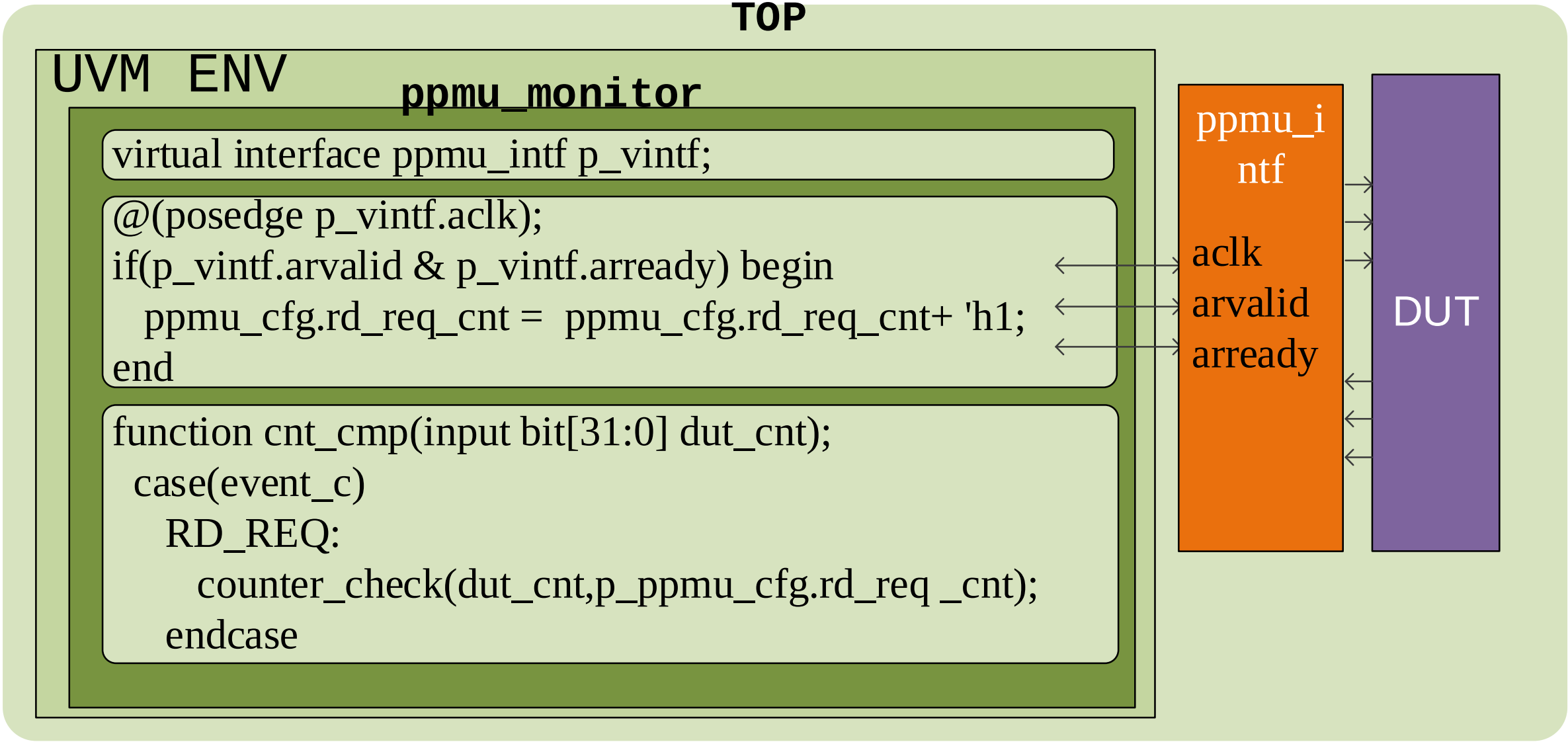


OOMR: Out-Of-Module-Reference a.k.a XMR(Cross Module Reference)

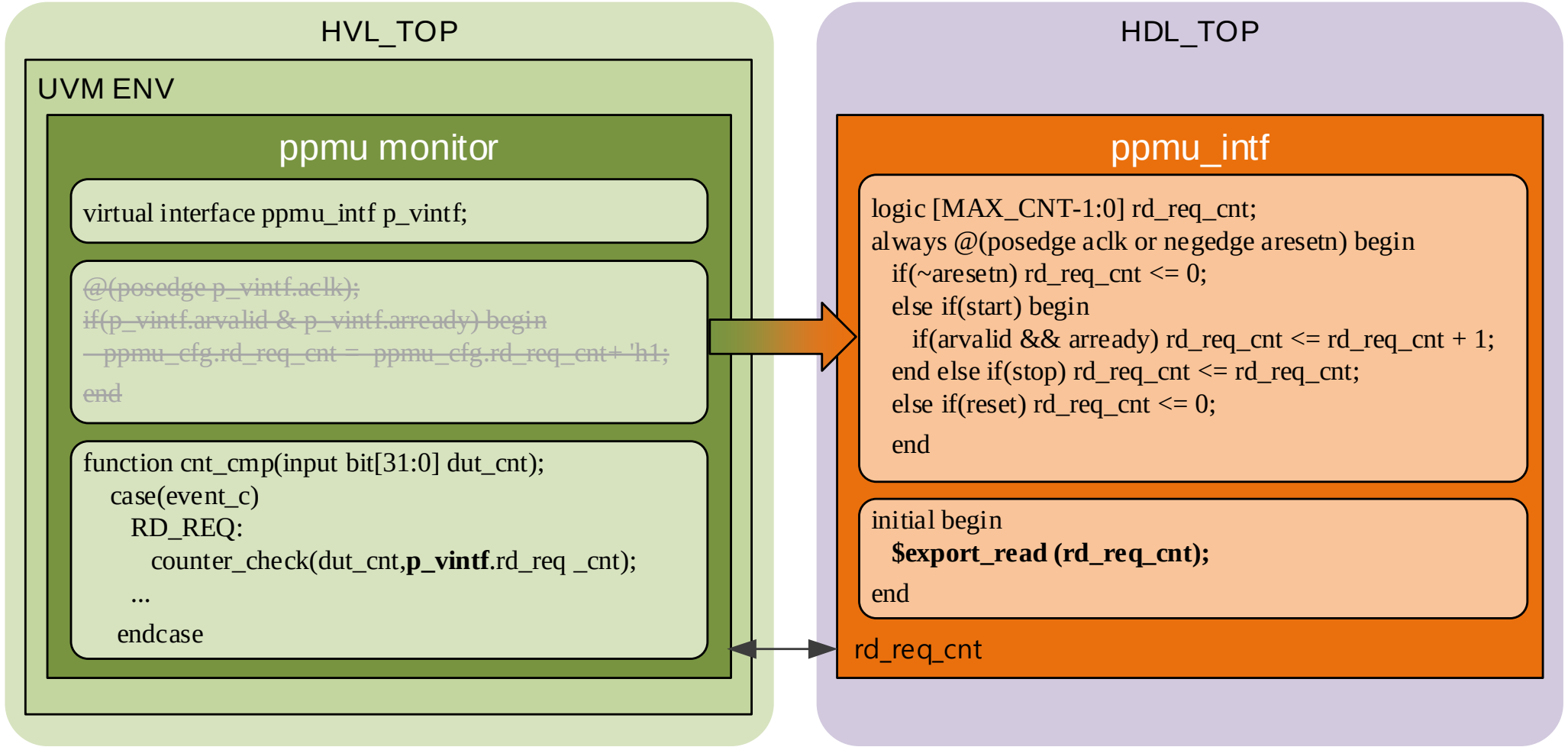
UVM Acceleration Obstacles

- Communication overhead between HVL and HDL
  - It can cause severe performance degradation.
- Hardware access signals that are collected incompletely
  - This problem can cause below iteration again and again.
    - Waveform generation
    - Problem shooting
    - Design recompilation

Example of UVM environment



Example of UVMA environment



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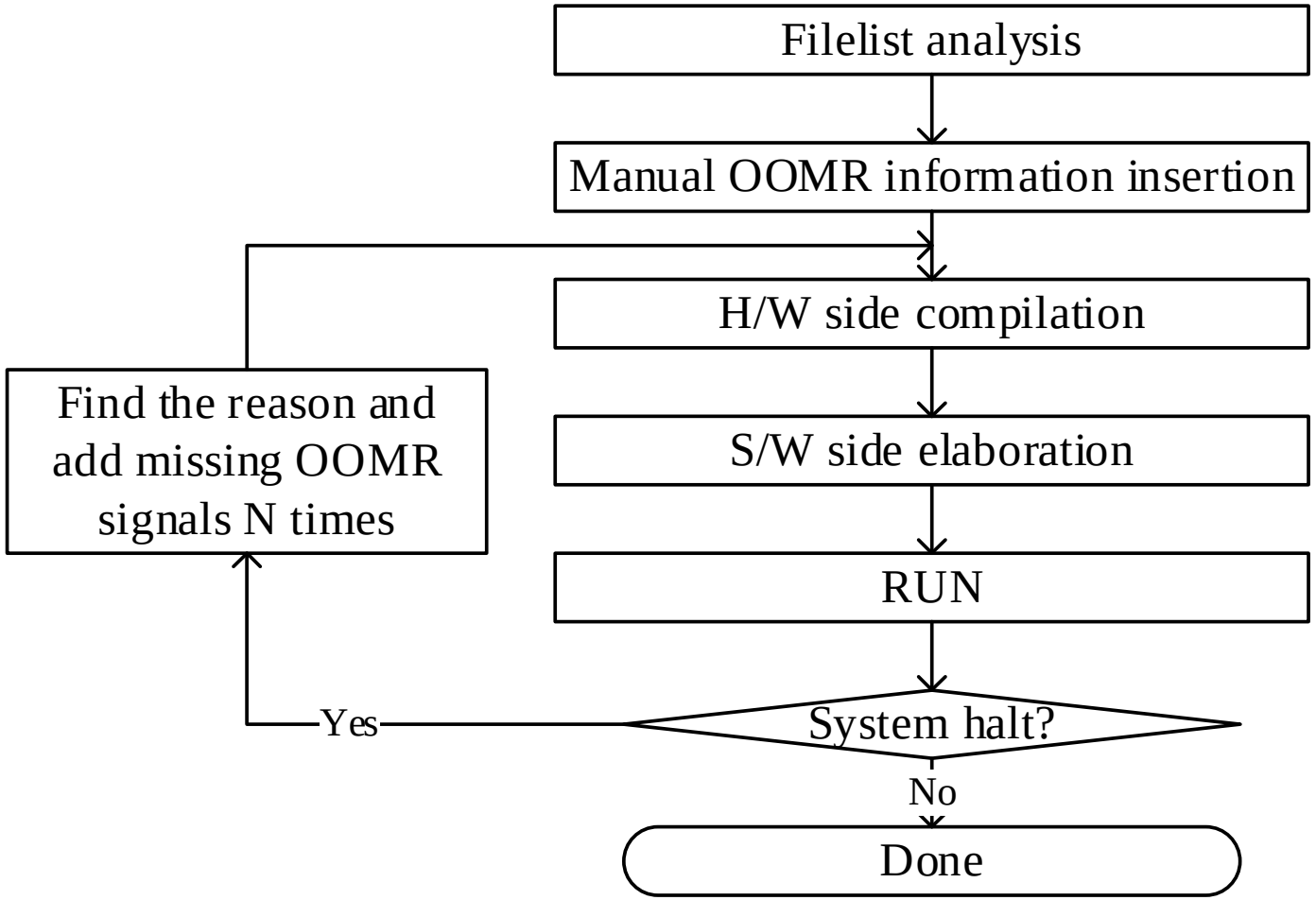
Current Generation Flow



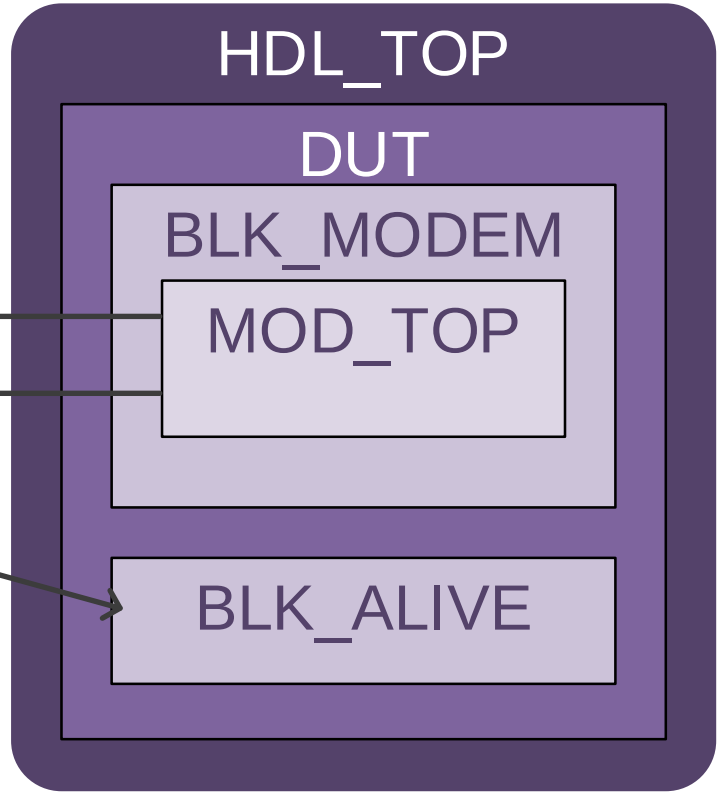
Frozen test vector example

HVL_TOP

```
fork
begin
    …
    wait(top.dut.BLK_MODEM.MOD_TOP.oPwrReq);
    wait(top.dut.BLK_MODEM.MOD_TOP.oPwrAck);
    …
    force top.dut.BLK_ALIVE.oPwrUp = 1'b1;
    …
end
```

missed signals

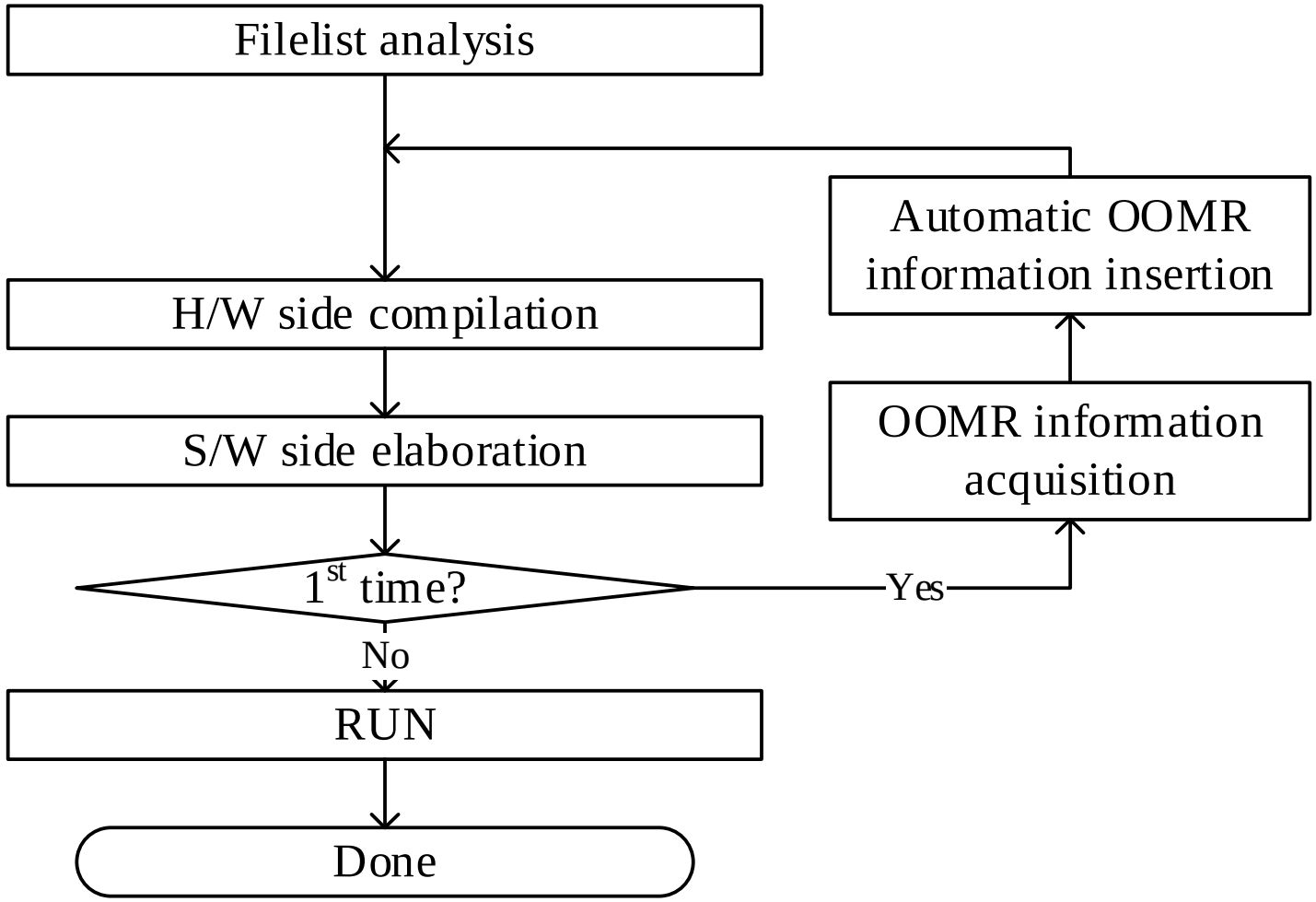
wait forever!



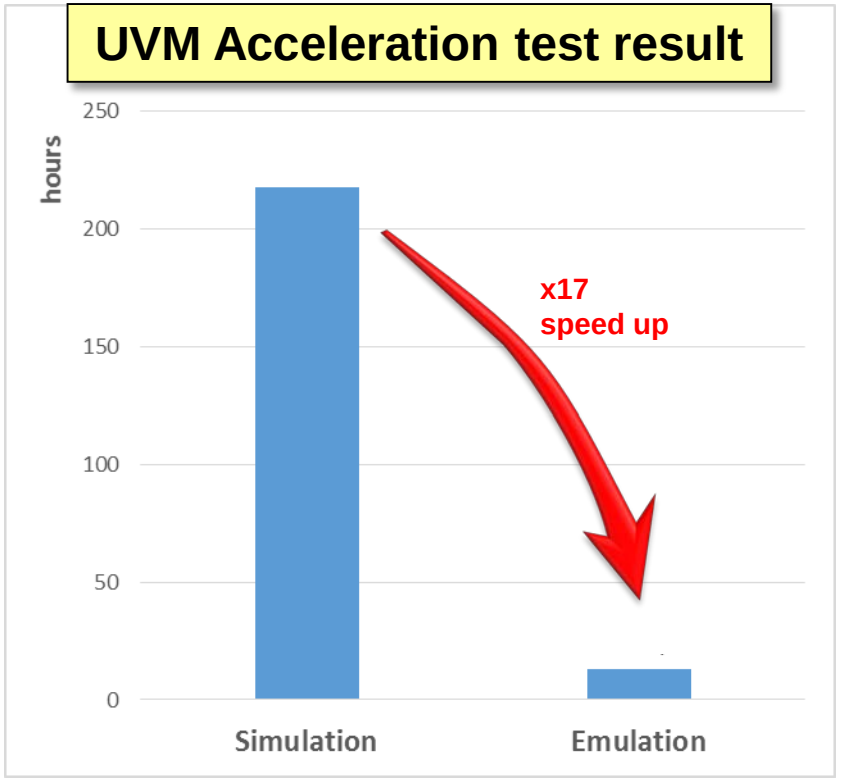
OOMR signal list

```
…
signal_export( top.dut.BLK_MODEM.MOD_TOP.oPwrReq);
…
```

Proposed Generation Flow



Result of UVM Acceleration



Normal vectors				Power aware vectors			
Test Vectors	Normalized Simulation Time	Normalized Emulation Time	Speed-up	Test Vectors	Normalized Simulation Time	Normalized Emulation Time	Speed-up
121	17	1	x17	16	21	1	x21

Other Considerations

- Unsynthesizable library handling
  - Use simulation model in the HVL side
- Power aware emulation
  - UPF information for stubbed out RTL block should be handled
- DFS(Dynamic Frequency Scaling) emulation
  - Use 1 clock instance, do not populate all clock instances

Summary

- To make UVM Acceleration environment,
  - Choose UVMA-friendly test vectors by simulation profiling
  - Split one UVM environment into 2 domains
    - HVL and HDL
  - Move clock related codes of HVL to HDL for performance
  - Add OOMR information during UVMA environment compilation

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Q & A