2019 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

Using Modal Analysis to Increase Clock Domain Crossing (CDC) Analysis Efficiency and Accuracy

Kurt Takara, Mentor Graphics, A Siemens Business
Gargi Sharma, Mentor Graphics, A Siemens Business
Ajay Thadhlani, Barefoot Networks,
Bhrugurajsinh Chudasama, Barefoot Networks

Mentor® A Siemens Business

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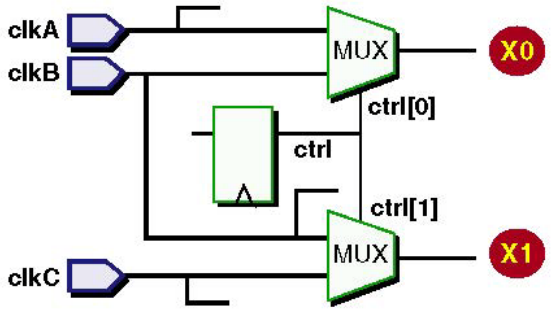
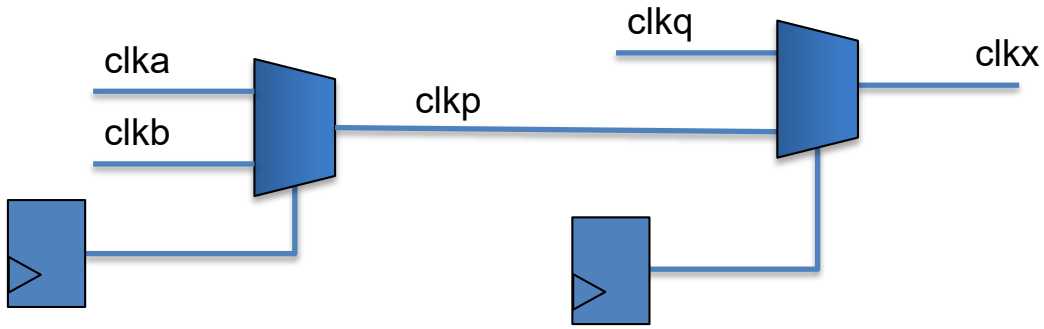
Clock Muxing Pessimism



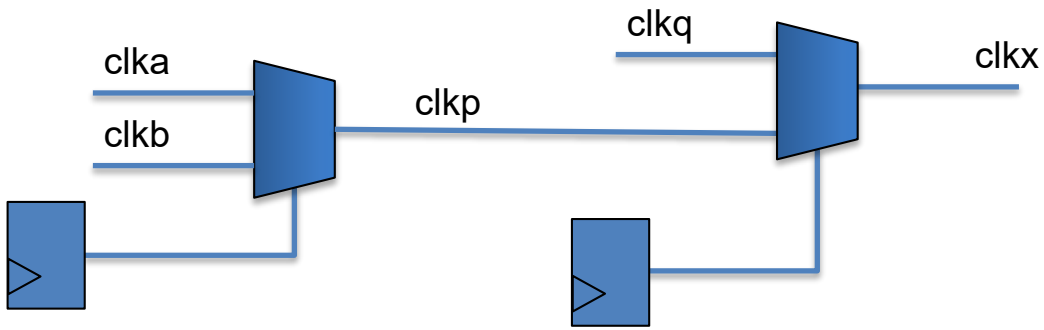
- Assume clkA, clkB, clkC are asynchronous
- Pessimistically, assume the mux ctrl signal will dynamically switch
  - Mux outputs cannot be considered synchronous to either inputs
  - Mux outputs are considered new asynchronous clock groups and
- Pessimistically, five clock groups identified: clkA, clkB, clkC, X0, X1.

Options for Controlling Clock Muxing



- Configuration options
  1. Multiple SDC files to specify unique configurations
  2. Infer new asynchronous clock domains at mux outputs
     - Pessimistic approach appropriate for dynamic clock switching
  3. Multi-mode analysis
     - Single-configuration modal method
     - Multi-configuration modal method

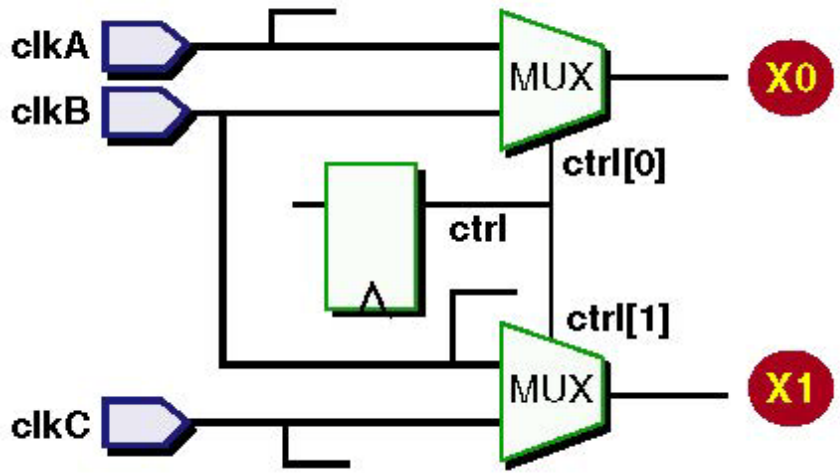
Single-Configuration Modal Method



clkx: clka, clkb, clkq
clkx path example:
To/From clka crossings:
- Report clkb crossings violations
- Report clkq crossings violations

- For single-configuration modal methods, the mux outputs will be associated with multiple clocks
- Optimistically consider one crossing violation per CDC path => missed paths
- Pessimistically consider multiple crossings per CDC path => noisy

Multi-Configuration Modal Method



cdc_mode_0: X0 = clkA and X1 = clkB
ctrl = 2'b00
cdc_mode_1: X0 = clkA and X1 = clkC
ctrl = 2'b01
cdc_mode_2: X0 = clkB and X1 = clkB
ctrl = 2'b10
cdc_mode_3: X0 = clkB and X1 = clkC
ctrl = 2'b11

- For static clock mode scenarios, the mux outputs will be associated with only one of the input clocks at any given configuration
- CDC analysis considers legal operational modes

Modal Analysis Methods

Single-configuration Method

- Run once
- Better performance
- Configure for optimism or pessimism
  - Will not consider legal modes for clock mux interdependence
  - Optimistic mode will miss CDC scenarios
  - Pessimistic mode does not scale to large designs

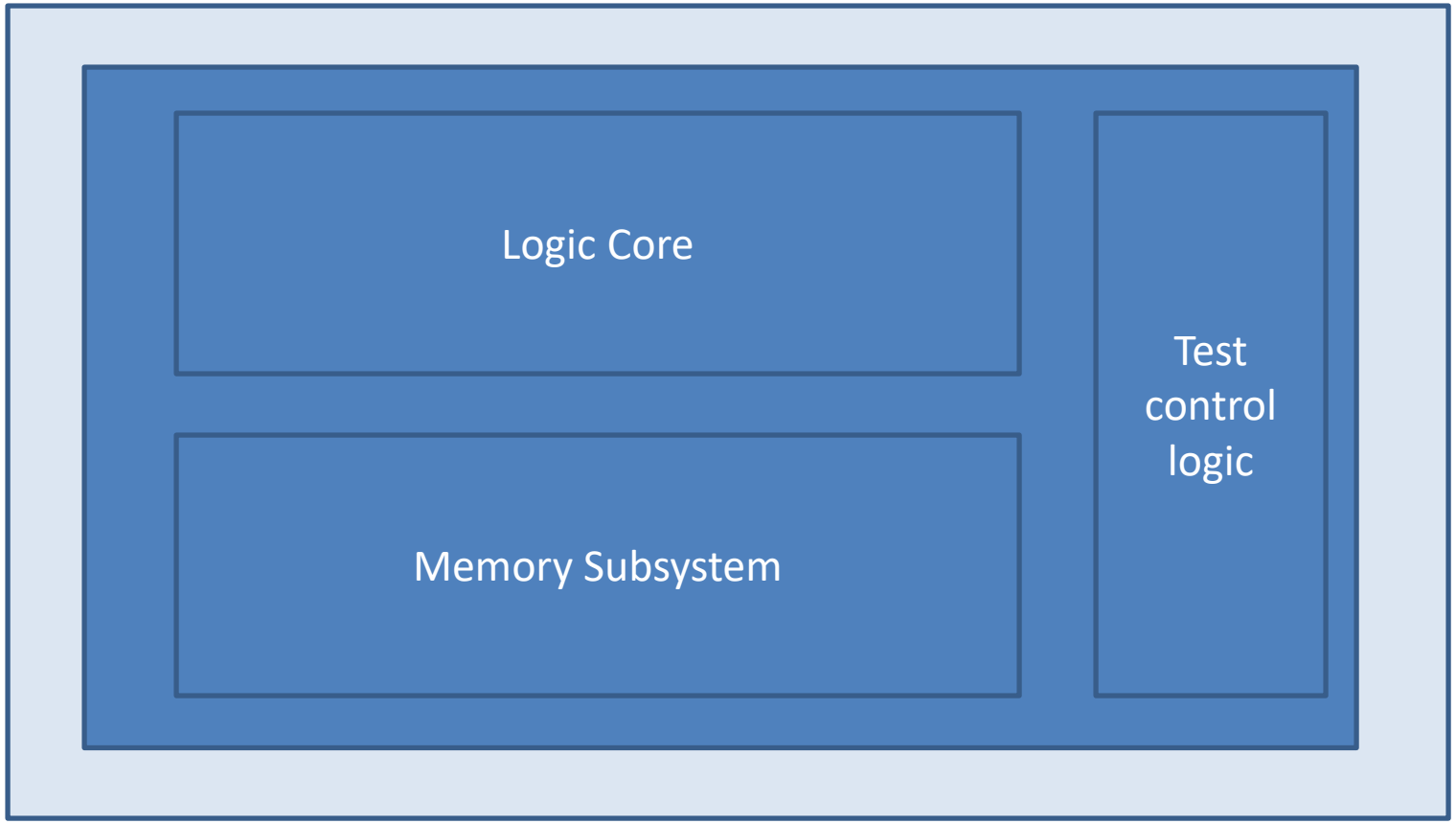
Multiple-configuration method

- Run multiple times
- Parallelize for performance
- Higher accuracy
  - Considers legal modes only for clock mux interdependence
  - Aggregation of results enables compare/contrast between modes
  - Every path can be correlated to specific operational modes

Modal Analysis Methodology

- Phase 1: Design setup
  - Automatically detect clock configuration registers
  - Calculate design configuration permutations & combinations
  - Identify all possible operational modes
  - Designers determine legal/illegal operational configurations
- Phase 2: CDC analysis
  - Runs CDC analysis on all legal operational modes
  - Aggregates mode-specific CDC results
- Phase 3: CDC Debug
  - Designers review aggregated results, then compare and contrast the good and bad synchronization structures for CDC paths across different operational modes

Example Design



Example Design

- Primary clocks
  - 2 functional clocks
  - JTAG/MBIST clock
  - 2 SCAN clocks
  - 2 SCAN clock chain clocks
- Test four major modes
  - Functional
  - MBIST
  - Shift
  - Capture

Design Clock Configuration

- Initially, 182 asynchronous clock domains identified
  - 7 primary clocks
  - 175 muxed clocks
- Divided into 4 legal modes:

```
# Mission mode
cdc mode mode_0 -set *.blkDftCtrl.DFT__BIST_MODE_i.DFT_MRK_BUF.Z 1'b0 -set *.blkDftCtrl.DFT_SCAN_EN.Q 1'b0 -set  *.blkDftCtrl.dftScanCtrl.DFT__SCAN_MODE 1'b0
# Shift mode
cdc mode mode_1 -set *.blkDftCtrl.DFT__BIST_MODE_i.DFT_MRK_BUF.Z 1'b0 -set *.blkDftCtrl.DFT_SCAN_EN.Q 1'b1 -set  *.blkDftCtrl.dftScanCtrl.DFT__SCAN_MODE 1'b1
# Capture mode TDF
cdc mode mode_2 -set *.blkDftCtrl.DFT__BIST_MODE_i.DFT_MRK_BUF.Z 1'b0 -set *.blkDftCtrl.DFT_SCAN_EN.Q 1'b0 -set  *.blkDftCtrl.dftScanCtrl.DFT__SCAN_MODE 1'b1
# BIST mode
cdc mode mode_3 -set *.blkDftCtrl.DFT__BIST_MODE_i.DFT_MRK_BUF.Z 1'b1 -set *.blkDftCtrl.DFT_SCAN_EN.Q 1'b0 -set  *.blkDftCtrl.dftScanCtrl.DFT__SCAN_MODE 1'b0
```

Design Operation Modes

- Modal analysis resolved all muxed clocks

	Primary Clocks	Muxed Clocks	Total Clocks
Normal Analysis	7	175	182
Modal Analysis	7		182

Normal vs. Modal Comparison

	Correct CDC paths	Incorrect CDC paths	Total CDC paths
Normal CDC Analysis	4	12161	12165
Modal Analysis (aggregated results)	16	9860	9876
Modal Analysis (results per configuration)	4	2132-2944	2136-2948

	Run time
Normal CDC Analysis	8m 26s
Modal Analysis (aggregated results)	8m 43s

Benefits of Modal Analysis

- Captures the modal nature of the design
  - Legal operational modes become well-defined and explicitly specified
  - Avoids misinterpretation of the specification
- Reduces complexity and “pessimism”
  - Avoids a huge number of violations
  - Groups results per operational modes of the design.
  - Eliminates pessimistic results due to clock grouping pessimism
- Improves multi-mode analysis accuracy
  - Enables analysis of the correlation between design modes
  - Designers easily see commonalities and differences between modes
  - Designers quickly identify design issues and CDC bugs
    - Without the aggregation of results, designers would review the N mode results separately which would increase the review time by up to N times.

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Thank you!

- Questions?

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