Using Cadence and MathWorks Tools Together for Mixed-Signal Design and Verification

Graham Reith, MathWorks

Andrew Beckett, Cadence Design Systems









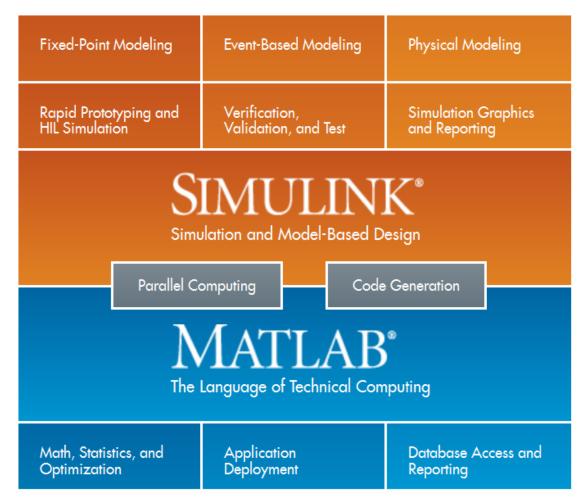
Agenda

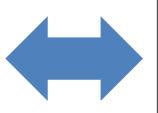
- Overview of MathWorks and Cadence Platform Integration
- Using MATLAB with Cadence Virtuoso ADE for Data Analysis and Visualization
 - Data Mining, Post-processing and Visualization
- System-level Modelling in Simulink
 - Modelling Analog and Digital Components
- An Integrated Design Flow for Mixed-signal Systems
- Including Transistor-level Models with Cadence Virtuoso AMS Designer
 - Co-simulation
 - Validation and Refinement of System-level Models
- Exporting Models from Simulink to Cadence
 - Behavioural Models and Testbenches for Mixed-signal Verification



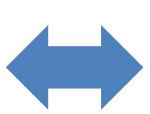


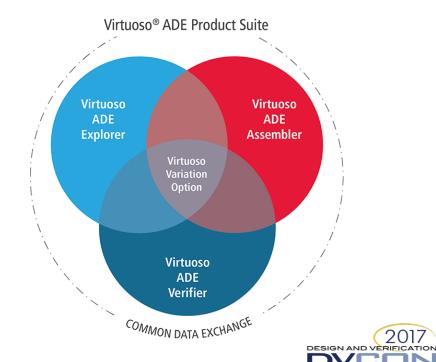
MathWorks and Cadence Platform Integration













Using MATLAB with Cadence Virtuoso ADE for Data Analysis and Visualization





New MATLAB Integration

- New MATLAB integration to Cadence® Virtuoso® ADE Explorer and Assembler
- Create circuit performance measurements using MATLAB
- All Virtuoso ADE Explorer and Assembler simulation data exposed to MATLAB
- High-level query interface enables powerful data mining and post-processing capability
- Interface with MATLAB
 - Open MATLAB interactively after simulation
 - Or create Virtuoso ADE output expressions to evaluate automatically at simulation run time



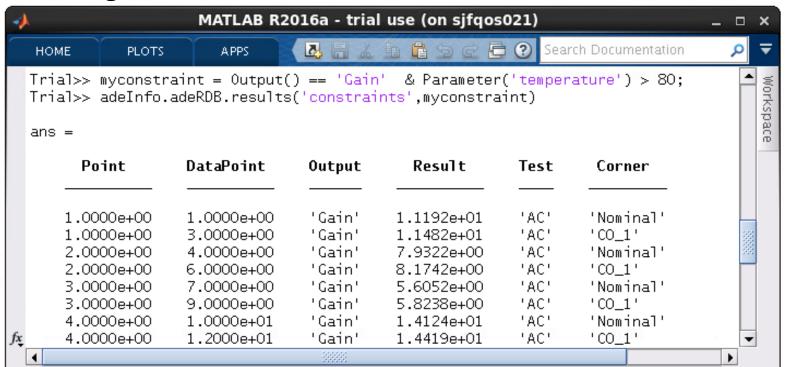


Using MATLAB with Virtuoso ADE Explorer and Assembler

- Open an interactive MATLAB session
 - Open MATLAB toolbar button



Query results using the Virtuoso ADE interface

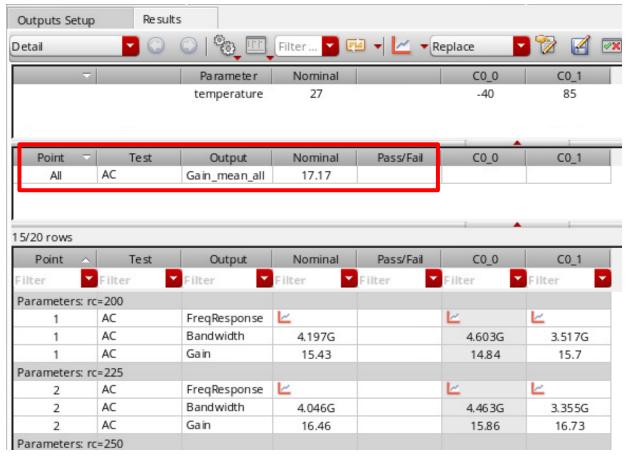






MATLAB Expression Results

 In this example, the MATLAB output computes the mean value of Gain across all sweep points and corners

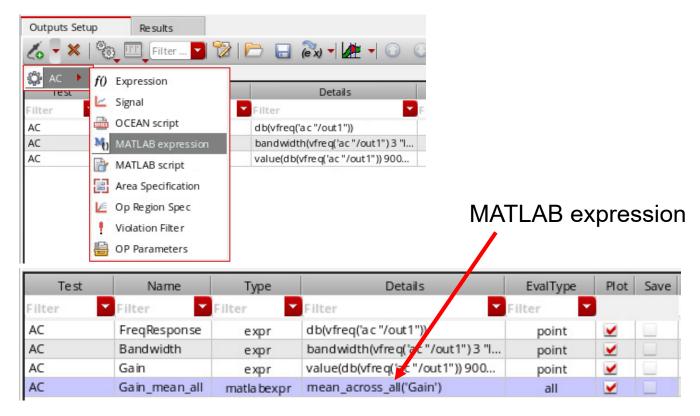






Create MATLAB Expression Outputs

- Outputs are evaluated automatically at run time
- Call custom or built-in MATLAB measurement functions
- Results are displayed in the Virtuoso ADE results table per point or across all points

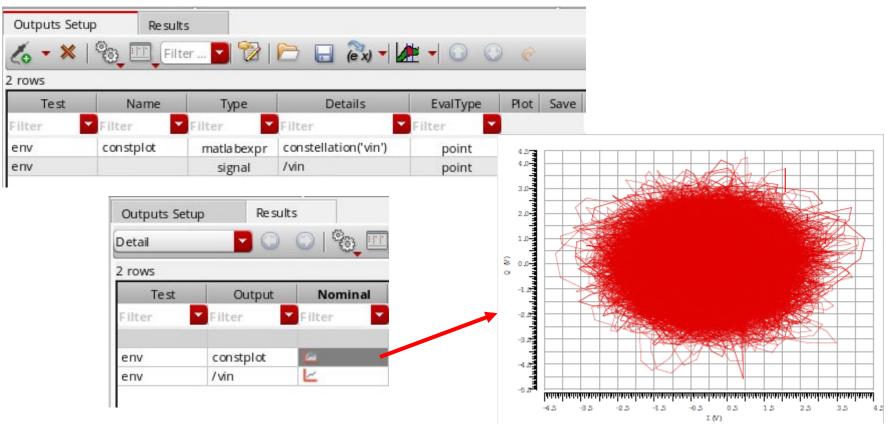






MATLAB Expression Return Value

Results from MATLAB can be waveforms or scalar measurement result values

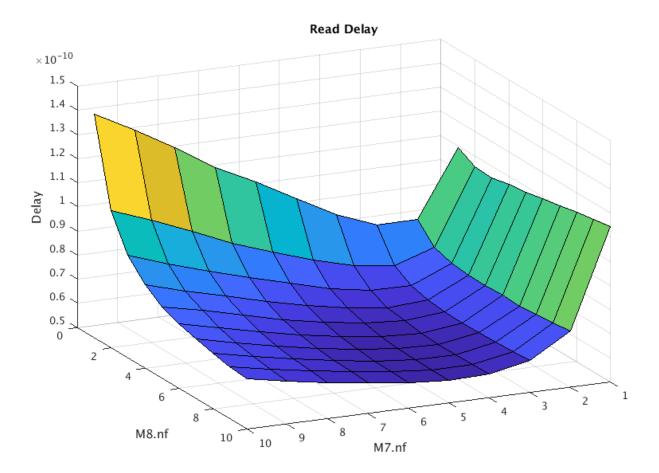






MATLAB Visualization

ADE results can also easily be plotted in MATLAB





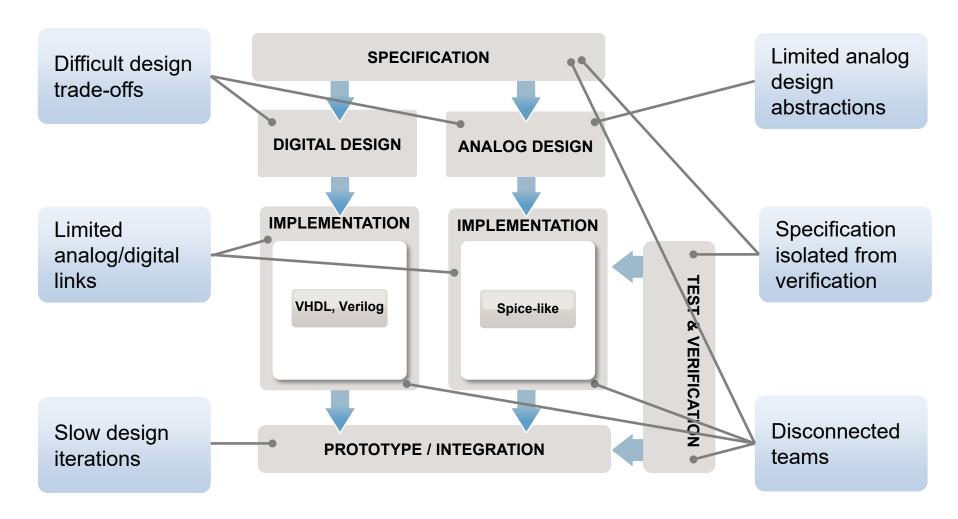


Introduction to System Modelling in Simulink





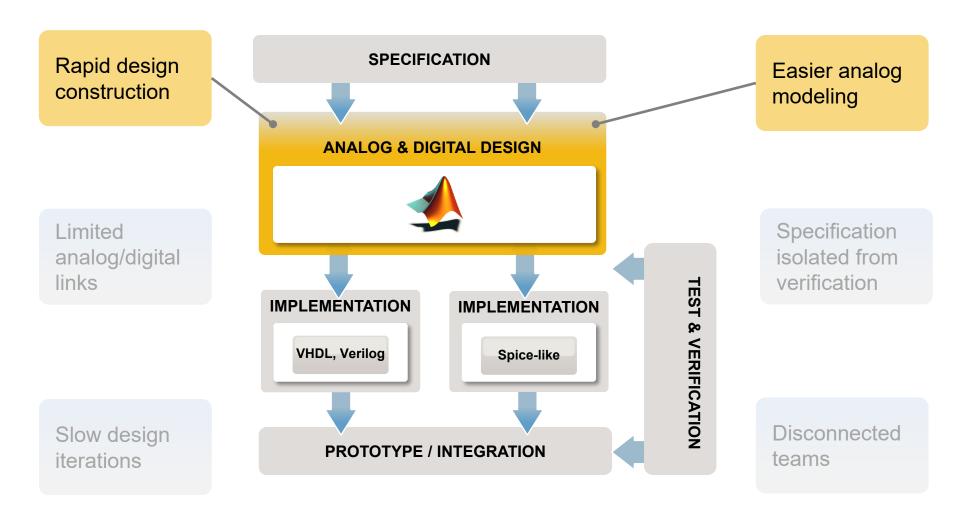
Mixed-Signal Design and Verification Challenges







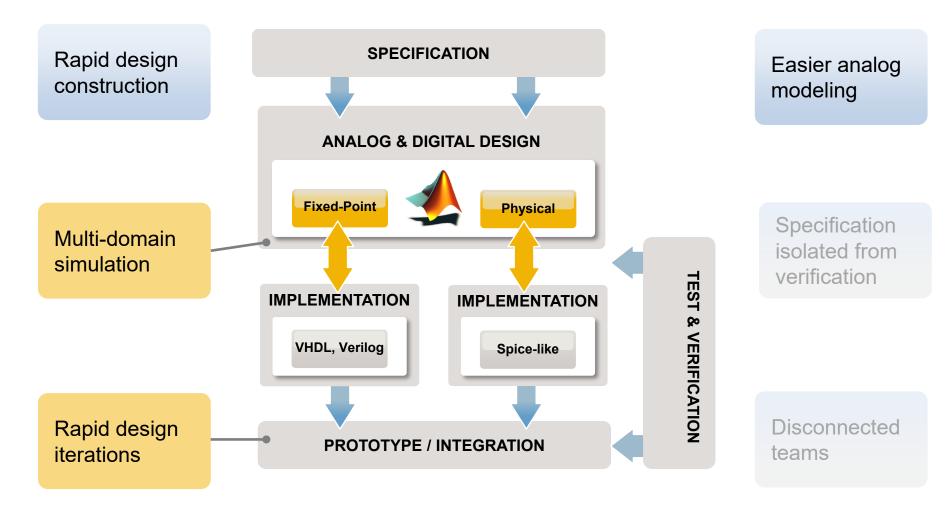
Focus on Algorithm Design







Anticipate Impairments at System-Level





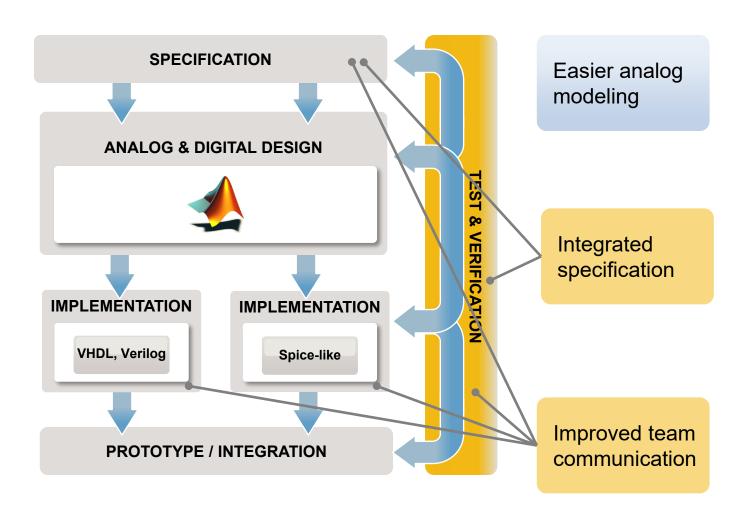


Continuous Verification

Rapid design construction

Multi-domain simulation

Rapid design iterations





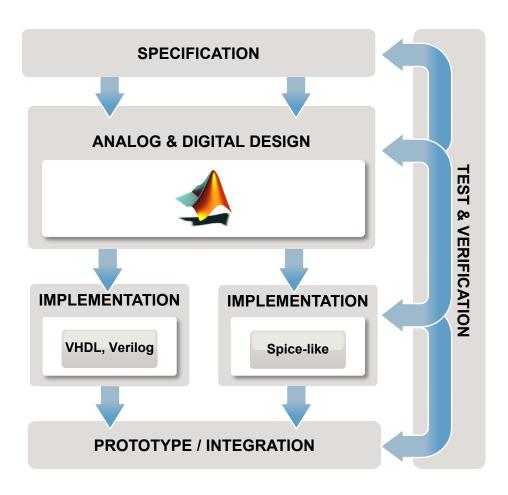


Integrated Design and Verification of Mixed-Signal Systems

Rapid design construction

Multi-domain simulation

Rapid design iterations



Easier analog modeling

Integrated specification

Improved team communication





A Next-Generation Workflow for System-Level Design of Mixed-Signal Integrated Circuits

By Kunihiko Tsuboi and Nobutaka Okumura, STARC

In the competitive world of mixed-signal design, project delays are deadly for profitability. Design cycles are short, and the market moves very quickly, giving a competitive edge to any company that manages to accelerate its design process. At the Semiconductor Technology Academic Research Center (STARC), we have been given the mission of finding a way to cut design time in half and eliminate costly respins for our supporting companies. We have achieved this goal with our new system-level design flow.

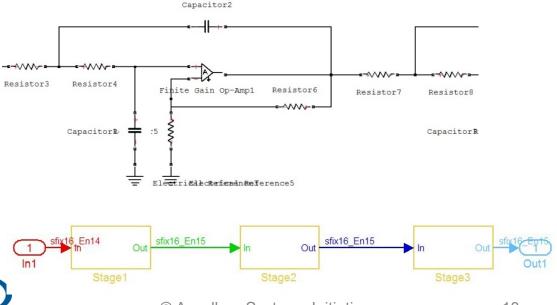
Our system-level design flow (which we call STARCAD-AMS) starts with rapid and extensive behavioral modeling in Simulink. Once we have a design that works at the system level, we generate C code from our Simulink models and import it into Cadence Virtuoso, where it is simulated using AMS Designer. We use our C code to verify the correctness of our circuit-level designs. We have benchmarked our STARCAD-AMS flow using a sigma-delta analog-to-digital converter (ADC) design. Our results show that design time is cut in half.

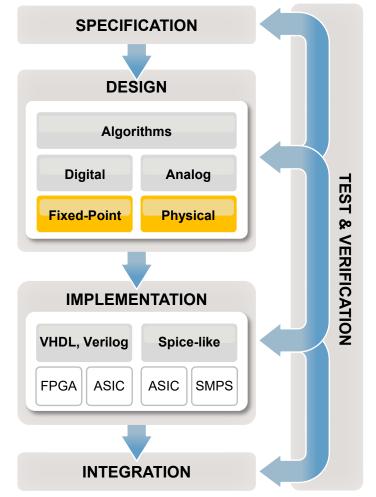
http://www.mathworks.com/company/newsletters/articles/a-next-generation-workflow-for-system-level-design-of-mixed-signal-integrated-circuits.html



Analog / RF Behavioral Modelling

- Mixed-behavioral and circuit design
- Modelling in the electrical domain
- Describe the architecture of the analog front-end



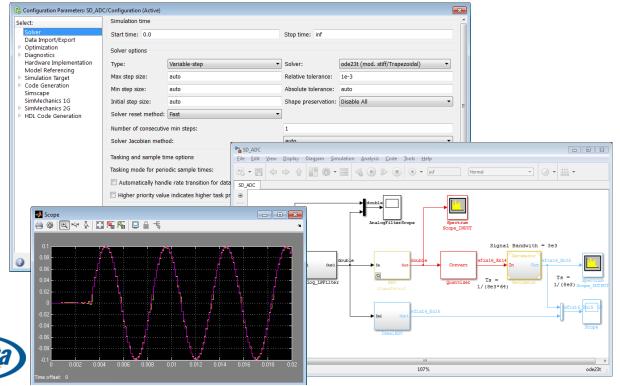


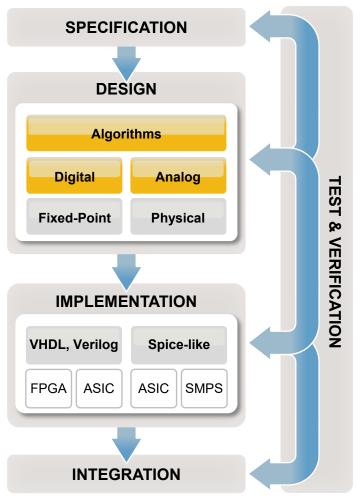


SYSTEMS INITIATIVE

Mixed-Signal Modelling with Simulink

- Analog and digital in same model
- Time handling
- Multiple solvers / schedulers



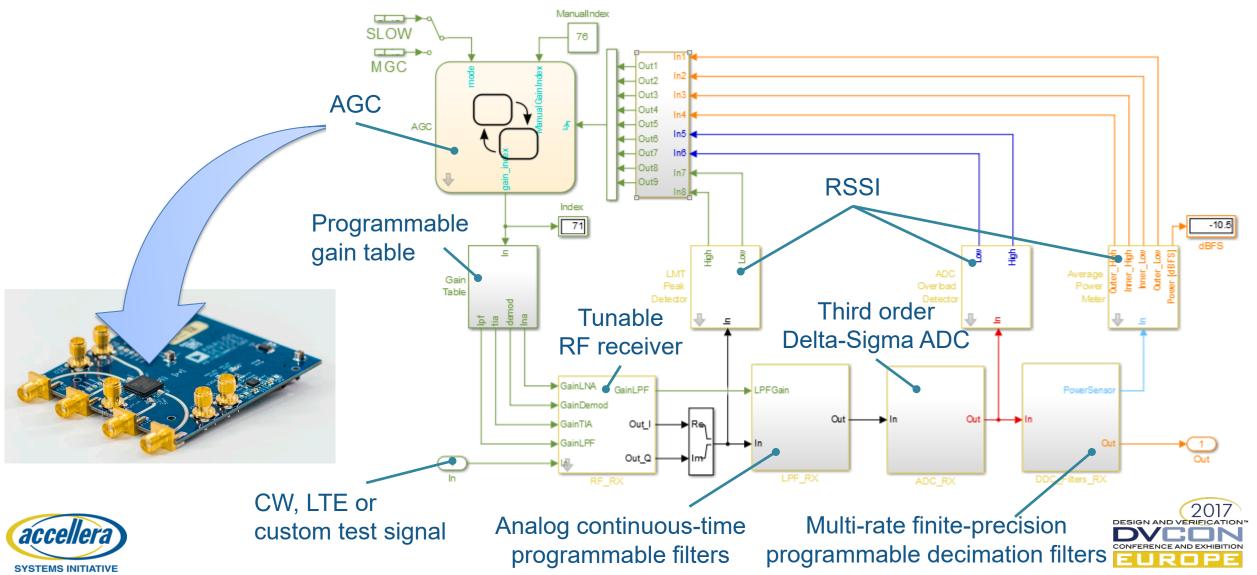




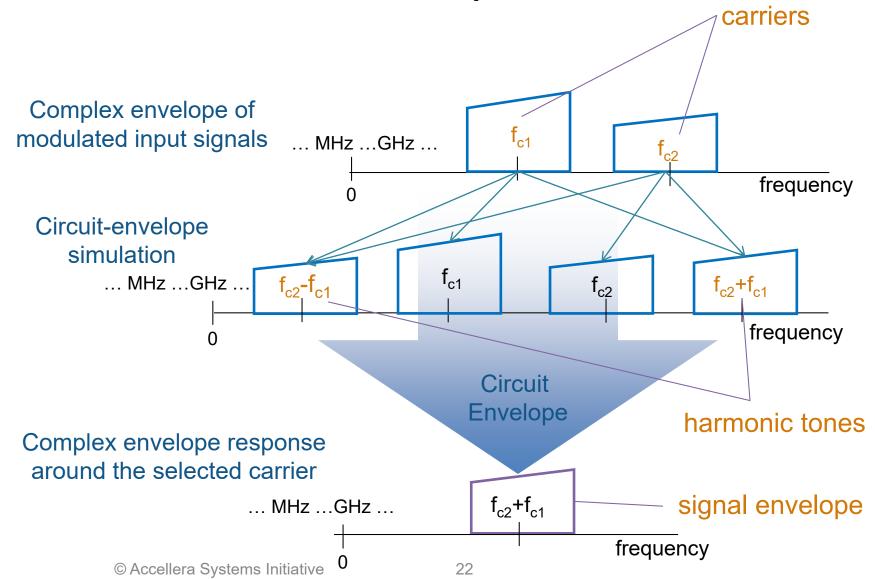


Example: AD9361 Agile RF Receiver

http://www.mathworks.com/hardware-support/analog-devices-rf-transceivers.html



Multi-Carrier Envelope Simulation for RF

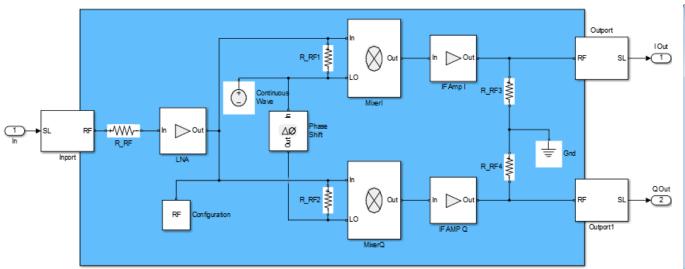


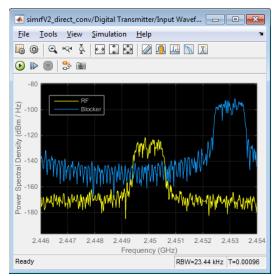




RF System-Level Simulation With RF Blockset

- Design the architecture and specs of the RF front-end
- Integrate RF with adaptive algorithms such as DPD, AGC
- Test and debug the implementation before going in the lab
- Provide a model to your colleagues and customers









Refining and Validating Models with Interfaces to Cadence Virtuoso AMS Designer





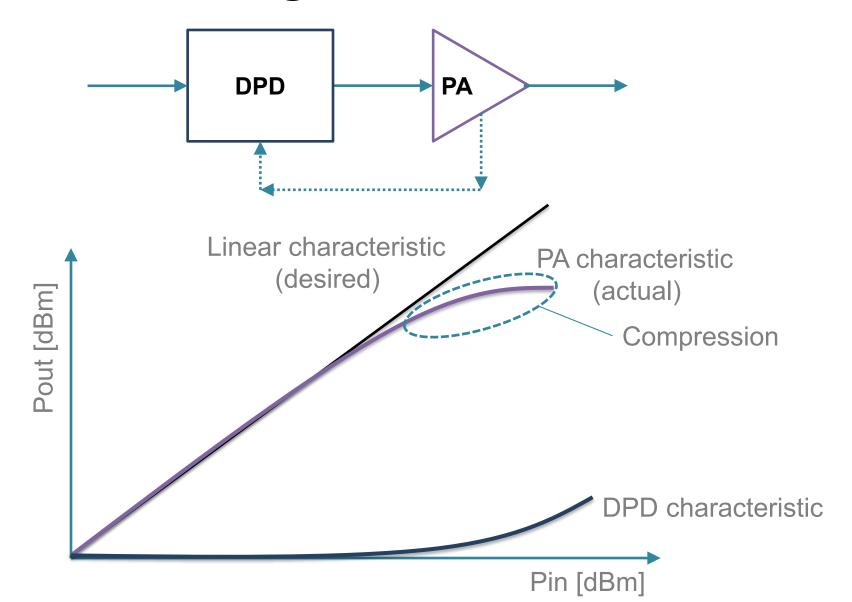
Model Development Is an Iterative Process

- Start with the available information
 - Data sheet parameters, design specs
- Refine the model
 - Include results coming from IC simulation or measurements from prototypes
- Validate
 - Test the model with new signals





What Is Digital Pre-Distortion?

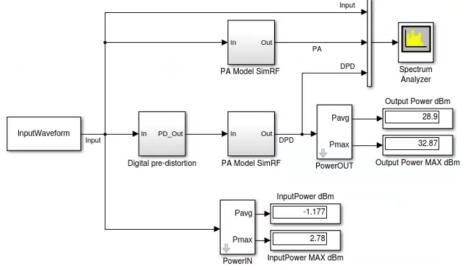


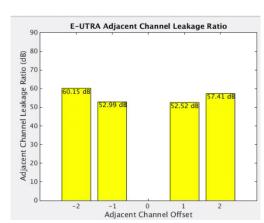


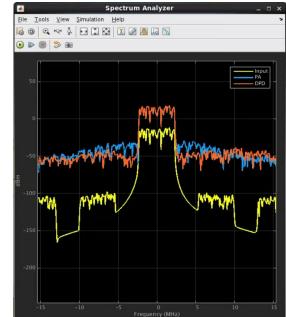


How to Design a DPD Algorithm?

- Characterize the PA using wideband signals (e.g. LTE)
 - Measurements
 - Circuit level simulation
- Identify an accurate model of the PA (e.g. Volterra series)
- Validate the PA model
- Design the Digital Pre-Distortion algorithm

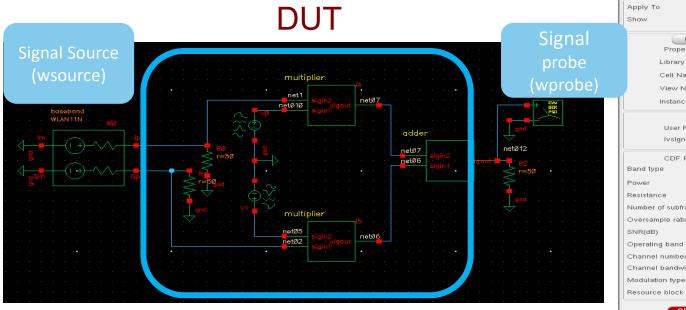


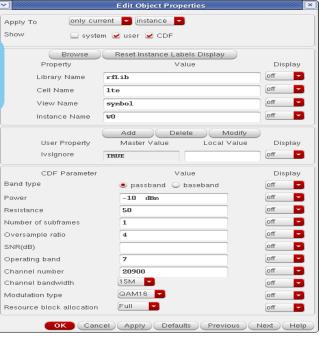






Cadence[®] Spectre[®] RF Wireless Analysis





Wireless standard-compliant

- Zigbee
- 802.11n
- 802.11ac
- LTE
- 802.11a
- 802.11p

The latest additions

- Bluetooth LE
- 802.11af/ah/ad
- 802.15.4g (smart meter)
- 802.11b
- Msource

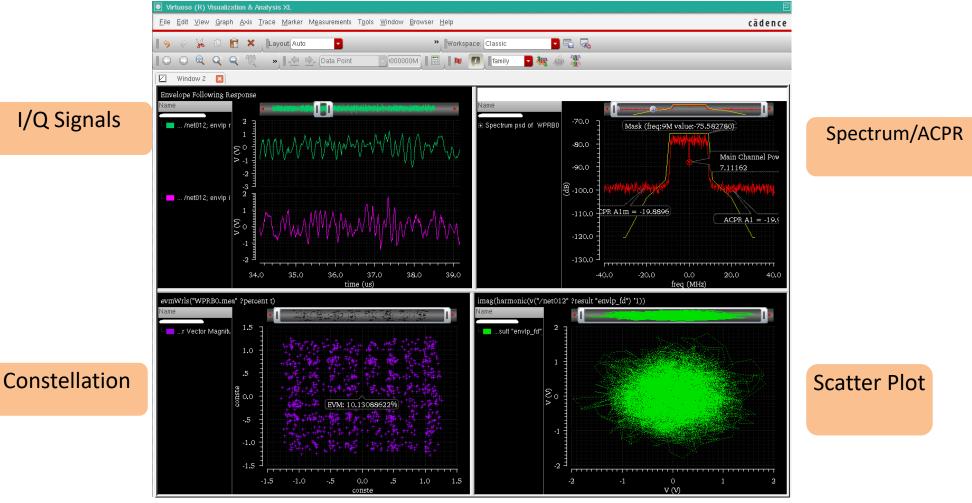
Powerful modeling technology

- Proprietary fast envelope analysis
- Efficient result post-processing
- Standard-specific post-processing
- EVM, BER, spectrum available directly with minimal or no setup





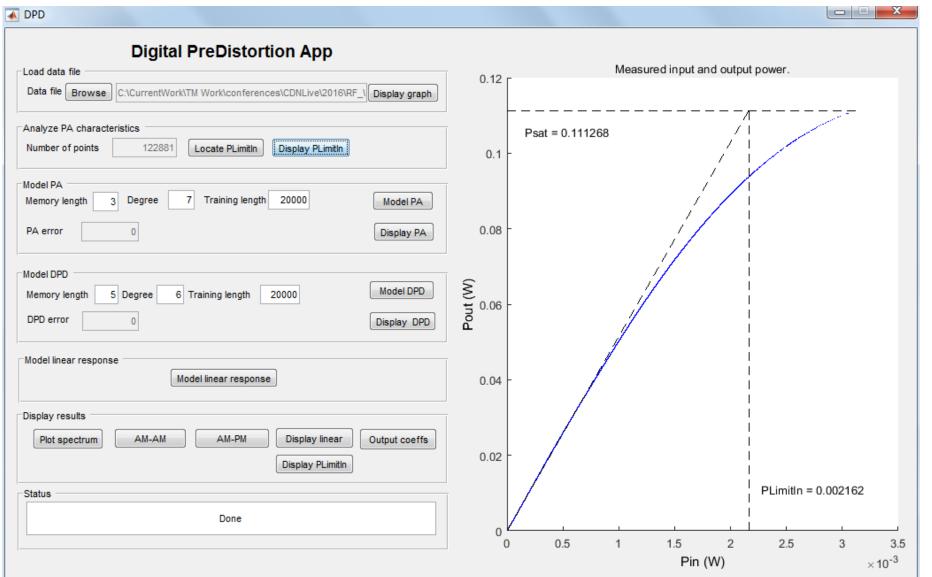
Automated post-processing setup in Virtuoso® ADE







PA Characterisation and the DPD App

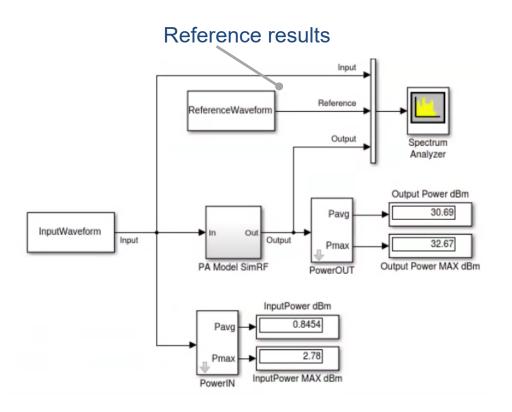






Validation of the PA Model

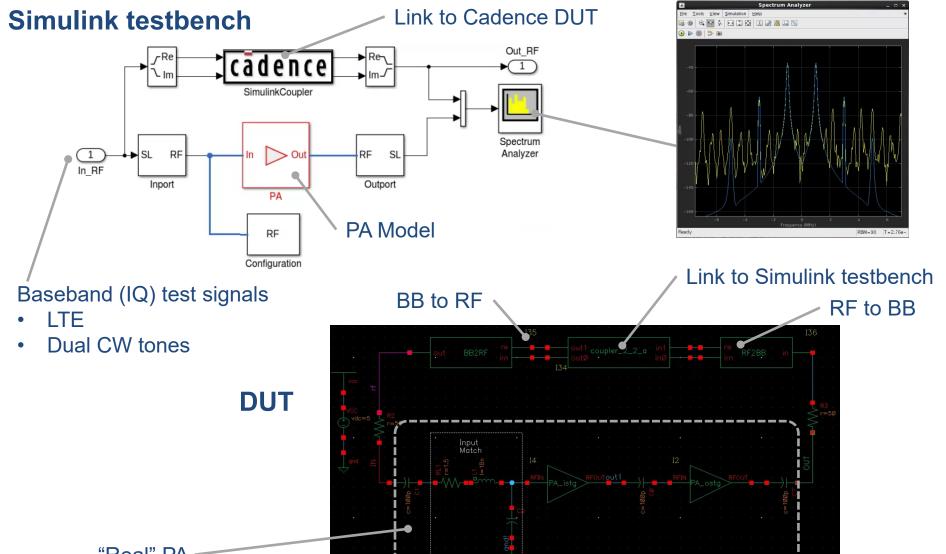
Order = 9





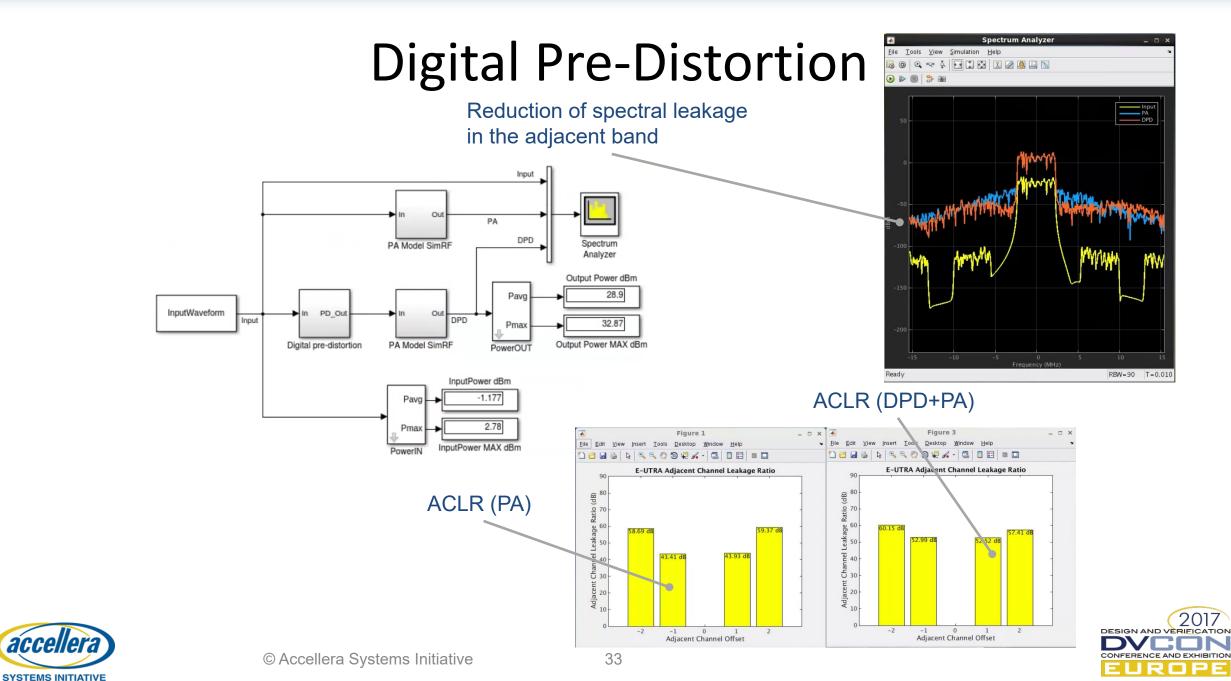


PA Model Validation Using Cosimulation









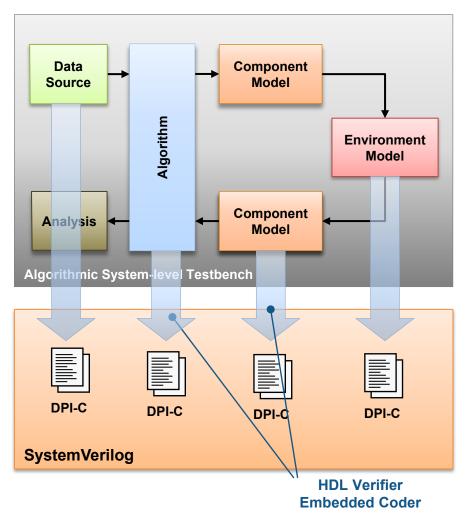
Exporting Models from MathWorks Tools to Cadence





SystemVerilog DPI-C Component Generation

Reuse of models in SystemVerilog environment



Develop

- System components (IP and test benches)
 in MATLAB and Simulink
- Model, Simulate, and Verify

Export

- Components as C code with SystemVerilog wrappers
- Fixed-point or real number interfaces

Integrate

DPI-C components in Virtuoso and Incisive

Verify

Verification of the complete system design





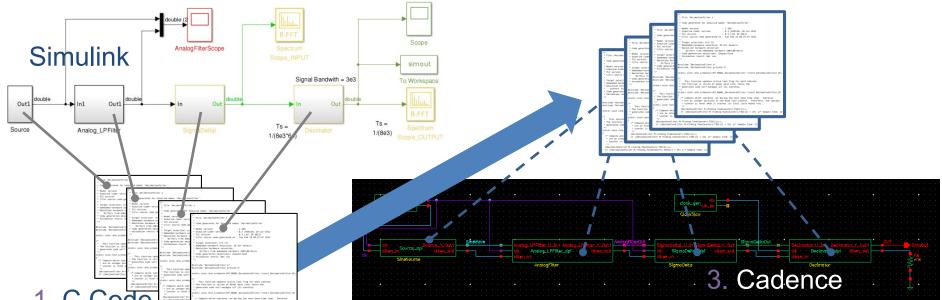
Using C Code Generation and the DPI-C Interface

- Make your model compliant with C code generation
- Generate C code from your Simulink model or MATLAB code
- Automatically wrap the C code using the DPI-C interface

Import, build and simulate an equivalent behavioral SystemVerilog

model in your IC design tool

2. SystemVerilog wrapper

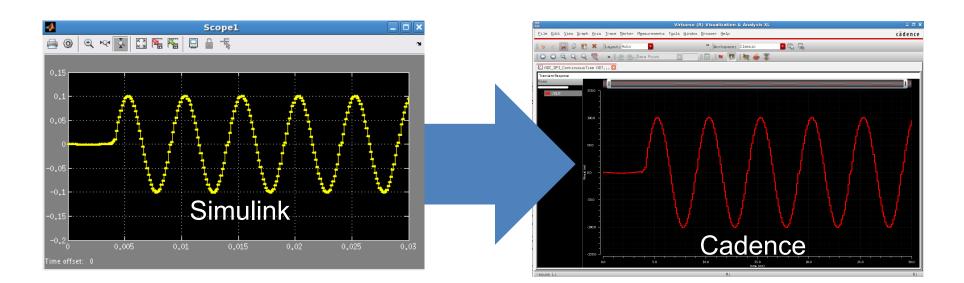






Benefits of C Code Generation and DPI-C Export

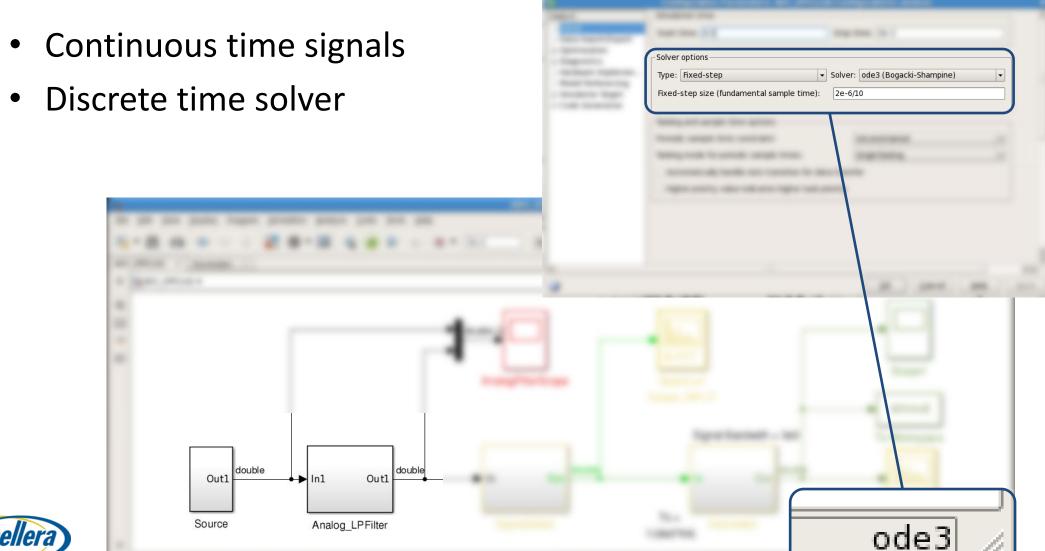
- Fast simulation using the native SystemVerilog DPI-C API
- Customizable approach supported by MathWorks
- Leverages mature C code generation technology
- Most suitable for testbench generation and IC verification
- Support discrete and continuous time signals







Export of Mixed-Signal Models

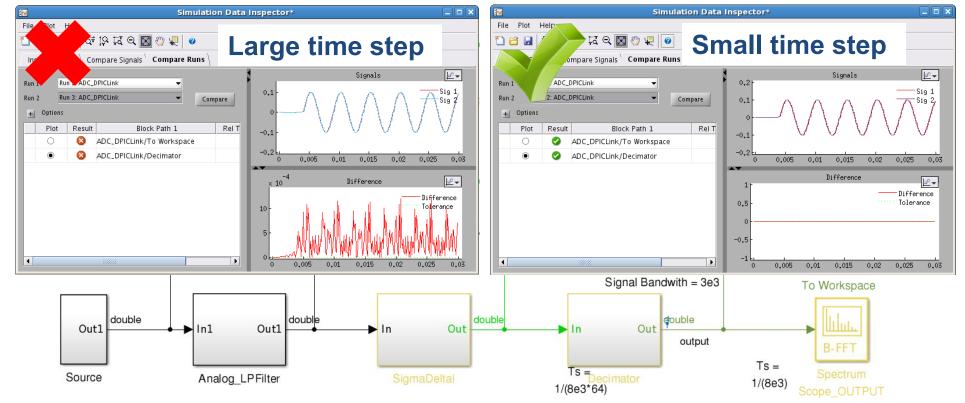






From Variable to Fixed Step Solver

- Chose a fixed sample time that it is small enough to give correct results
- Tradeoff accuracy and simulation time







Summary

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Questions

Finalize slide set with questions slide





References

- Virtuoso ADE Matlab Integration Rapid Adoption Kit
 - https://goo.gl/GCZXLv
- A Next-Generation Workflow for System-Level Design of Mixed-Signal Integrated Circuits
 - http://www.mathworks.com/company/newsletters/articles/a-next-generation-workflow-forsystem-level-design-of-mixed-signal-integrated-circuits.html
- AD9361 Agile RF Receiver
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- Adaptive DPD Design: A Top-Down Workflow
 - https://uk.mathworks.com/company/newsletters/articles/adaptive-dpd-design-a-top-down-workflow.html
- Solve RF/AMS Design Challenges Using the Cadence Virtuoso Solution and Tensilica DSPs
 - https://ip.cadence.com/uploads/1063/TIP WP Pipeline ADC Calibratiion and Testing FINAL-pdf



