2016 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

Unique Verification Case Studies of Low Power Mixed Signal Chips

Jeff Goswick – Principle Design Engineer, NXP Semiconductors

Venkatesh Ranga – Architect, NXP Semiconductors

Madhusudhan Subramanya – Architect, NXP Semiconductors

Anand Shirwal – Department Manager, NXP Semiconductors

Pramod Rajan K S – Senior Design Engineer, NXP Semiconductors

SECURE CONNECTIONS FOR A SMARTER WORLD

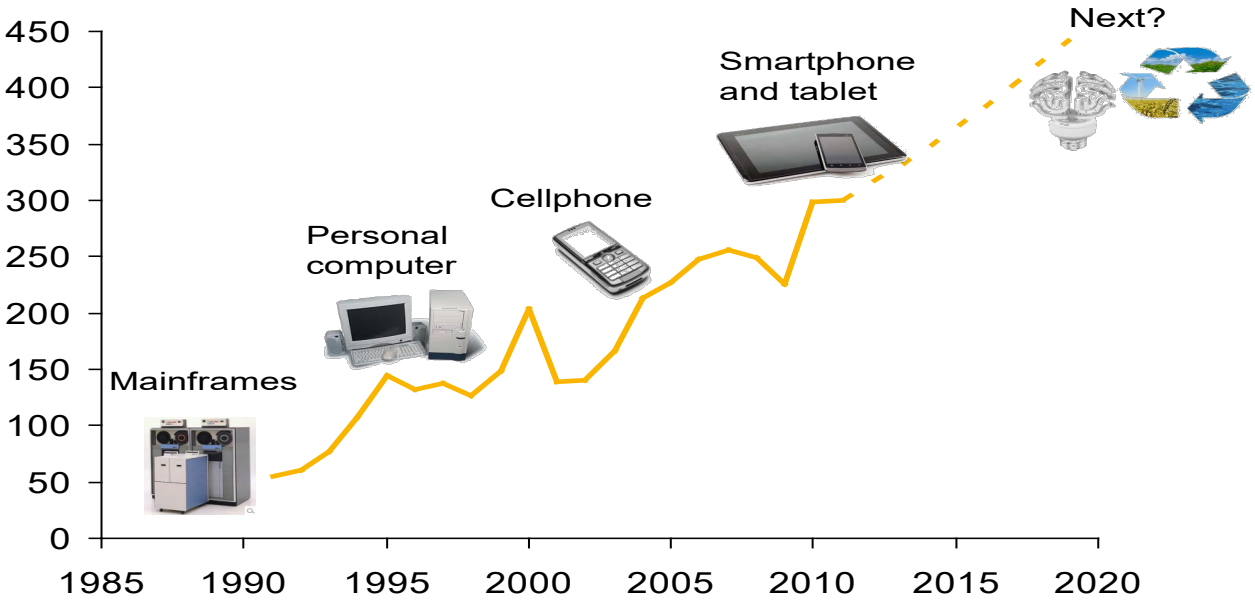
2016 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

Agenda

- Introduction
- Four Real Life Challenges Encountered in Low Power Mixed Signal SoC Verification
- Conclusion

Introduction

- Internet of Things (IoT) is a fast growing application domain and is a key driver in taking the semiconductor industry revenue to over 400 billion dollars by 2020.



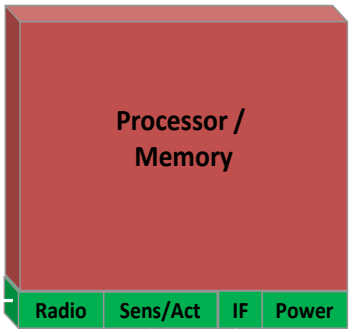
Source: WSTS (extrapolated after 2011), Cisco, BBC, Gartner, GSMA, OECD
(1) Excluding phones, computers,

Introduction

- From the chip design perspective, the IoT application area moves the focus away from the big system on chip (SOC) to the mixed signal world.

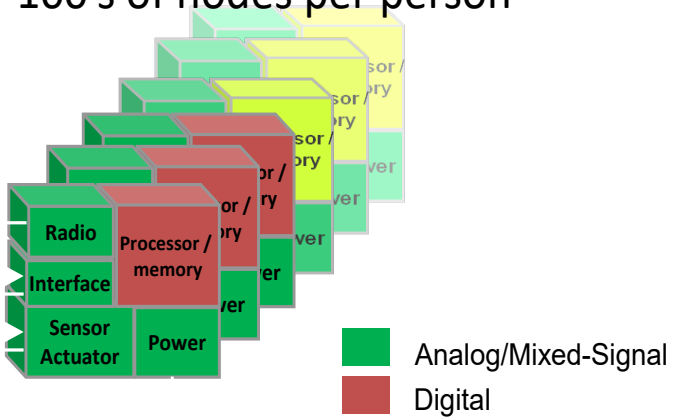
Digital age

- SoC Centric



Internet of smart things

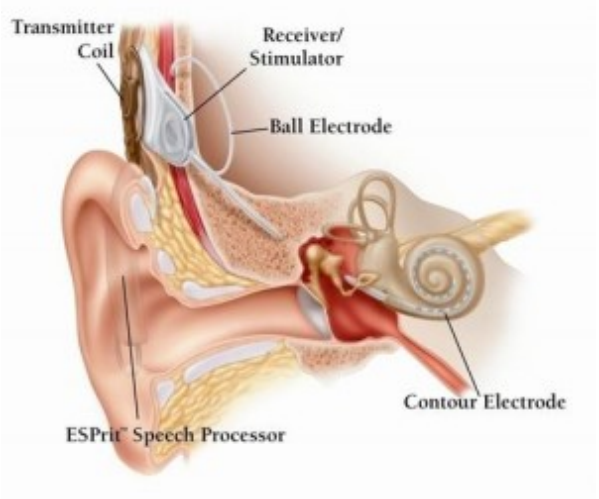
- 100's of nodes per person



Applications of the Case Studies

Low-power, Compact solution for temperature logging with NFC

This cost-effective, small-form-factor solution enables long-lasting time-temperature integrators (TTIs).



Wearable Product in Health Care Sector

Highly integrated ultra-low power operation, encompassing highly sensitive analogue front-ends, low power DSP, NVM, and wireless connectivity streaming data and audio robustly around and safely though the body.

Ideal solutions for micro speakers:

Class-D Audio Amplifier

Louder, Deeper, Better, & Safer

2016 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

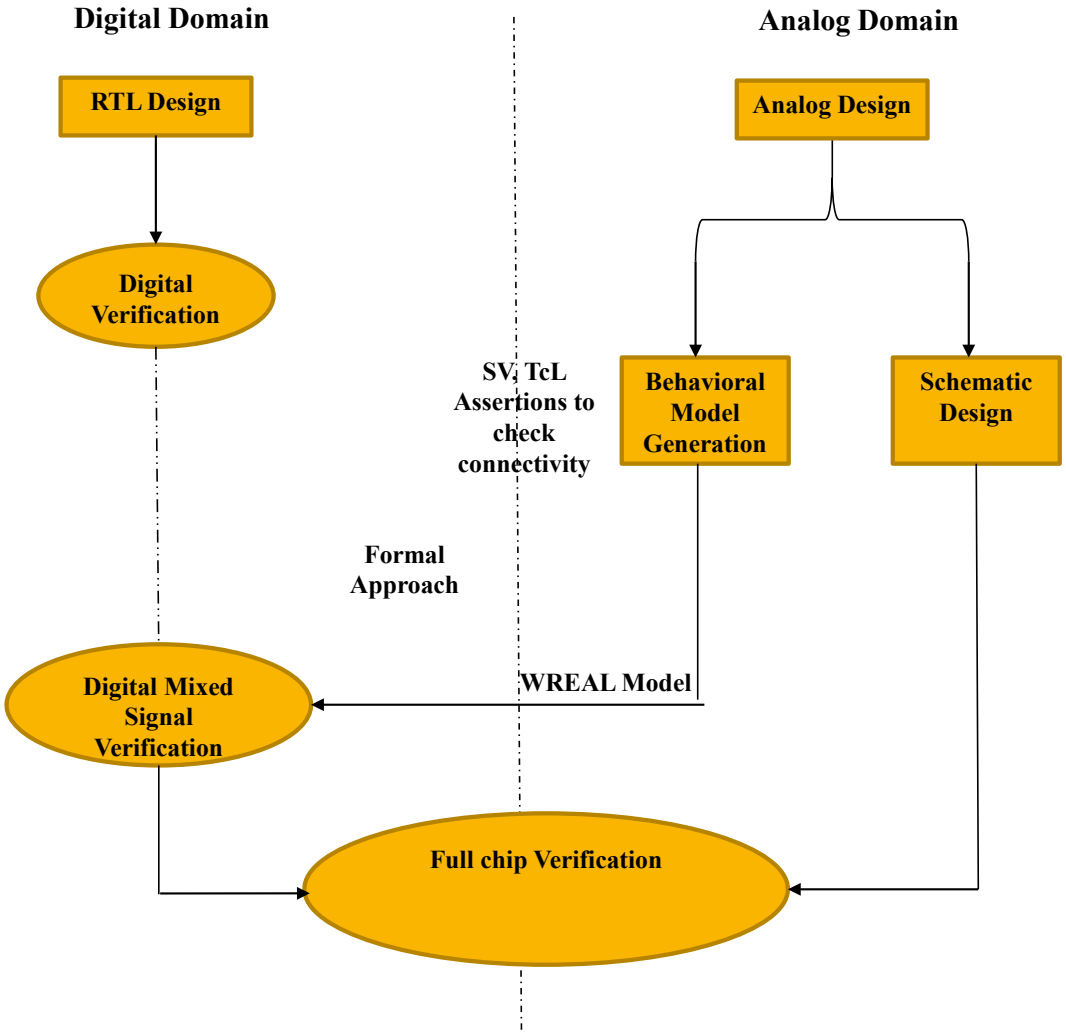
Real Life Challenges

Low Power Mixed Signal SoC Verification

1. Modeling induced power devices in CPF and verification environment implications
2. Analog behavioral modeling for verification of complex power management systems
3. Self-checking test bench environment and formal checks for connectivity
4. Low drop out (LDO) sign-off criteria

Real Life Challenges

Low Power Mixed Signal SoC Verification

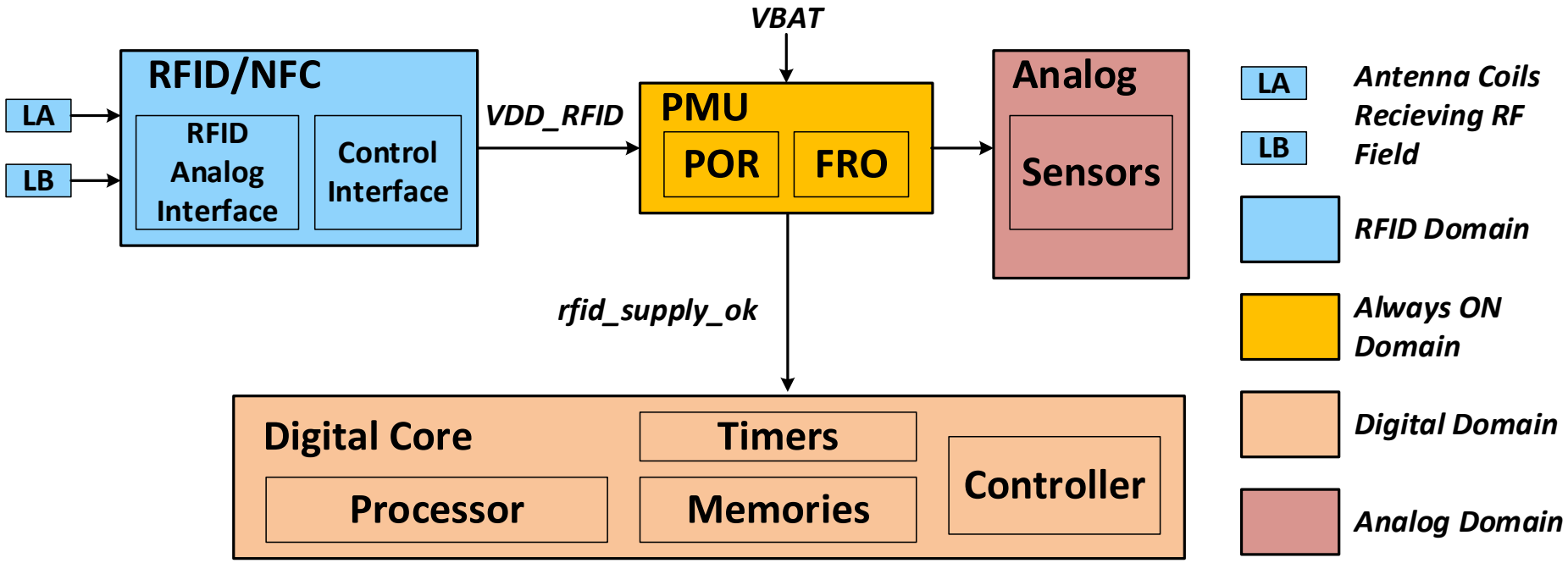


2016 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

Case Study – 1

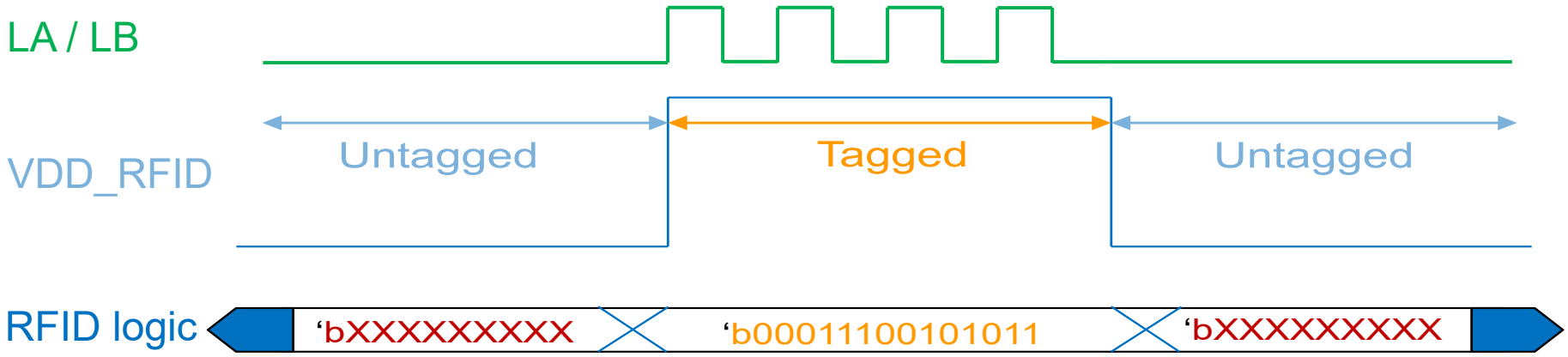
Modeling induced power devices in CPF and verification environment implications

- Challenge: model the RFID/NFC power domain and verify its structure using CPF.
- Power diagram of the NFC sensor:



RFID Domain Power

- The RFID is powered when the chip is “tagged” meaning when the antennas are receiving RF power from an NFC reader.
- To verify correct isolation and tagged/untagged transitions, in simulation the RFID logic should be corrupted when the chip is “untagged”.



The Issue: RFID Domain Isolation

- Power intent
  - The PMU sets “rfid_supply_ok” to 1 or 0 based on the presence or absence of VDD_RFID respectively.
  - This signal is used as the ‘isolation_condition’ in the CPF isolation rules for signals output from PD_RFID.
  - Initially, “rfid_supply_ok” was also used in the CPF for the ‘shutoff_condition’ of the PD_RFID domain.
- The same CPF is used for synthesis, simulation, and formal low power verification.

The Issue: RFID Domain Isolation

- In simulation PD_RFID logic is correctly corrupted when unpowered, but
  - When VDD_RFID=0, the PD_RFID domain is OFF, and the CPF causes simulation tools treat all outputs of PD_RFID as X.
  - This makes “rfid_supply_ok” to go X as well.
  - In order to bring the PD_RFID domain back to ON again, the ‘shutoff_condition’ signal ‘rfid_supply_ok’ needs to be made as 1.
  - But since ‘rfid_supply_ok’ is derived from ‘VDD_RFID’ itself, this cannot happen, a catch-22 situation.

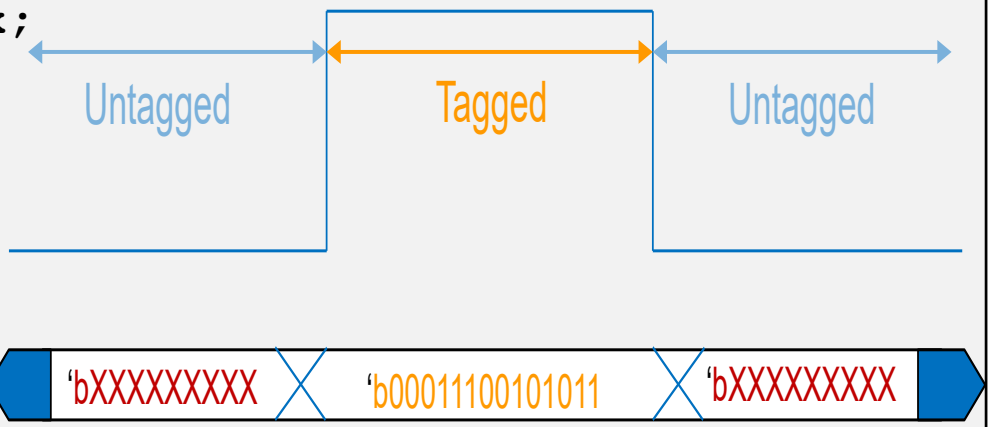
Solution, almost

- Define PD_RFID (create_power_domain in CPF) with "-external_controlled_shutoff" option without any "-shutoff_condition".
- This models the "self-powered" aspect of PD_RFID domain correctly in CPF.
- This makes the simulation tools to see "rfid_supply_ok" as 0 when PD_RFID is OFF, and as 1 whenever PD_RFID is ON.
- **BUT** – the simulator doesn't corrupt the logic in PD_RFID when the "vdd_rfid" power is off because of the "-external_controlled_shutoff" option.

Solution Implemented

- The test bench was modified to replicate the tool behavior. It corrupts the signals in the switched off domain when an “untagged” event is detected.

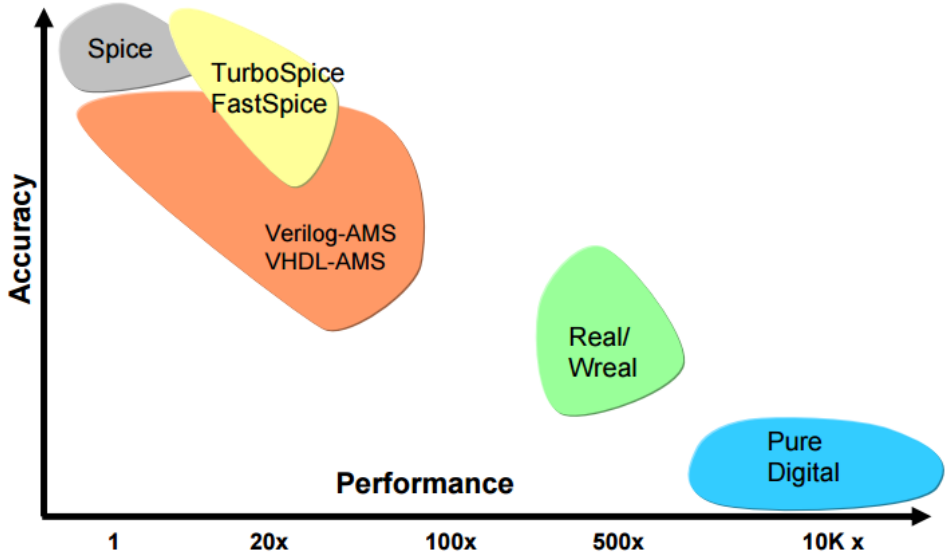
```
task corrupt_rfid_signals(input bit yes);
begin
  if(yes)
  begin
      force dut.Signals = 'bx;
  end
  else
  begin
      release dut.Signals;
  end
end
endtask
```



Case Study – 2

Analog behavioral modeling for verification of complex power management systems

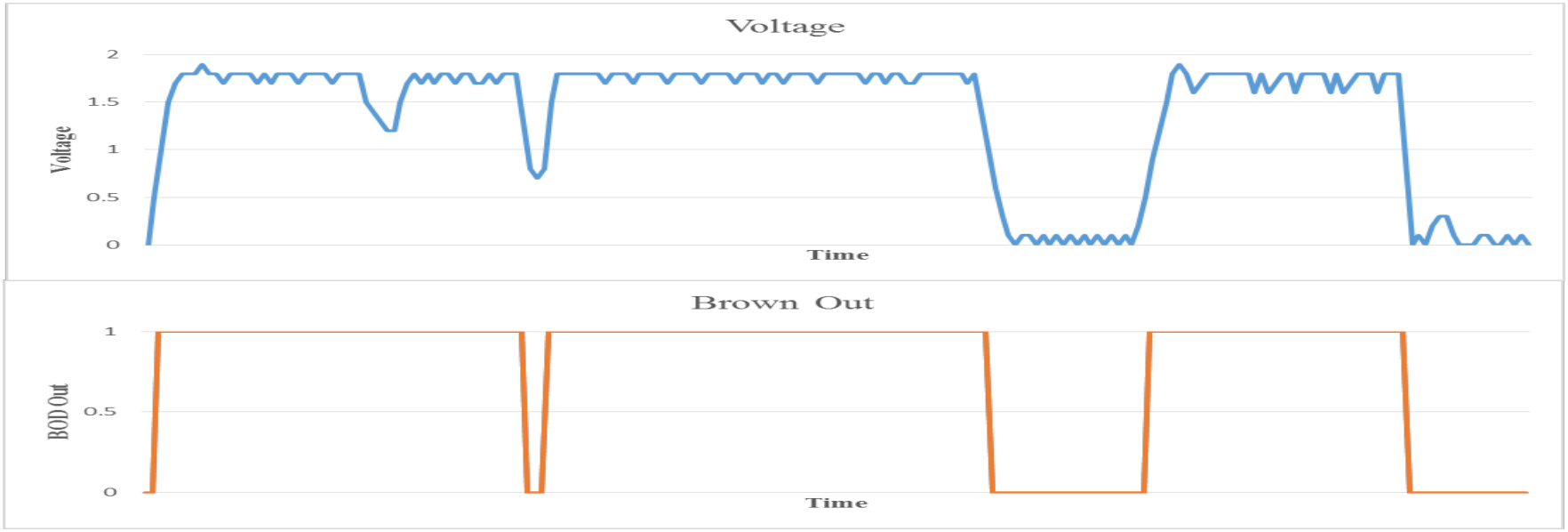
- Models of analog blocks are critical for mixed signal chip verification.
- Different abstraction levels are used in the project life cycle to tradeoff speed versus accuracy.
  - **System Verilog (SV):** Fast digital model with advantages for timing variation
  - **Verilog wreal:** Psuedo-analog model that runs on a digital simulation engine
  - **Verilog AMS:** Analog model for AMS simulations but faster than spice



Case Study – 2

Analog behavioral modeling for verification of complex power management systems

- Example: Supply voltage brown out detector (BOD)



Case Study – 2

Analog behavioral modeling for verification of complex power management systems

- System Verilog
  - Allows randomization of the analog parameters to better match reality.

```
forever
begin
  randomize(randDelayBodLdoDigHigh) with {randDelayBodLdoDigHigh>=10;
                                          randDelayBodLdoDigHigh<=50;};
  repeat (randDelayBodLdoDigHigh) @(posedge a2p_ulpo_clk_400khz);
  randomize(bod_ldo_dig);
  randomize(randDelayBodLdoDigLow) with {randDelayBodLdoDigLow>=10;
                                         randDelayBodLdoDigLow<=20;};
  repeat (randDelayBodLdoDigLow) @(posedge a2p_ulpo_clk_400khz);
  bod_ldo_dig = 1;
end
```

Case Study – 2

Analog behavioral modeling for verification of complex power management systems

- Wreal
  - Allows real number values to propagate on Verilog wires and ports.
  - Runs with only the digital simulation engine and license.
  - Can model simple ideal behavior or very complex behavior.
  - Can create a complex hierarchical model that can also aid in verifying the analog block itself by modeling “bottom up” using a Verilog netlist from a schematic capture tool (e.g. Cadence Virtuoso) and modeling leaf cells only.

Case Study – 2

Analog behavioral modeling for verification of complex power management systems

- Ideal wreal model

```
inout vdd_dig;
wreal vdd_dig;
real vdd_dig_p;
reg vdd_dig_hist;
...
// vdd_dig_hyst  = rising supply
always @( vdd_dig ) begin
  vdd_dig_hyst = vdd_dig > vdd_dig_p ? 1:0;
  vdd_dig_p    = vdd_dig;
end
assign a2a_bod_vdig = !p2a_bod_ldo_dig_enable ? 1'b0 :
  (pmu_bod_ldo_dig ?
    ((vdd_dig > 0.495 + p2a_bod_ldo_dig_thr_set * 0.025 +
                vdd_dig_hyst * p2a_bod_hyst_set * 0.0165) ? 1'b0 :
1'b1)
  : 1'bZ);
```

Case Study – 2

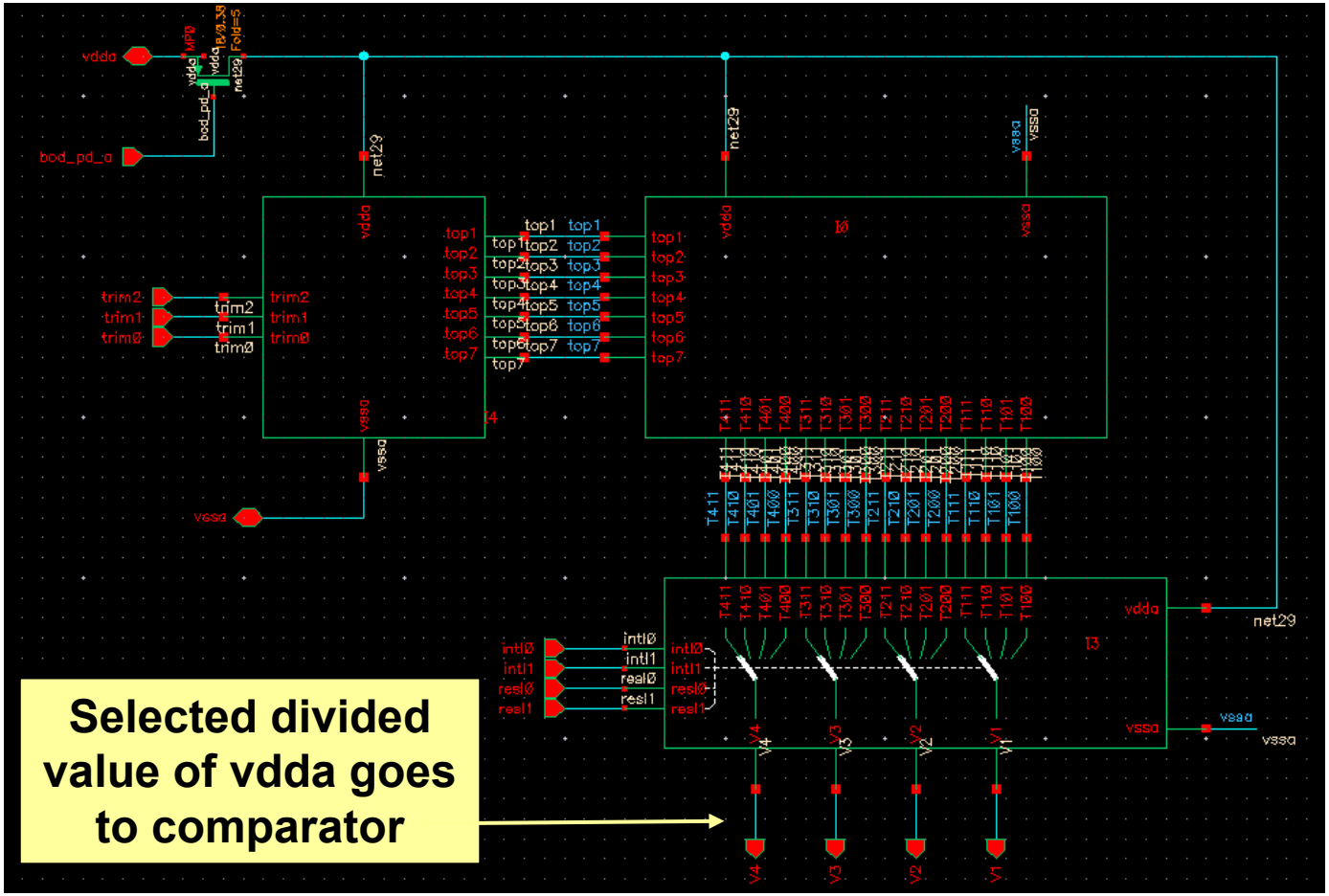
Analog behavioral modeling for verification of complex power management systems

- Bottom up / netlisted hierarchical models
  - Create hierarchical model from existing schematics
  - Port directions, names, bus widths, etc., automatically correct
  - Leaf cell behavioral models are simpler, easier to write, not as error prone
  - Top level model is largely correct by construction
  - Analog IP bugs often found during model creation

Case Study – 2
Netlisted wreal model

BOD circuits:

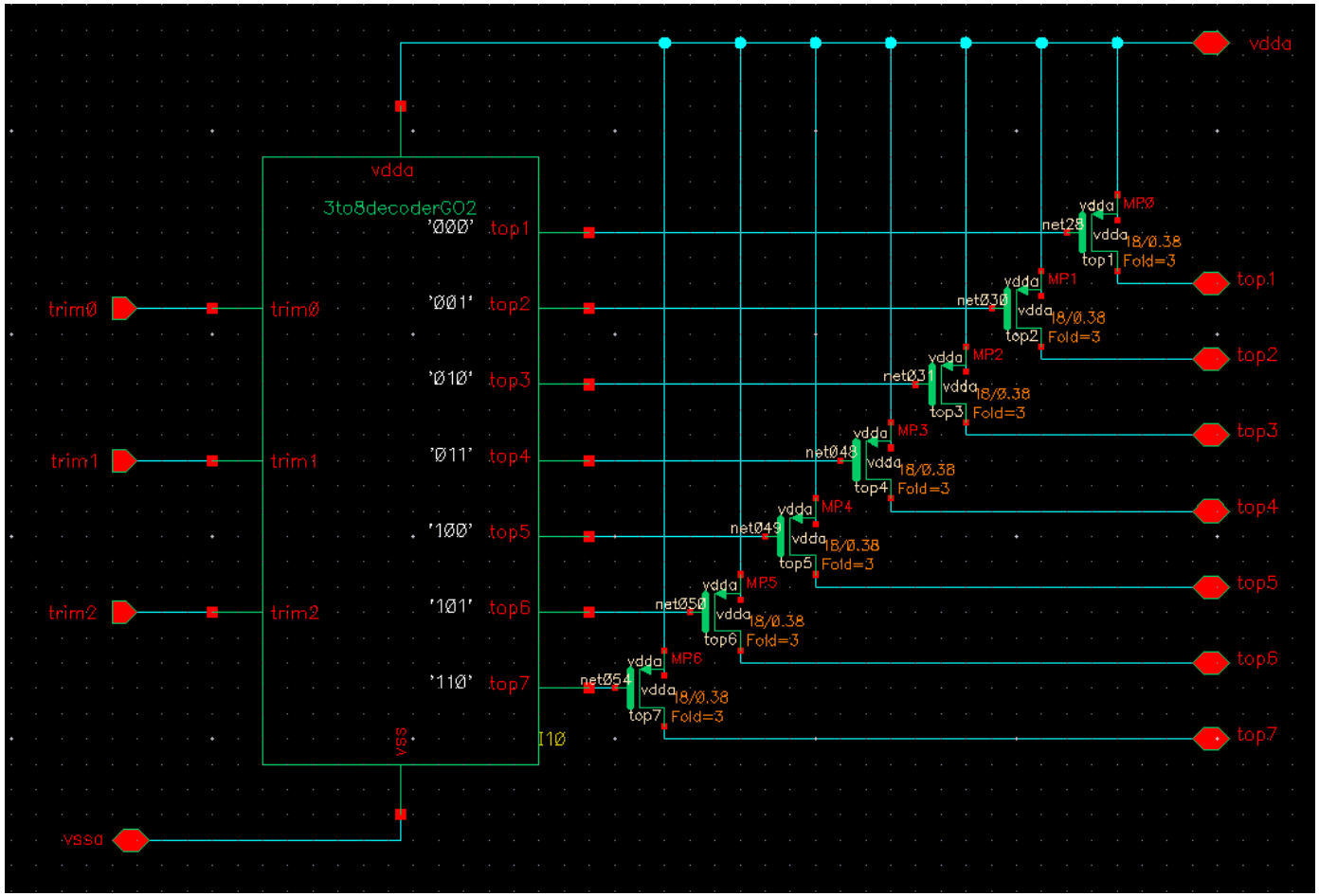
1. Trim mux
2. Vdd resistor divider
3. Trip level select mux



Case Study – 2
Netlisted wreal model

Trim mux:

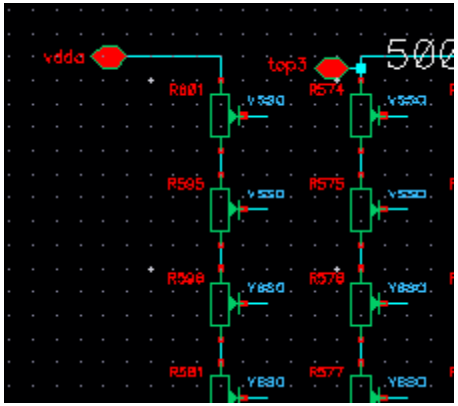
3 to 7 decoder & 7 pass gates to connect vdda to top tap points in resistor divider



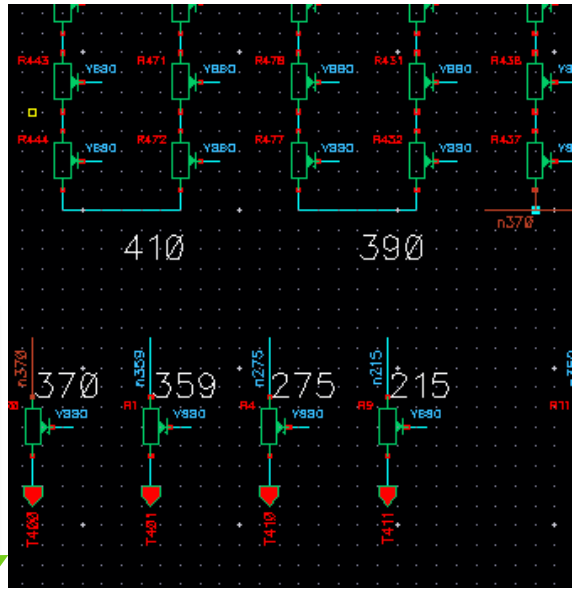
Case Study – 2
Netlisted wreal model

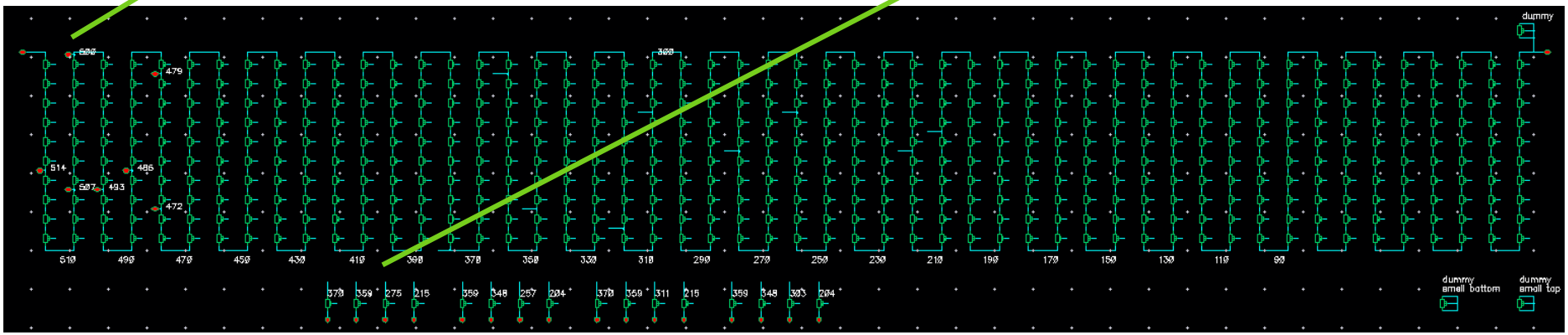
Resistor divider:

Trim supply input taps “top1”, “top2”, etc.



Divider output taps T400, T401, etc.





Case Study – 2
Netlisted wreal model

```
module divider_string_bod_lp ( T100, T101, T110, T111, T200,...
inout  top1, top2, top3, top4, top5, top6, top7, vdda, vssa;
output T100, T101, T110, T111, T200,...
wreal T100, T101, T110, T111, T200,...

always @(top1 or top2 or top3 or top4 or top5 or top6 or top7)
begin
  bad_rladder = 0;
  if (top7 === 1)
    ladder_length = 472;
  ...
 else
    bad_rladder = 1;
end
assign vdda_value_i = bad_rladder === 0 ? vdda_value
                                        : `wrealXState;
assign T100 = vdda_value_i * 273 / ladder_length;
assign T101 = vdda_value_i * 231 / ladder_length;
```

Case Study – 2

Analog behavioral modeling for verification of complex power management systems

- Verilog AMS model snippet

```
  always @ (threshold,hyst) begin
    rvref_lo = rvin + `step_size_trig * (threshold);
    rvref_hi = rvin + `step_size_trig * (threshold) +
`step_size_hyst * (hyst);
  end

  a2d #(.vh(0.001),.vl(-0.001)) i_convert_lo(comparator_lo,
ref_lo_e);
  a2d #(.vh(0.001),.vl(-0.001)) i_convert_hi(comparator_hi,
ref_hi_e);

  analog begin
    V(ref_lo_e,n) <+ V(p,n)-transition(rvref_lo,0,100n,100n);
    V(ref_hi_e,n) <+ V(p,n)-transition(rvref_hi,0,100n,100n);
  end
```

2016 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

Case Study – 3

Self-checking testbench and verification environment for mixed signal SoCs

- Leverage the digital verification techniques for mixed signal designs.
- Employ assertion techniques such as PSL and SVA.
- SV bind capability enables assertions developed at module level to be re-used at top level.

Case Study – 3

Self-checking testbench and verification environment for mixed signal SoCs

- Several methods of connectivity checks at the digital and analog boundary interface were deployed including a formal approach and a TcL based connectivity check.

```
TcL:
check_connectivity $path(SOURCE) $path(DESTINATION)
```

Case Study – 3

Self-checking testbench and verification environment for mixed signal SoCs

- Assertions were coded in SV to check on the internal supply voltage of an analog block to be within a threshold level.

```
assert (((VGG * 1000) > l_vgg_val) && ((VGG * 1000) <
          h_vgg_val))
else $display("VGG out of regulation with value: %f
     expected to be: %f", (VGG * 1000), vgg_val);
```

2016 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

Case Study – 3

Self-Checking Testbench and Verification Environment for Mixed Signal SoCs

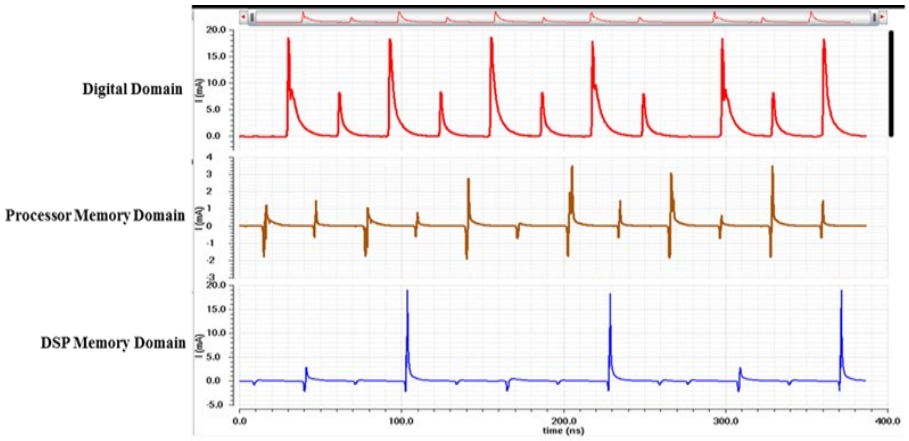
- Incisive Formal Verifier (IFV/ IEV) from Cadence was used for Formal Verification.
- Conformal Low Power used for Formal Power Intent Verification.
- Cadence's "Enterprise Planner" was used to track the verification progress. This tool supports a methodology to maintain the traceability matrix.

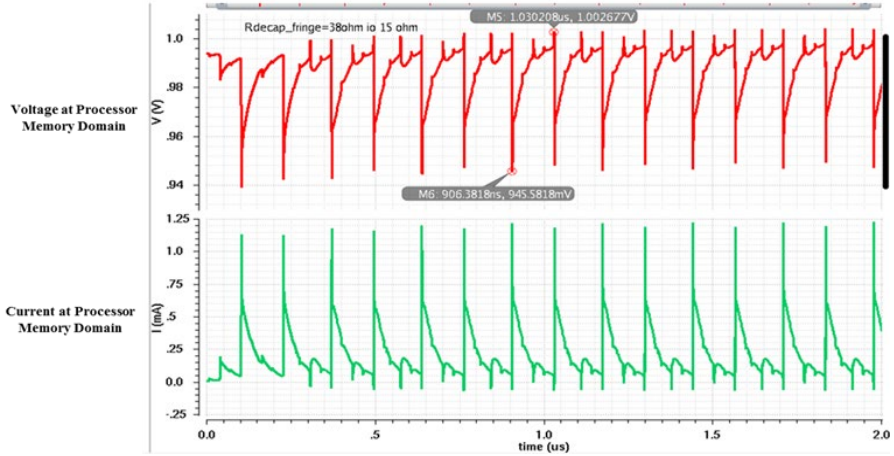
Case Study : 4
LDO Sign off Criteria

- To design a low power compact LDO an accurate model of the chip power behavior across the various operating modes is needed.
- Around 5 use-cases were identified per LDO which simulated the different modes like startup mode, idle mode, processor running at different speeds etc. on the synthesized netlist initially and finally on the back annotated clock tree inserted netlist.
- Simulation data was given to red hawk tool to generate the Chip Power Models-CPM for the above scenarios.

Case Study : 4
LDO Sign off Criteria

- These SPICE level chip power models were used in the LDO sign off simulations to finalize the design of the LDO blocks and determine the amount of de-caps to be used in the chip for every domain to ensure power integrity.
- Figure shows the SPICE simulation snapshot of peak current excursion for the digital, processor memory and DSP memory domains.





Case Study – 4

Low drop out (LDO) sign-off criteria.

- Table below outlines the peak to average current consumption ratio, which turned out to be high for the memory domain.

Domains	Peak Current (mA)	Average Current (mA)
Digital Domain	18.8	1.53
Processor Memory domain	19	0.211
DSP Memory Domain	3.51	0.0668

- The processor memory domain suffered from excessive voltage drop in these simulations. This was fixed by increasing the number of de-caps in this domain.

Conclusion

- While CPF supports classical power scenarios like always on, shut off it required changes in the environment to model the Induced Power scenario.
- Power management systems have very intricate dependencies between the analog and the digital controller. To jump start the verification we started using randomized System Verilog models then replaced it with Wreal models and finally the Verilog AMS models, thus achieving high accuracy in final sims while reducing overall verification time.
- Digital techniques like assertions and formal checks proved to be useful in the mixed signal world. Continuing along these lines we intend to evaluate UVM for future chips.
- A robust method to sign off LDO resulted in the accurate verification of power supply which is key in ensuring silicon power integrity.

Questions ?

2016 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

Thank You