

Trends in Functional Verification: A 2016 Industry Study

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ABSTRACT

In 2002 and 2004, Collett International Research, Inc. conducted its well-known ASIC/IC functional verification studies, which provided invaluable insight into design and verification trends at that point in time. However, after the 2004 study, no additional Collett studies were conducted. [1][2] Three private functional verification studies were commissioned in 2007, 2010, and 2012. Although the data from these studies has been referenced in various publications and blogs, these studies were never officially published. To address this dearth of knowledge, two new studies were commissioned in 2014 and 2016. The 2014 study was a world-wide, double-blind, functional verification study covering all electronic industry market segments. The findings from this study were published in the proceedings of the 2015 Design Automation Conference. [3] The 2016 study followed the format of the 2014 study and is the focus of this invited talk. The findings from the 2016 functional verification study provide invaluable insight into the state of today's electronics industry.

Categories and Subject Descriptors

B.6.3 [Logic Design]: Design Aids—Verification

General Terms

Design, Standardization, Languages, Verification

Keywords

Functional Verification Trends, Verification Effort

1. INTRODUCTION

This paper presents the findings from a world-wide, double-blind, functional verification study, covering all electronic industry market segments. Our study was modeled after the original 2002 and 2004 Collett International Research, Inc. studies. [1][2] In other words, we endeavored to preserve the original wording of the Collett questions whenever possible to facilitate trend analysis. To ensure anonymity, we commissioned Wilson Research Group to execute our study. The purpose of preserving anonymity was to prevent biasing the participants' responses. Furthermore, to ensure that our study would be executed as a double-blind study, the compilation and analysis of the results did not take into account the identity of the participants.

For the purpose of our study we used a multiple sampling frame approach that was constructed from eight independent lists that we acquired. This enabled us to cover all regions of the world—as well as cover all relevant electronics industry market segments. It is important to note that we decided not to include our own account team's customer list in the sampling frame. This was done in a deliberate attempt to prevent biasing the final results.

After data cleaning the results to remove inconsistent or random responses (e.g., someone who only answered “a” on all questions), the final sample size consisted of 1738 eligible participants (i.e., $n=1738$). To put this figure in perspective, the famous 2004 Ron Collett International study sample size consisted of 201 eligible participants.

Unlike the 2002 and 2004 Collett IC/ASIC functional verification studies, which were conducted only in North America (US and Canada), our study covered all regions of the world. Our study results have been compiled both globally and regionally, but for the purposes of this paper (and due to space), we are presenting only the globally compiled results. Finally, our study results cover both the ASIC/IC and FPGA market segments. However, due to space, this paper focuses only on the ASIC/IC findings. To learn about the FPGA findings from our study, visit the Verification Horizons BLOG. [4]

1.1 Confidence Interval

All surveys are subject to sampling errors. To quantify this error in probabilistic terms, we calculate a confidence interval. For example, we determined the overall margin of error for our study to be $\pm 2.36\%$ at a 95% confidence interval. In other words, this confidence interval tells us that if we were to take repeated samples of size $n=1738$ from a population, 95% of the samples would fall inside our margin of error $\pm 2.36\%$, and only 5% of the samples would fall outside.

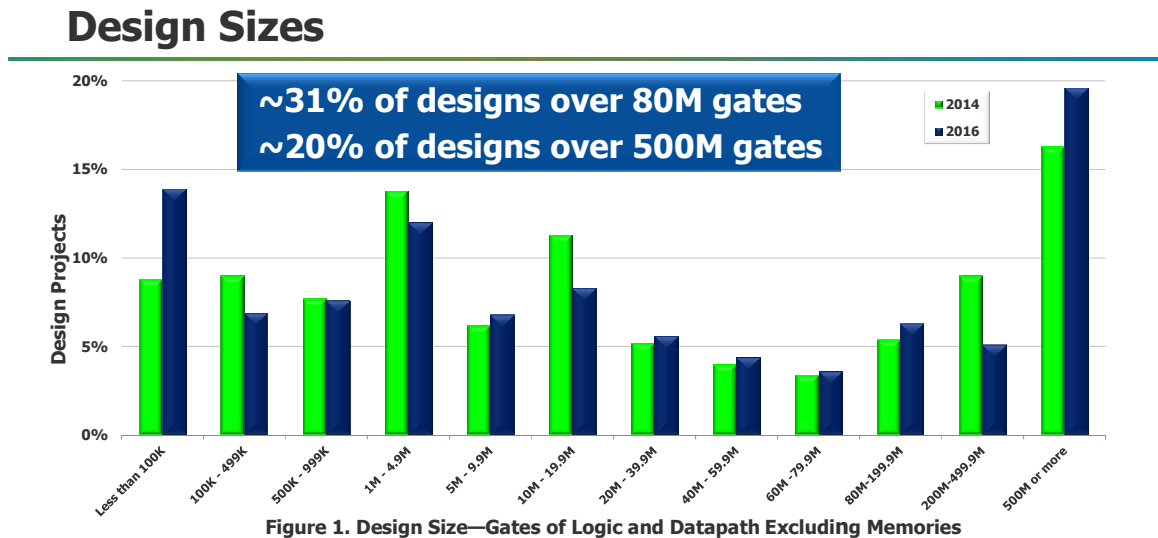
1.2 Paper Organization

The remainder of this paper is organized as follows. In Section 2, we discuss the study results specifically related to various aspects of design to illustrate growing complexity. In Section 3, we discuss trends in terms of project resources. In Section 4,

we examine verification technology adoption trends (for example, code coverage, functional coverage, assertions, constrained-random verification, formal property checking, emulation and FPGA prototyping). In addition, this section presents adoption trends for various design and verification language and methodology standards (for example, VHDL, Verilog, SystemVerilog UVM, and SVA). Section 5 focuses on verification effectiveness. In Section 6, we describe various bias concerns when conducting a large study such as ours, and then discuss what we did to address these concerns. Finally, in Section 7, we draw some conclusions from our study and discuss other aspects of the verification process that we believe need to be studied in the future.

2. DESIGN TRENDS

In this section, we present trends related to various aspects of design to illustrate growing design complexity. Figure 1 shows the trends from the 2014 and 2016 studies in terms of project participants by design sizes (gates of logic and datapath, excluding memories). The key takeaway here is that the electronic industry continues to move to larger designs. In fact, 31 percent of today’s projects are working on designs are over 80M gates, while almost 20 percent of today’s projects are working on designs are over 500M gates. What was particularly interesting in the 2016 study was the sharp increase in projects working on designs less than 100K gates. Perhaps these small designs are sensors associated with the emerging IoT market. Finally, it is important to note that Figure 1 represents projects by design size and not silicon volume in terms of production.



But increased design size is only one dimension of the growing complexity challenge. What has changed significantly in design since the original Collett studies is the dramatic movement to SoC class of designs. In 2004, Collett found that 52 percent of designs included one or more embedded processors. Our 2016 study found that the number of designs with embedded processors had increased to 72 percent. Furthermore, 49 percent of all designs today contain two or more embedded processors, while 16 percent of today’s designs include eight or more embedded processors. SoC class designs add a new layer of verification complexity to the verification process that did not exist with traditional non-SoC class designs due to hardware and software interactions, new coherency architectures, and the emergence of complex network-on-a-chip interconnect.

In addition to the increasing number of embedded processors contained within an SoC, it is not uncommon to find in the order of 150 integrated IP blocks within today’s more advanced SoCs. Many of these IP blocks have their own clocking requirements, which often present new verification challenges due to metastability issues involving signals that cross between multiple asynchronous clock domains. [5]

In Figure 2, we see that 91 percent of all designs today have two or more asynchronous clock domains, which is just slightly down from the 2012 and 2014 studies. In fact, there has not been any significant changes in the trends for the number of asynchronous clock domain since 2007 (i.e., essentially the same curve). The majority of projects are working on designs containing between two and twenty asynchronous clock domains.

One of the challenges with verifying clock domain crossing issues is that there is a class of metastability bugs that cannot be demonstrated in simulation on an RTL model. To simulate these issues requires a gate-level model with timing, which is often not available until later stages in the design flow. However, existing static clock-domain crossing (CDC) verification tools can identify clock domain issues directly on an RTL model at earlier stages in the design flow.

ASIC/IC Multiple Asynchronous Clock Domain Trends

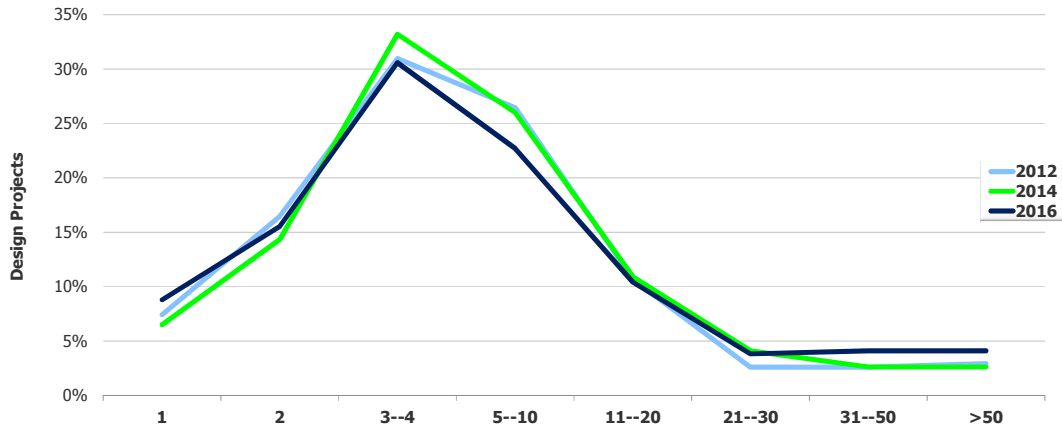


Figure 2. ASIC/IC Number of Independent Clock Domains

3. RESOURCE TRENDS

In this section we discuss the growing resource trends due to rising design complexity. Figure 3 shows the percentage of total project time spent in verification. As you would expect, the results are all over the spectrum; whereas, some projects spend less time in verification, other projects spend more. The average total project time spent in verification in 2016 was 55 percent, which did not change significantly from 2014.

ASIC/IC Verification Project Time

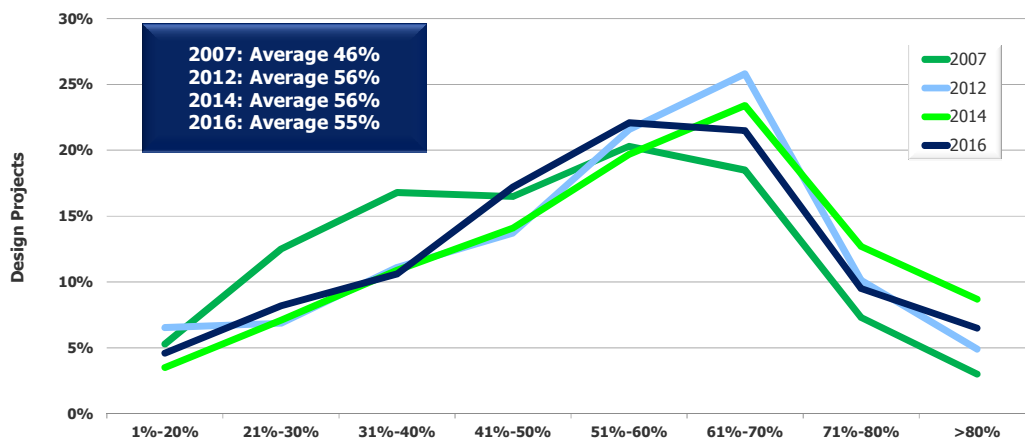


Figure 3. Percentage of ASIC/IC Project Time Spent in Verification

Perhaps one of the biggest challenges in design and verification today is identifying solutions to increase productivity and control engineering headcount. To illustrate the need for productivity improvement, we discuss the trend in terms of increasing engineering headcount. Figure 4 shows the mean peak number of engineers working on a project. Again, this is an

industry average since some projects have many engineers while other projects have few. You can see that the mean peak number of verification engineers today is greater than the mean peak number of design engineers. In other words, there are, on average, more verification engineers working on a project than design engineers. This situation has changed significantly since 2007.

Another way to comprehend the impact of today’s project headcount trends is to calculate the compounded annual growth rate (CAGR) for both design and verification engineers. Between 2007 and 2016 the industry experienced a 3.6 percent CAGR for design engineers and a 10.4 percent CAGR for verification engineers. Clearly, the double-digit increase in required verification engineers has become a major project cost-management concern, and is one indicator of growing verification effort.

More Verification Engineers vs Design Engineers

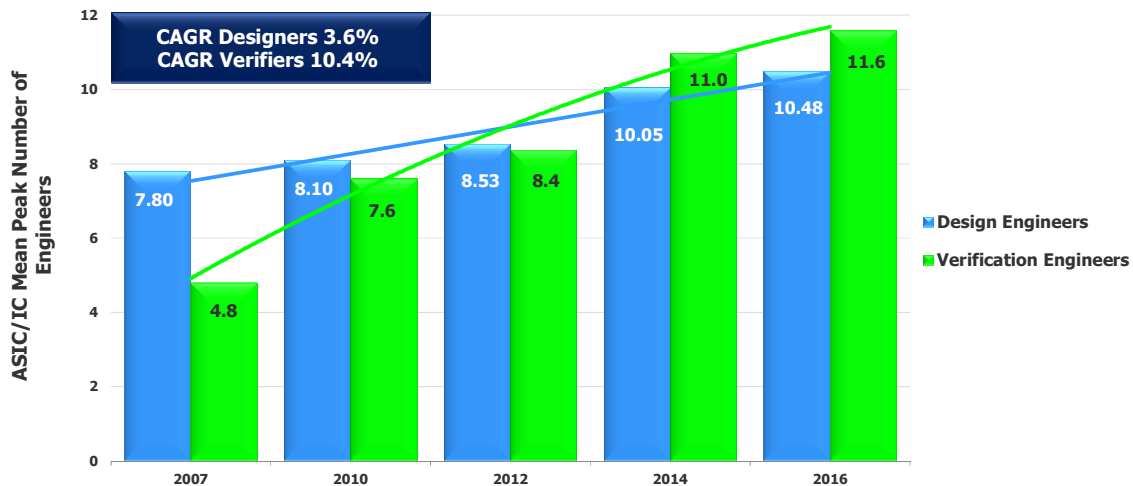


Figure 4. Mean Peak Number of Design and Verification Engineers working on a project

But verification engineers are not the only project stakeholders involved in the verification process. Design engineers spend a significant amount of their time in verification too, as shown in Figure 5. In 2016, design engineers spent slightly more time in design activities, yet still a significant amount of time involved in verification.

Where ASIC/IC Designers Spend Their Time

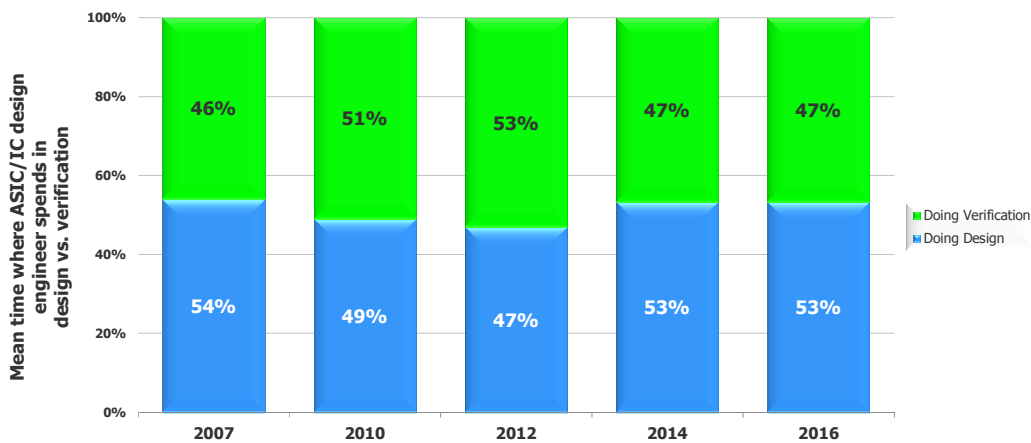


Figure 5. Where Design Engineers Spend Their Time

However, this is a reversal in the trends observed from the 2010 and 2012 studies, which indicated that design engineers spent more time in verification activities than design activities. The data suggest that design effort has risen since 2012 when you take into account that: (a) design engineers are spending more time in design, and (b) there was a nine percent CAGR in required design engineers between 2012 and 2014 (shown in Figure 4), which is a steeper increase than the overall 3.6 CAGR for design engineers spanning 2007 through 2016. The data from our study suggest that implementing low-power features into the design might be contributing to this increased design effort.

Figure 6 shows where verification engineers spend their time (on average). We do not show trends here since this aspect of project resources was not studied prior to 2012, and there were no significant changes in the results between 2012, 2014 and 2016.

Our study found that verification engineers spend more of their time in debugging than any other activity. This needs to be an important research area whose future solutions will be necessary for improving productivity and predictability within a project.

Where ASIC/IC Verification Engineers Spend Their Time

2016 Where ASIC/IC Verification Engineers Spend Their Time

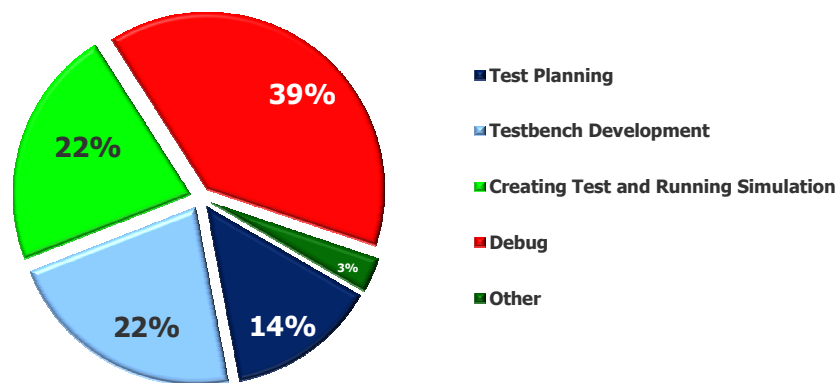


Figure 6. Where Verification Engineers Spend Their Time

4. VERIFICATION SOLUTION TRENDS

In this section we examine various dynamic verification technology adoption trends.

4.1 Dynamic Verification Techniques

Figure 7 shows the adoption trends for various simulation-based techniques from 2007 through 2016, which include code coverage, assertions, functional coverage, and constrained-random simulation.

One observation from these adoption trends is that the electronic design industry has matured its verification processes since 2007. This maturity is likely due to the growing complexity of designs as discussed in the previous section. Another observation is that code coverage and constrained-random simulation adoptions appeared to have declined. However, the results have been skewed due to the increased number in projects working on designs less than 100K. In general, projects working on smaller designs are less mature in their verification processes. Taking this into account, it appears that the adoption for all the techniques list in Figure 7 has leveled off. This trend is likely due to the scaling limitations of simulation when applying these techniques. That is, these techniques generally works well at the IP block or subsystem level of simulation, but generally become less effective at the full SoC integration level for large designs.

4.2 Static Verification Techniques

Figure 8 shows the adoption trends for formal property checking (e.g., model checking), as well as automatic formal applications (e.g., SoC integration connectivity checking, deadlock detection, X semantic safety checks, coverage reachability analysis, and many other properties that can be automatically extracted and then formally proven). Formal property checking traditionally has been a high-effort process requiring specialized skills and expertise. However, the recent emergence of automatic formal applications provides narrowly focused solutions and does not require specialized skills to adopt. While formal property checking adoption experienced incremental growth between 2012 and 2014, the adoption of automatic formal applications increased by 62 percent. Yet, in 2016 formal property checking experienced a 31 percent growth. One

observation is that many projects which have experienced benefits with the adoption of automatic formal applications are now maturing their formal skills by adopting formal property checking. In general, formal solutions (i.e., formal property checking combined with automatic formal applications) are one of the fastest growing segments in functional verification.

ASIC/IC Dynamic Verification Adoption Trends

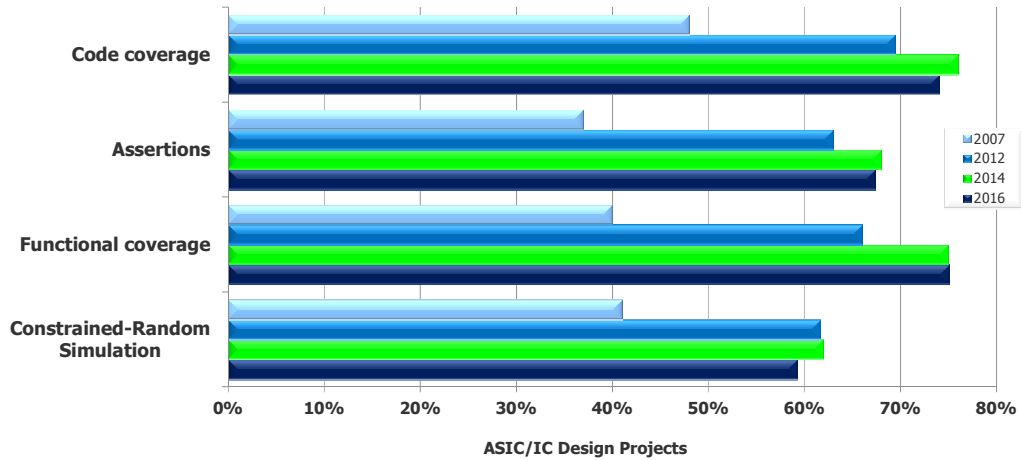


Figure 7. Dynamic Verification Adoption Trends

ASIC/IC Formal Technology Adoption Trends

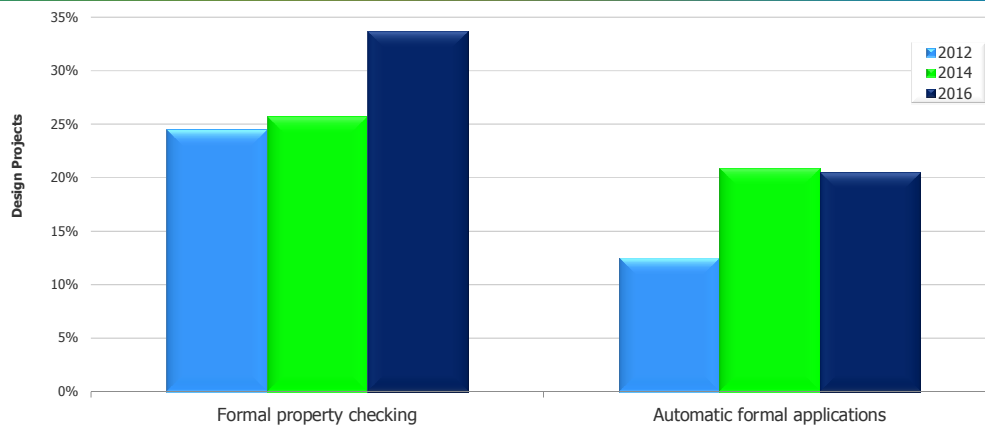


Figure 8. Formal Technology Adoption Trends

4.3 Emulation and FPGA Prototyping

Historically, the simulation market has depended on processor frequency scaling as one means of continual improvement in simulation performance. However, as processor frequency scaling levels off, simulation-based techniques are unable to keep up with today’s growing complexity. This is particularly true when simulating large designs that include both software and embedded processor core models. Hence, acceleration techniques are now required to extend verification performance for very large designs. In fact, emulation and FPGA prototyping have become key platforms for SoC integration verification where both hardware and software are integrated into a system for the first time. In addition to SoC verification, emulation and FPGA prototyping are also used today as a platform for software development.

Today, 24 percent of the projects from our study have adopted emulation, while about 30 percent of the projects have adopted FPGA prototyping. Figure 9 describes various objectives for adopting emulation, while Figure 10 describes various objectives for adopting FPGA prototyping. You might note that the results do not sum to 100 percent since multiple answers were accepted from each study participant. One observation is that the percentage is different between the two graphs, yet the order

for the objective adoption (from least common reason to most) is the same between emulation and FPGA prototyping. In other words, other than performance reasons, there is not a significant difference in the objective for using emulation nor FPGA prototyping. Finally, between 2014 and 2016 there was a significant increase in the use of emulation for IP development and verification, while there was an increase in the use of FPGA Prototyping for system validation.

Why was Emulation Performed?

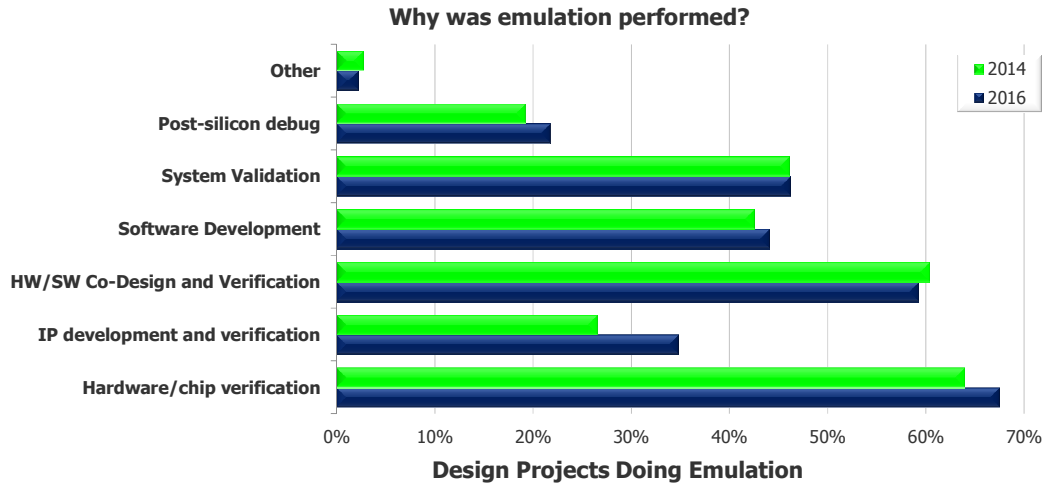


Figure 9. Why Was Emulation Used?

Why was FPGA Prototyping Performed?

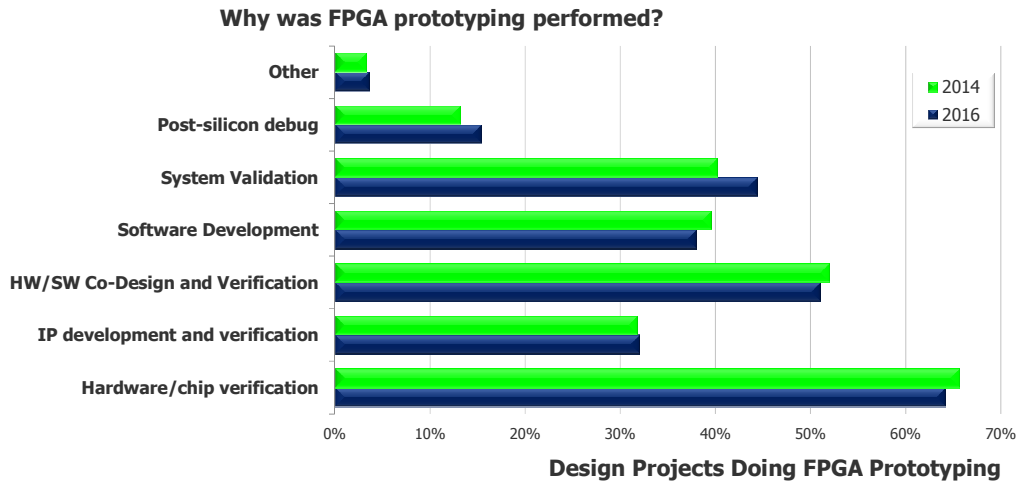


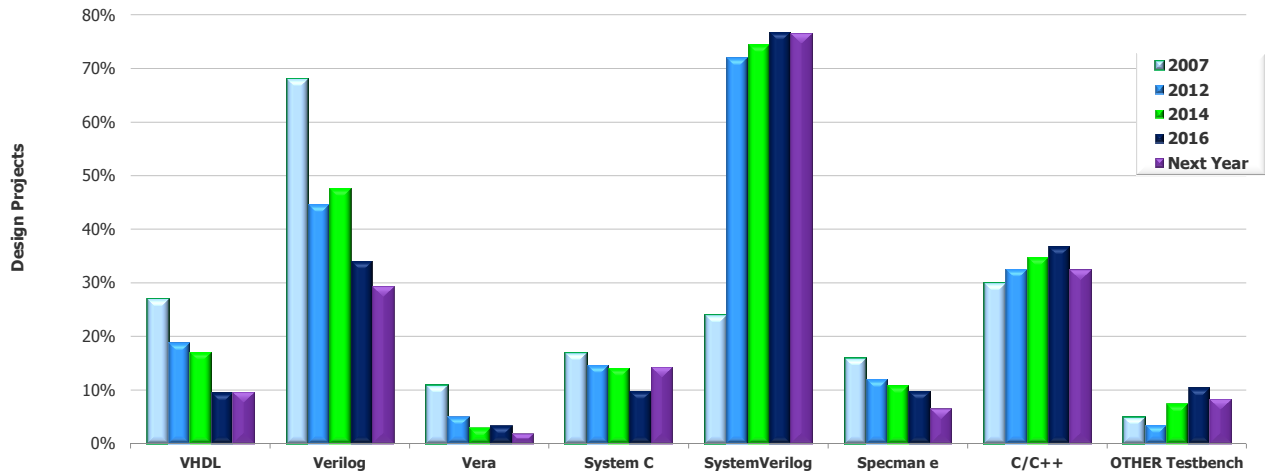
Figure 10. Why Was FPGA Prototyping Used?

4.4 Verification Languages and Libraries

In this section, we present the adoption trends for verification language and base-class libraries. As previously noted, the reason some of the results sum to more than 100 percent is that some projects are using multiple languages; thus, individual participants can have multiple answers.

Figure 11 shows the adoption trends for languages used to create testbenches. Essentially, the adoption rates for all languages used to create testbenches are either declining or flat, with the exception of SystemVerilog. Nonetheless, the data suggest that SystemVerilog adoption is starting to saturate or level off at about 75 percent.

ASIC/IC Verification Language Adoption Trends

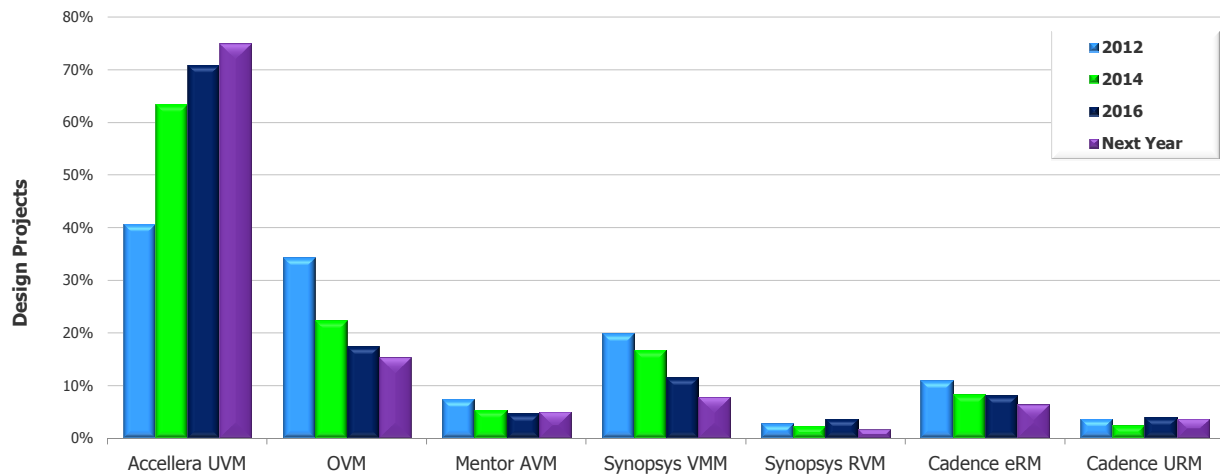


* Multiple answers possible

Figure 11. Languages Used for Verification (Testbenches)

Figure 12 shows the adoption trends for various testbench methodologies built using class libraries. Here we see a decline in adoption of all methodologies and class libraries with the exception of Accellera’s UVM¹, whose adoption increased by 54 percent between 2012 and 2014, and an additional 13 percent between 2014 and 2016. Furthermore, our study revealed that UVM is projected to grow an additional 6 percent within the next year.

ASIC/IC Testbench Methodology Adoption Trends



* Multiple answers possible

Figure 12. Methodologies and Testbench Base-Class Libraries

¹ Universal Verification Methodology (UVM) is a standard to enable efficient development and reuse of verification environments and verification IP (VIP) throughout the electronics industry. Accellera provides both an API standard for UVM and a reference implementation. That reference implementation is a class library defined using the syntax and semantics of SystemVerilog (IEEE 1800).

Figure 13 shows the industry adoption trends for various assertion languages, and again, SystemVerilog Assertions seems to have saturated or leveled off.

ASIC/IC Assertion Language Adoption

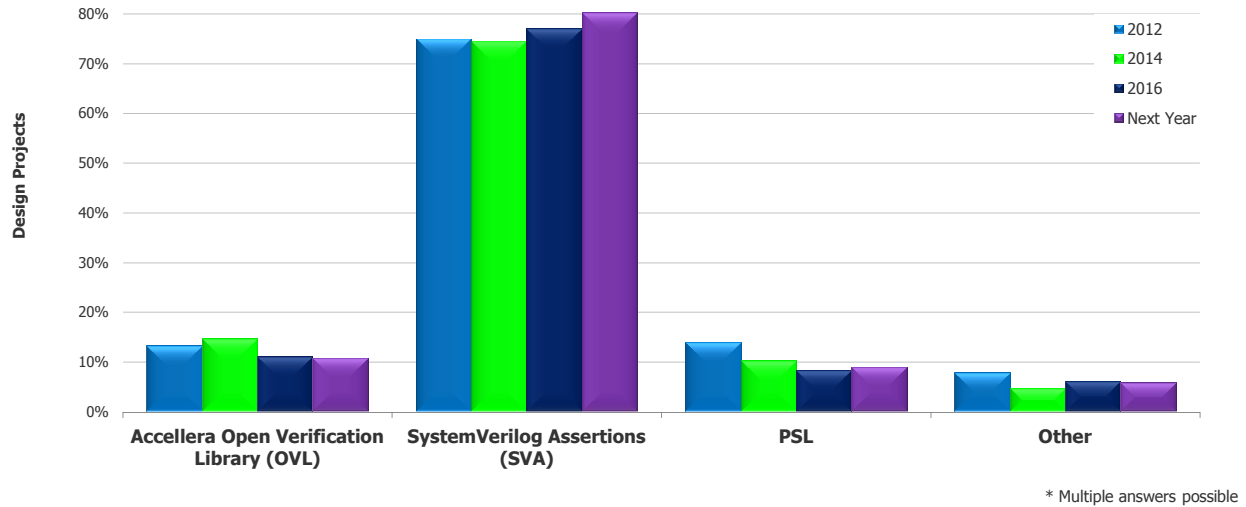


Figure 13. Assertion Language Adoption

5. VERIFICATION RESULTS

In section 3, we provided data that suggest a significant amount of effort is being applied to functional verification. An important question the various studies have tried to answer is whether this increasing effort is paying off. In this section, we present verification results findings in terms of schedules, number of required spins, and classification of functional bugs.

ASIC/IC Completion to Original Schedule

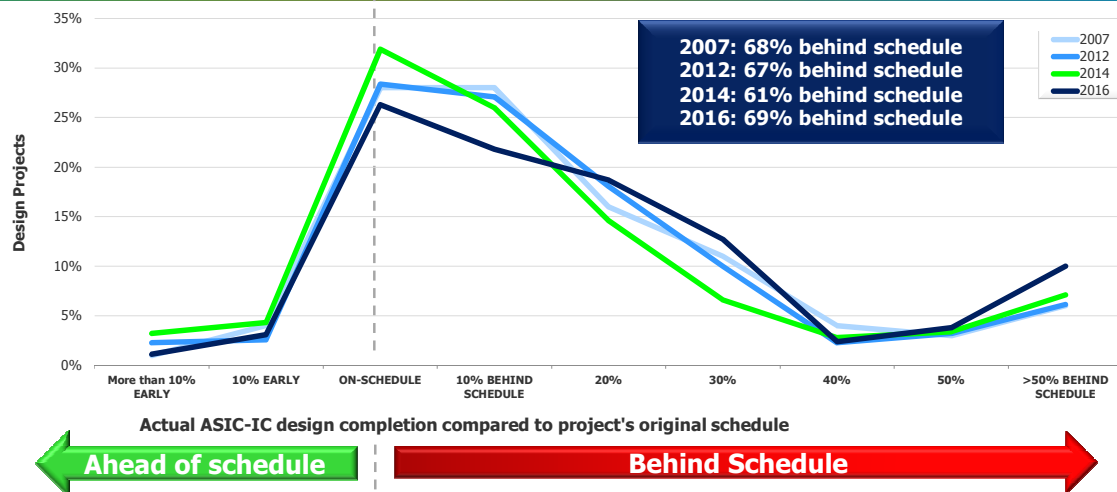


Figure 14. Design Completion Compared to Original Schedule

Figure 14 presents the design completion time compared to the project's original schedule. The data suggest that in 2014 there was a slight improvement in projects meeting their original schedule; where in the 2007, 2012 and 2016 studies about 68 percent of the projects were behind scheduled, compared to 61 percent in 2014. It is unclear if this improvement was due to

the industry becoming more conservative in project planning or simply better at scheduling—or an anomaly with the 2014 study. Regardless, meeting the originally planned schedule is still a challenge for most of the industry.

Number of Required ASIC/IC Spins Before Production

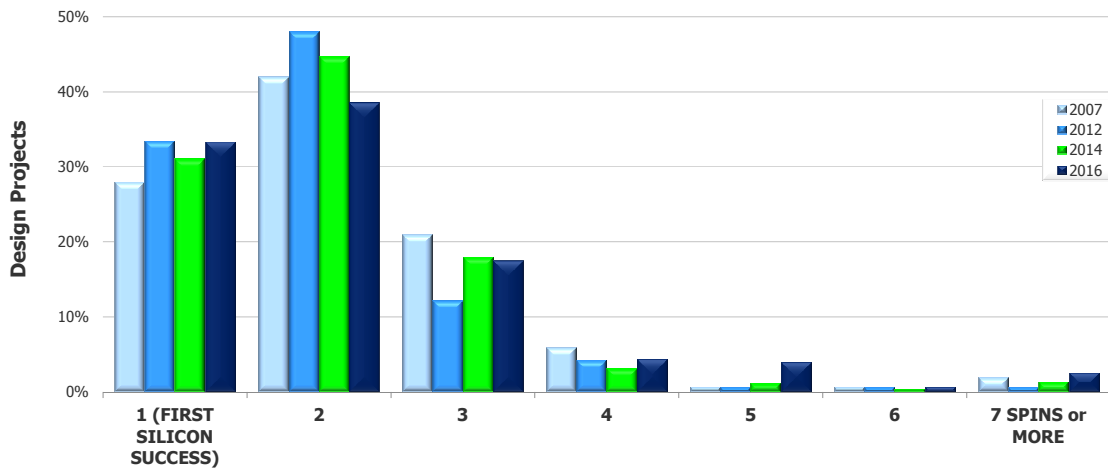


Figure 15. Number of Required Spins

Other results trends worth examining relate to the number of spins required between the start of a project and final production. Figure 15 shows this industry trend from 2007 through 2016. Even though designs have increased in complexity, the data suggest that projects are not getting any worse in terms of the number of required spins before production. Still, only about 30 percent of today’s projects are able to achieve first silicon success. Another concern is the downward trend in achieving second silicon success.

Number of FPGA Bug Escapes to Production

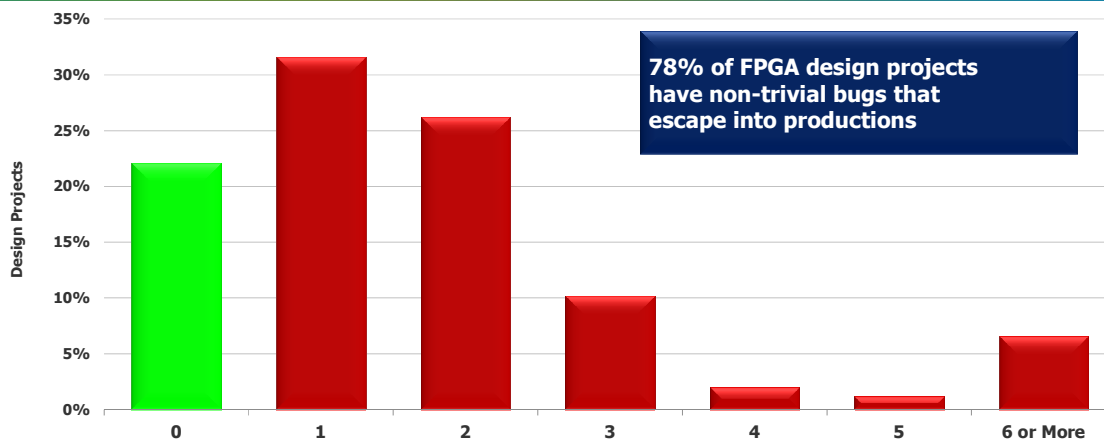


Figure 16. FPGA Non-Trivial Bug Escapes to Production

The number of required spins that occur prior to market production can be a useful metric for determining the overall verification effectiveness of an ASIC/IC project’s verification process. Unfortunately, we lack such a metric for FPGA projects. Although the focus of this paper is on the ASIC/IC findings from our study, we have decided to share our findings related to a new question we asked with the goal of assessing the effectiveness of an FPGA project’s verification/validation process. That is, how many non-trivial bugs escaped into production and were found in the field? The results were surprising

and are presented in Figure 16. Only 22 percent of today’s FPGA design projects are able to produce designs without a non-trivial bug escaping into the final product. For many market segments (such as mil-aero or large network routers) the cost of upgrading the FPGA in the field can be huge since this requires a complete revalidation of the system.

Figure 17 shows various categories of flaws that are contributing to respins. Again, you might note that the sum is greater than 100 percent on this graph, which is a result of multiple flaws triggering a respin.

Flaws Contributing to ASIC/IC Respins

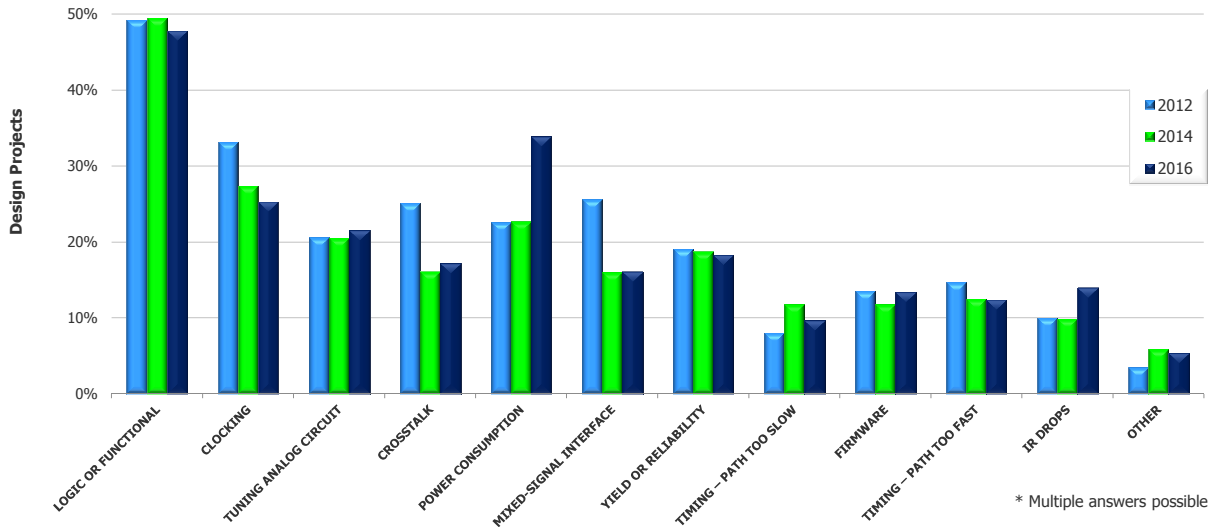


Figure 17. Trends in Types of Flaws Resulting in Respins

Logic and functional flaws remain the leading causes of respins. In addition, the 2016 findings suggest there was a spike in power consumption and IR drop issues.

Root Cause of ASIC/IC Functional Flaws

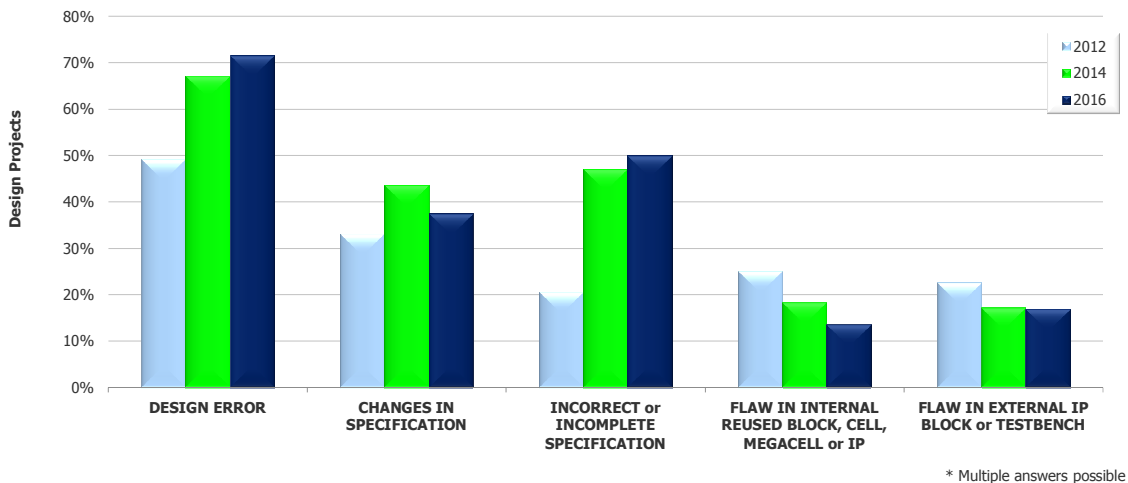


Figure 18. Root Cause of Functional Flaws

Figure 18 examines the root cause of logical or functional flaws (previously identified in Figure 17) by various categories. The data suggest design errors are the leading cause of functional flaws, and the situation is worsening. In addition, problems

associated with changing, incorrect, and incomplete specifications are a common theme often voiced by many verification engineers and project managers.

Root Cause of ASIC/IC Functional Flaws

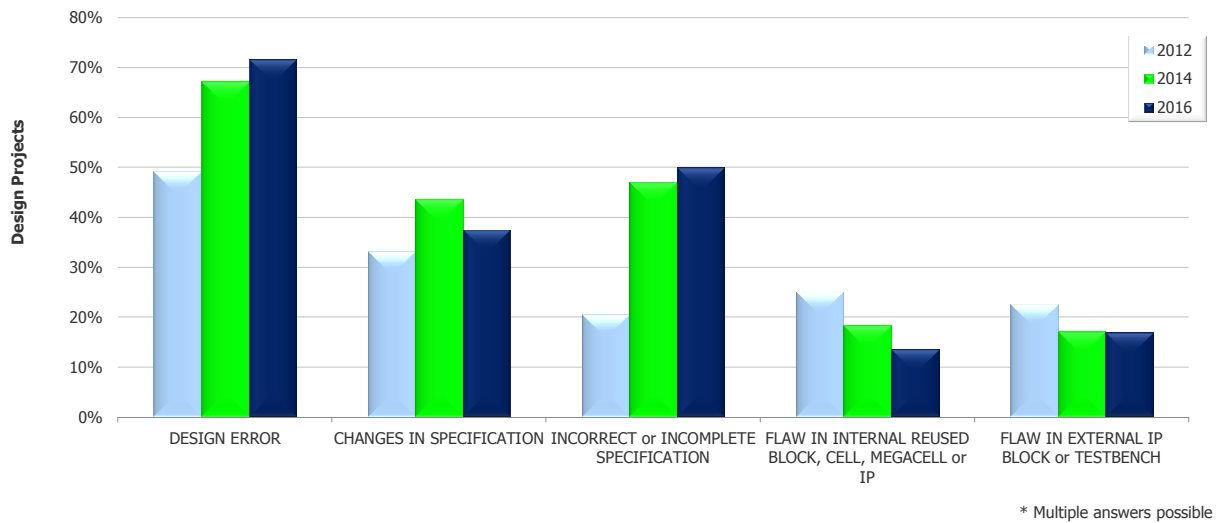


Figure 18. Root Cause of Functional Flaws

6. MINIMIZING STUDY BIAS

When architecting a study, three main concerns must be addressed to ensure valid results: *sample validity bias*, *non-response bias*, and *stakeholder bias*. Each of these concerns is discussed in the following sections, as well as the steps we took to minimize these bias concerns.

6.1 Sample Validity Bias

To ensure that a study is unbiased, it's critical that every member of a studied population have an equal chance of participating. An example of a biased study would be when a technical conference surveys its participants. The data might raise some interesting questions, but unfortunately, it does not represent members of the population that were unable to participate in the conference. The same bias can occur if a journal or online publication limits its surveys to only its subscribers.

A classic example of sample validity bias is the famous Literary Digest poll in the 1936 United States presidential election, where the magazine surveyed over two million people. This was a huge study for this period in time. The sampling frame of the study was chosen from the magazine's subscriber list, phone books, and car registrations. However, the problem with this approach was that the study did not represent the actual voter population since it was a luxury to have a subscription to a magazine, or a phone, or a car during The Great Depression. As a result of this biased sample, the poll inaccurately predicted that Republican Alf Landon versus the Democrat Franklin Roosevelt would win the 1936 presidential election.

For our study, we carefully chose a broad set of independent lists that, when combined, represented all regions of the world and all electronic design market segments. We reviewed the participant results in terms of market segments to ensure no segment or region representation was inadvertently excluded or under-represented.

6.2 Non-Response Bias

Non-response bias in a study occurs when a randomly sampled individual cannot be contacted or refuses to participate in a survey. For example, spam and unsolicited mail filters remove an individual from the possibility of receiving an invitation to participate in a study, which can bias results. It is important to validate sufficient responses occurred across all lists that make up the sample frame. Hence, we reviewed the final results to ensure that no single list of respondents that made up the sample frame dominated the final results.

Another potential non-response bias is due to lack of language translation, which we learned during our 2012 study. The 2012 study generally had good representation from all regions of the world, with the exception of an initially very poor level of participation from Japan. To solve this problem, we took two actions:

1. We translated both the invitation and the survey into Japanese.
2. We acquired additional engineering lists directly from Japan to augment our existing survey invitation list.

This resulted in a balanced representation from Japan. Based on that experience, we took the same approach to solve the language problem for the 2014 and 2016 study.

6.3 Stakeholder Bias

Stakeholder bias occurs when someone who has a vested interest in survey results can complete an online study survey multiple times and urge others to complete the survey in order to influence the results. To address this problem, a special code was generated for each study participation invitation that was sent out. The code could only be used once to fill out the survey questions, preventing someone from taking the study multiple times or sharing the invitation with someone else.

6.4 2010 Study Bias

While architecting the 2012 study, we did discover a non-response bias associated with the 2010 study. Although multiple lists across multiple market segments and across multiple regions of the world were used during the 2010 study, we discovered that a single list dominated the responses, which consisted of participants who worked on more advanced projects and whose functional verification processes tend to be mature. Hence, for this paper we have decided not to publish any of the 2010 results as part of verification technology adoption trend analysis. However, we did include the 2010 data in mean number of peak engineers per project analysis, shown in Figure 4, and the percentage of time a design engineers spends in design versus verification, shown in Figure 5—and the reader can ignore the 2010 results in these two data points if they choose.

The 2007, 2012, 2014, and 2016 studies were well balanced and did not exhibit the non-response bias previously described for the 2010 data. Hence, we have confidence in talking about general industry trends presented in this paper.

7. CONCLUSION

This paper presents the findings from a recent world-wide, double-blind, functional verification study, covering all electronic industry market segments. To our knowledge, this is the largest functional verification study that quantitatively provides insight into today's functional verification process in terms of verification technology adoption, effort, and effectiveness.

The data our study reveals is certainly of value, but it does not represent all challenges associated with SoC design (such as SoC integration verification and system validation).² In fact, many of the techniques used for block and subsystem verification that we studied do not scale well to the SoC integration and system-level validation space (e.g., constrained-random, functional coverage, and general formal property checking). In addition, our study does not encompass ESL or virtual prototyping. We believe that future studies should be expanded to include these emerging challenges.

Finally, we believe that the benefit from an industry study is not necessarily the quantitative values that the answers reveal but the new questions they raise and the healthy dialogue that ensues.

8. ACKNOWLEDGMENTS

The authors would like to thank Larry and Zachary Wilson (from Wilson Research Group), and Merlyn Brunken (from Mentor Graphics Corporation) for their expertise and guidance in conducting very large industry studies.

9. REFERENCES

- [1] R. Collett, "2002 IC/ASIC functional verification study," Industry Report from Collett International Research, Inc. 2003.
- [2] R. Collett, "2004 IC/ASIC functional verification study," Industry Report from Collett International Research, Inc. 2005.
- [3] H. Foster, *Trends in functional verification: A 2014 industry study*. In the Proceedings of the 2015 Design Automation Conference: 48:1-48:6
- [4] H. Foster, (2016, August, 8), *Prologue: The 2016 Wilson Research Group Functional Verification Study*. Retrieved from <http://go.mentor.com/4Qa1S>
- [5] R. Ginosar, "Metastability and Synchronizers: A Tutorial," IEEE Design & Test, Issue No.05 - Sept/Oct (2011 vol.28)

² Due to space limitation, we have decided not to present power management verification trends from our study in this paper. This data has been published in our Verification Horizons BLOG. [4]