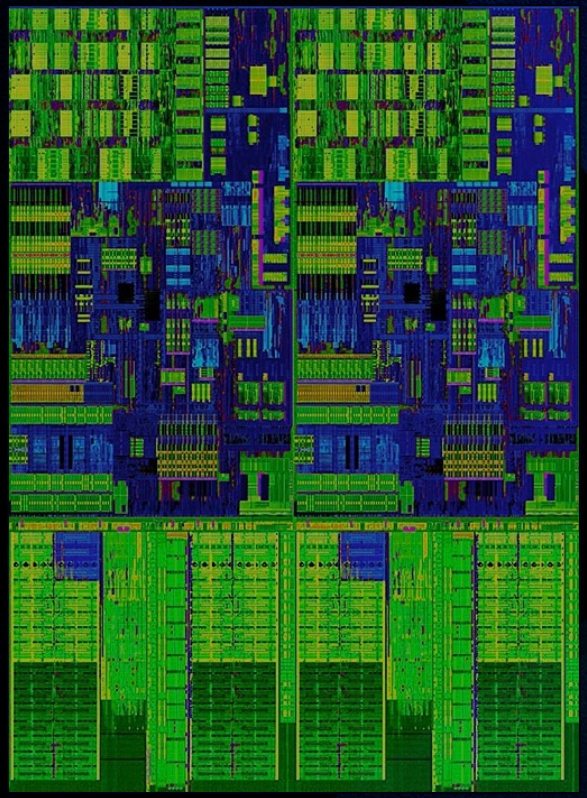


Trends in Functional Verification:
A 2016 Industry Study

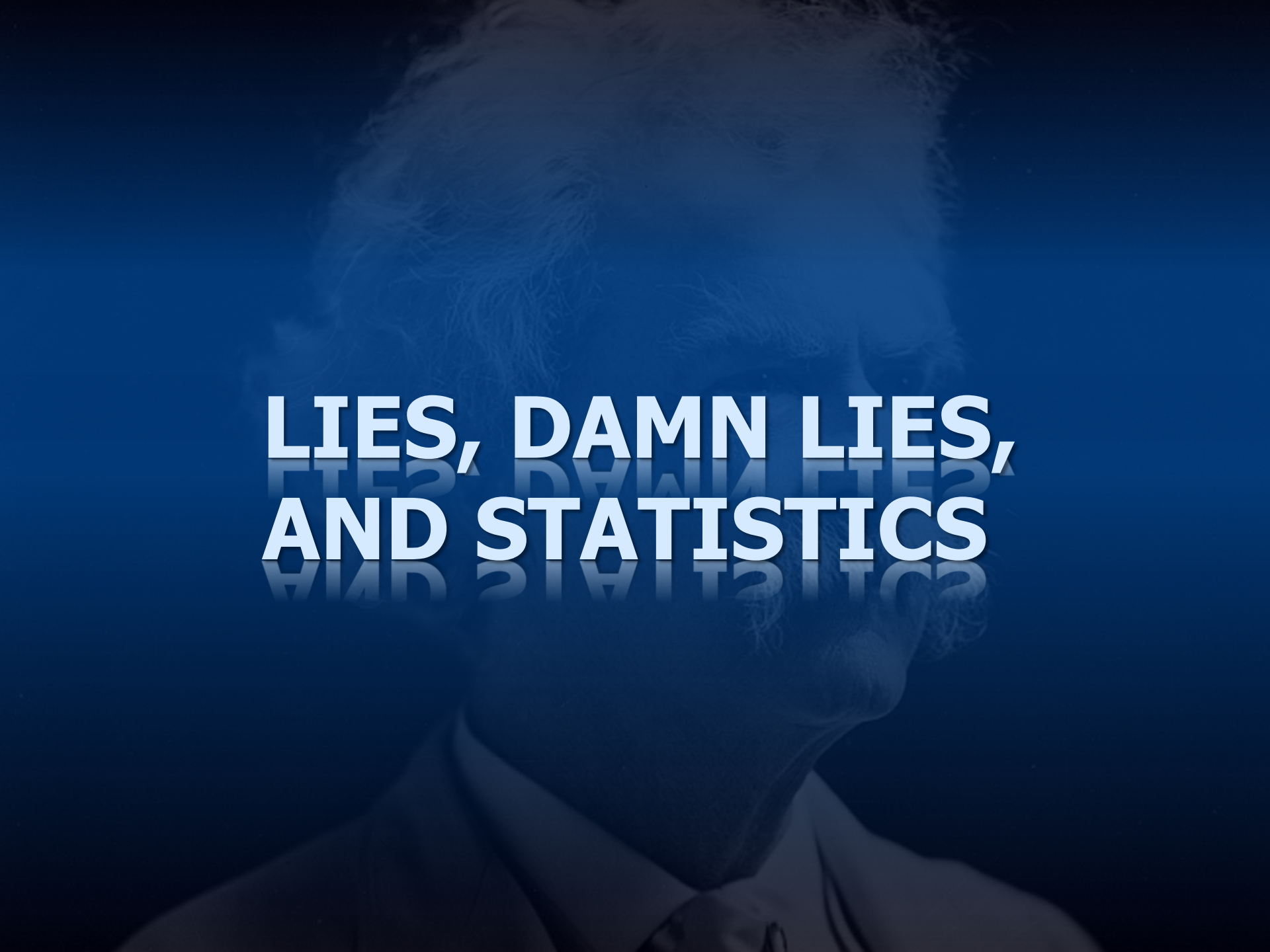
Invited Talk

Harry D Foster
Chief Scientist Verification
Mentor Graphics Corp

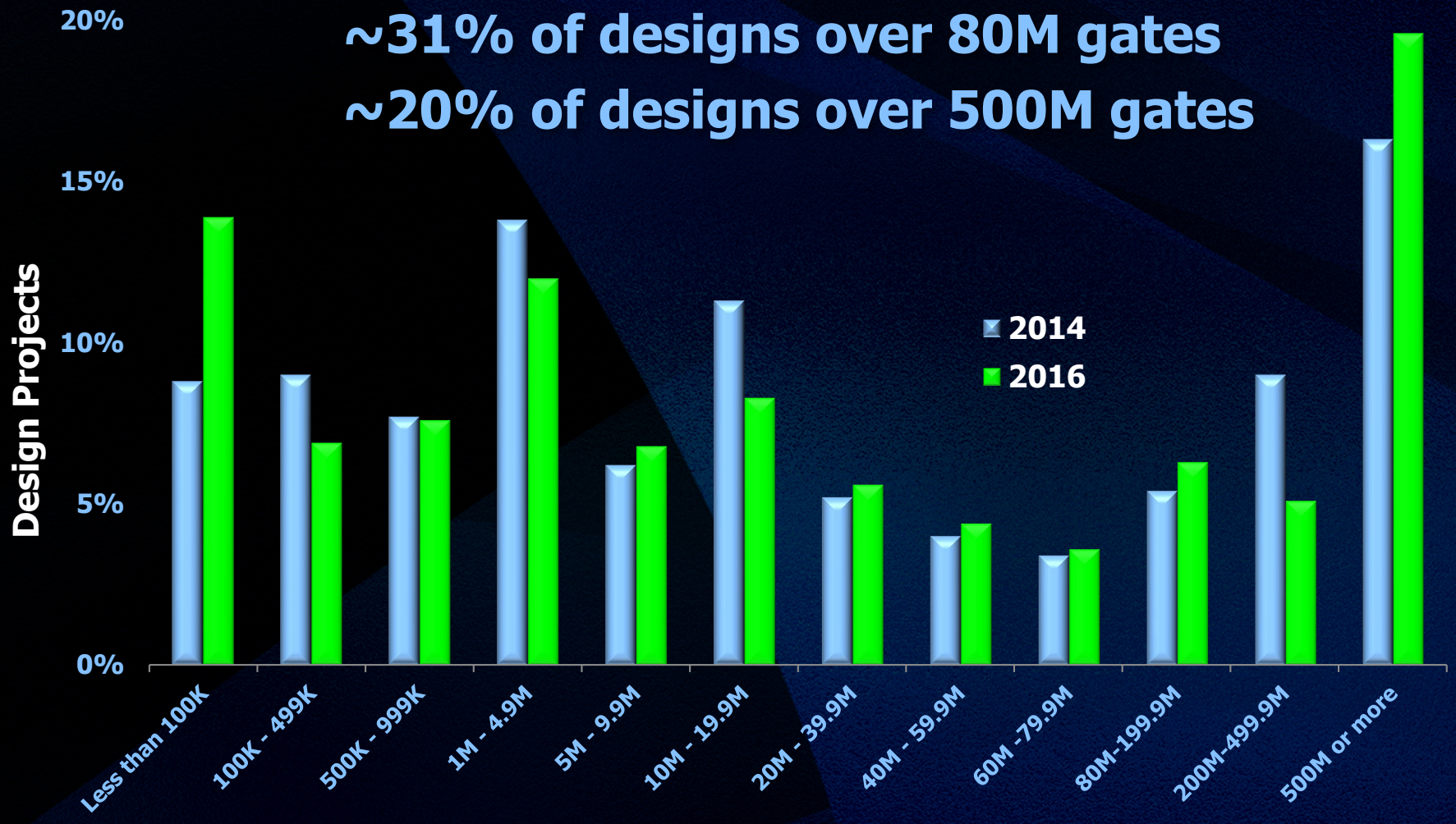
February 28, 2017

2017 DESIGN AND VERIFICATION DVCON CONFERENCE AND EXHIBITION UNITED STATES

Mentor Graphics®


LIES, DAMN LIES,
AND STATISTICS

Design Size by Projects

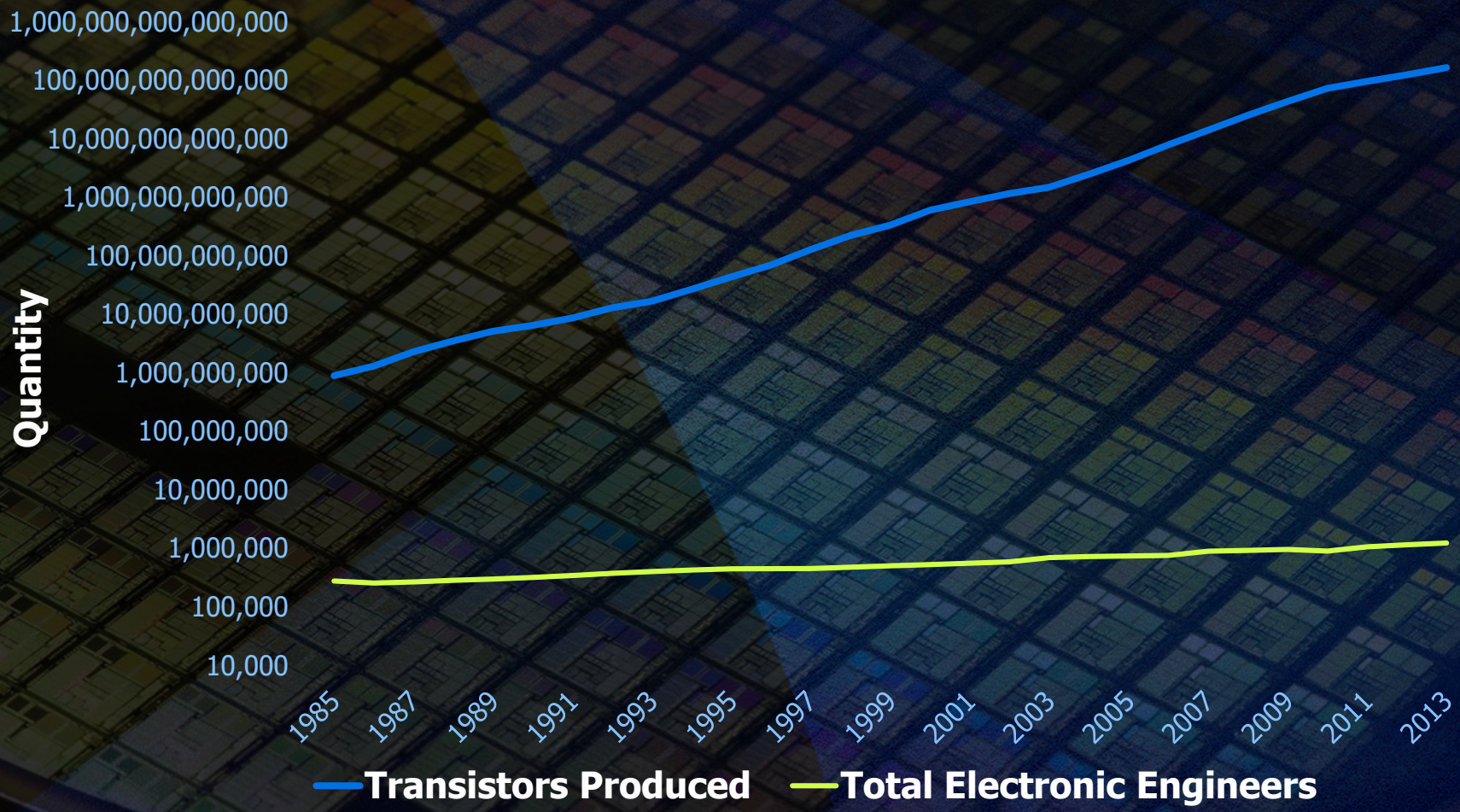


Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Study Background

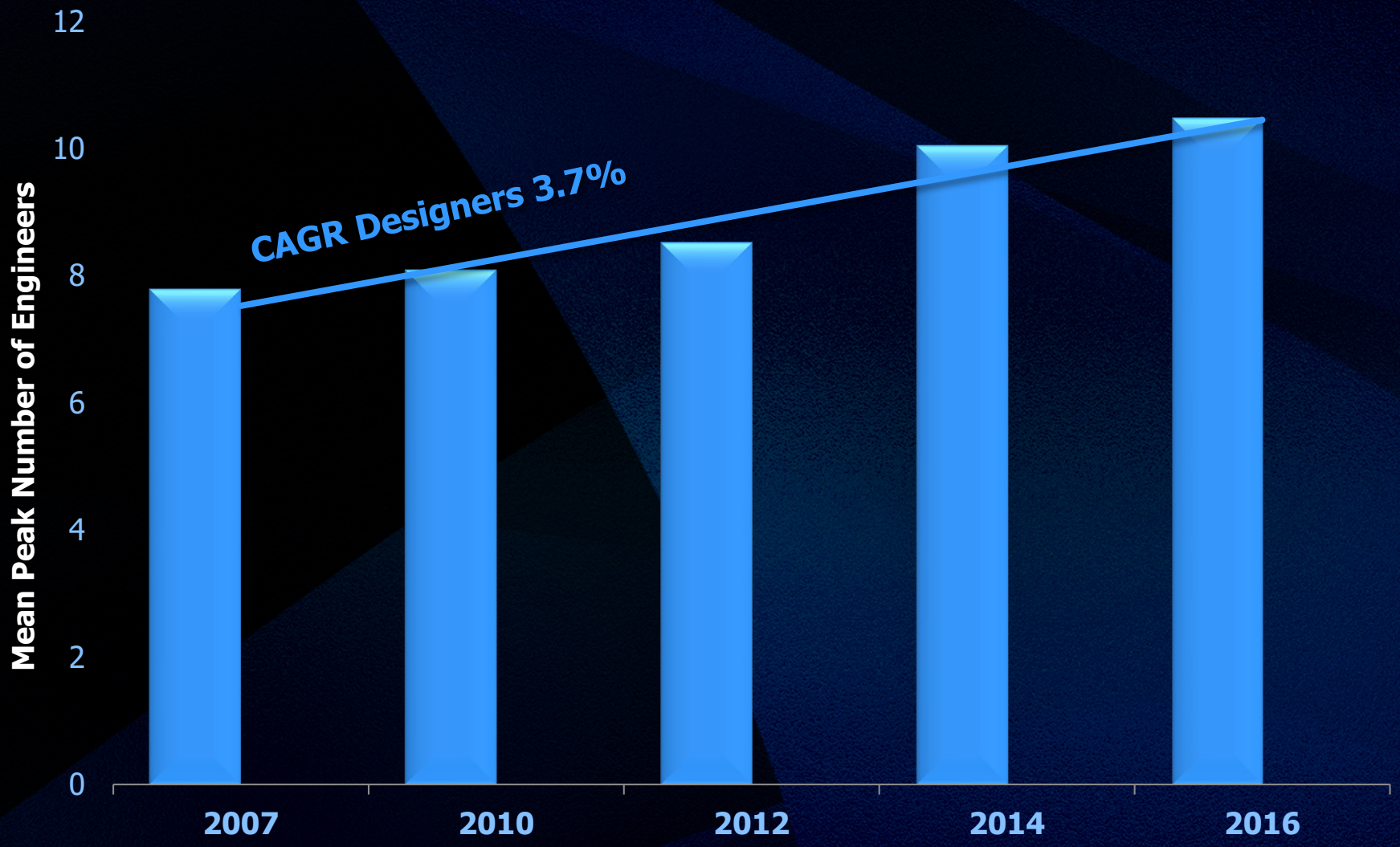
- Worldwide study
  - North America, India/China, Japan, Rest of World
- Sample frame consisted of 1738 participants
  - **8%** smaller than our 2014 study (1886)
  - **3.3x** larger than our 2012 study
  - **9.4x** larger than the 2004 Collett International study
- Confidence interval 95%
  - **±2.36%** Margin of Error

Design Productivity Grew 5 Orders of Magnitude Since 1985



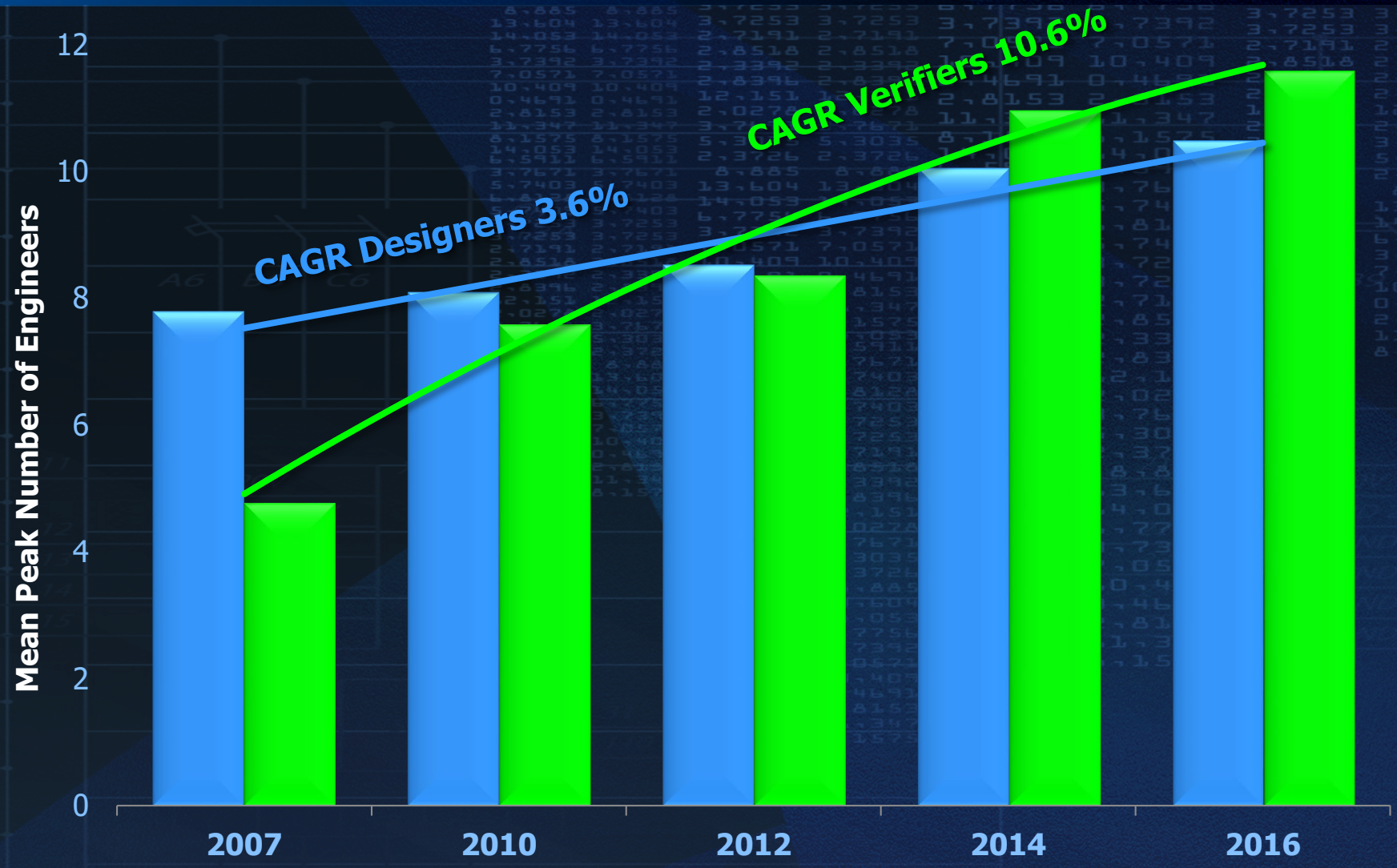
Source: Technology Research Group – EDA Database, 1986, EDA TAM, 1989 & Gartner/Dataquest 2005 Seat Count Report, Gary Smith EDA, 2013 Seat Count Analysis, VLSI Research, 2013 - Transistors Produced Analysis

Demand for Design Engineers Grows Slowly

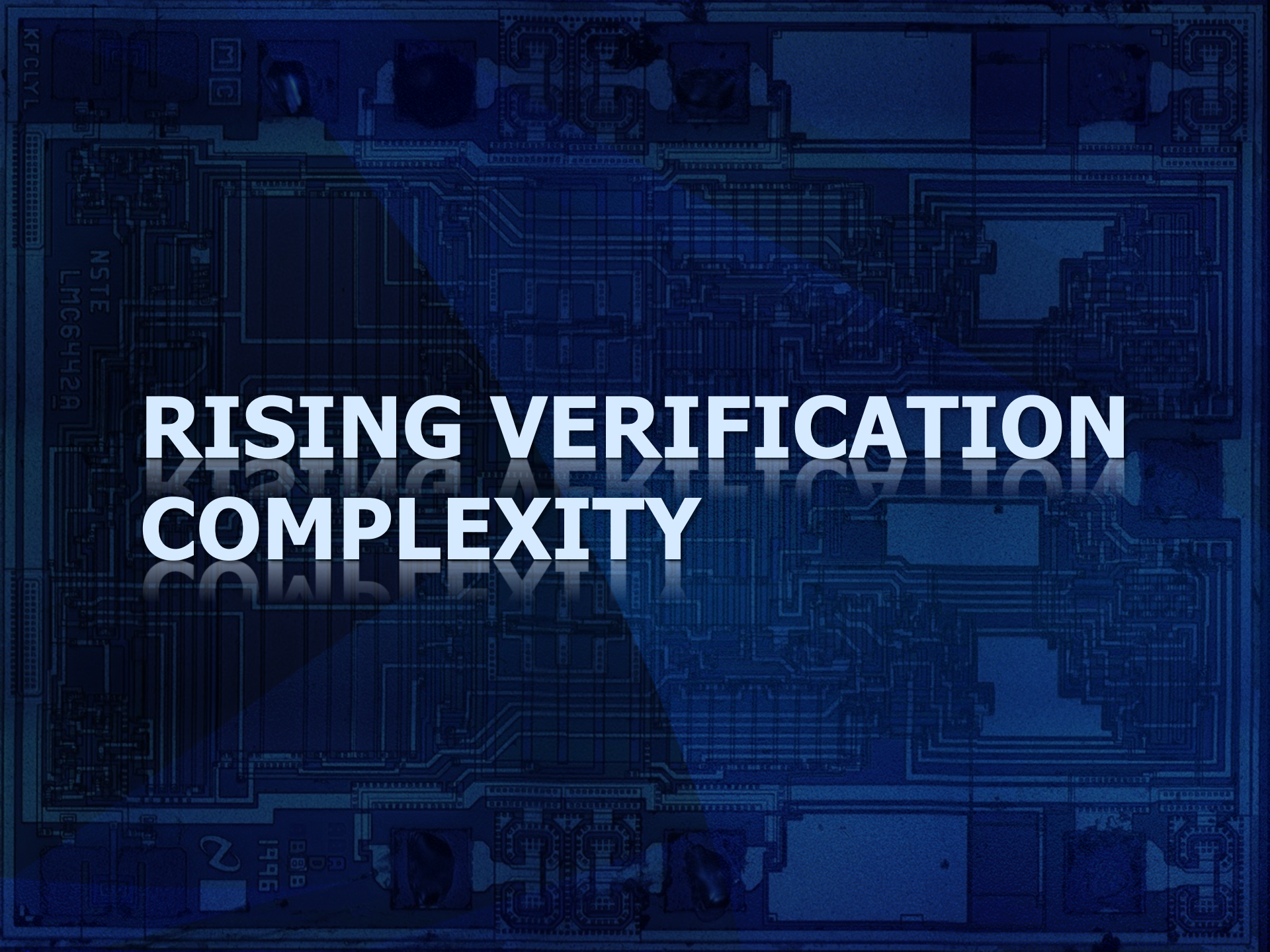


Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Demand for Verification Engineers 3X Designers

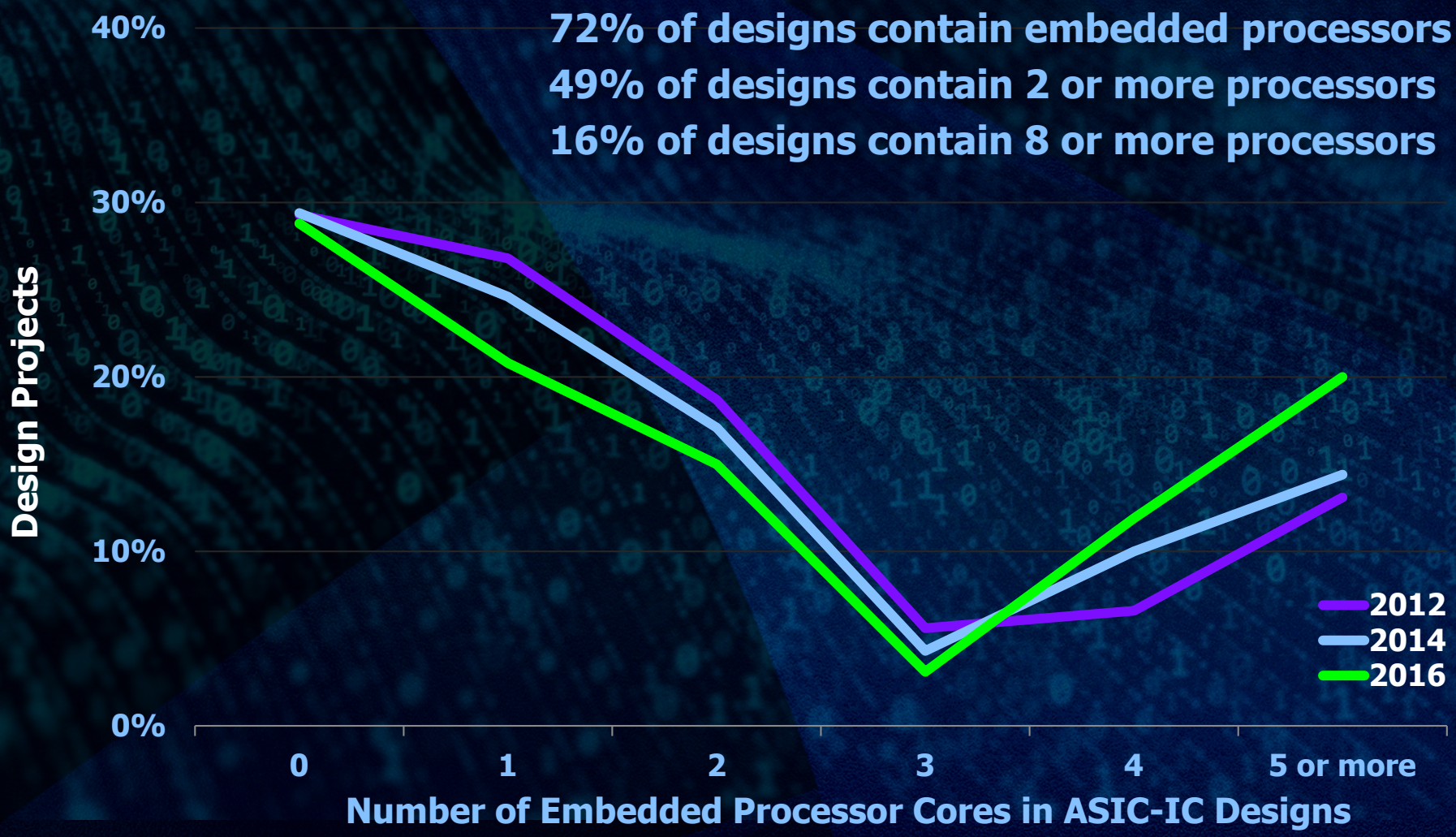


Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study


RISING VERIFICATION
COMPLEXITY

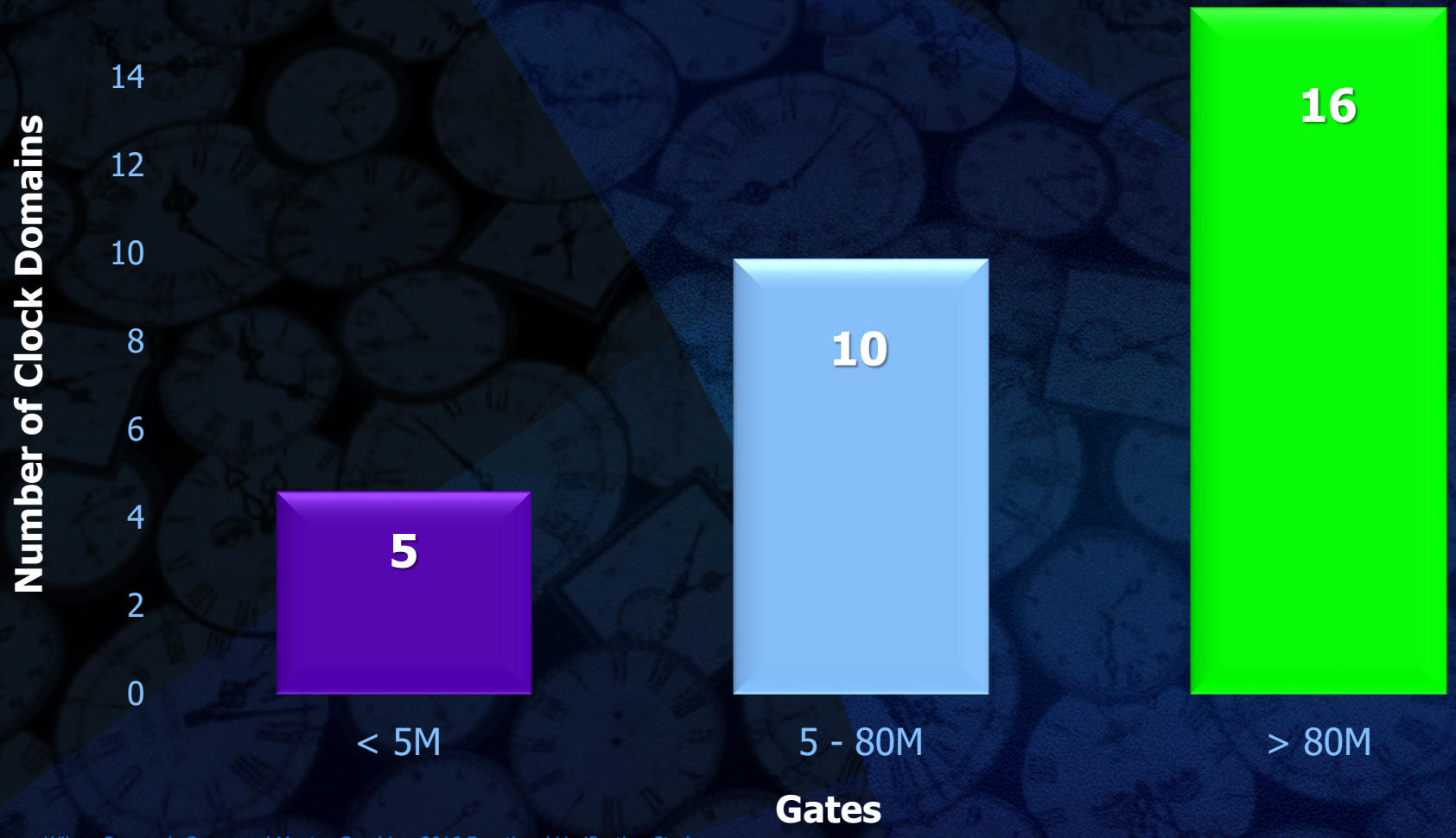
Emergence of New Verification Requirements

It's an SoC World



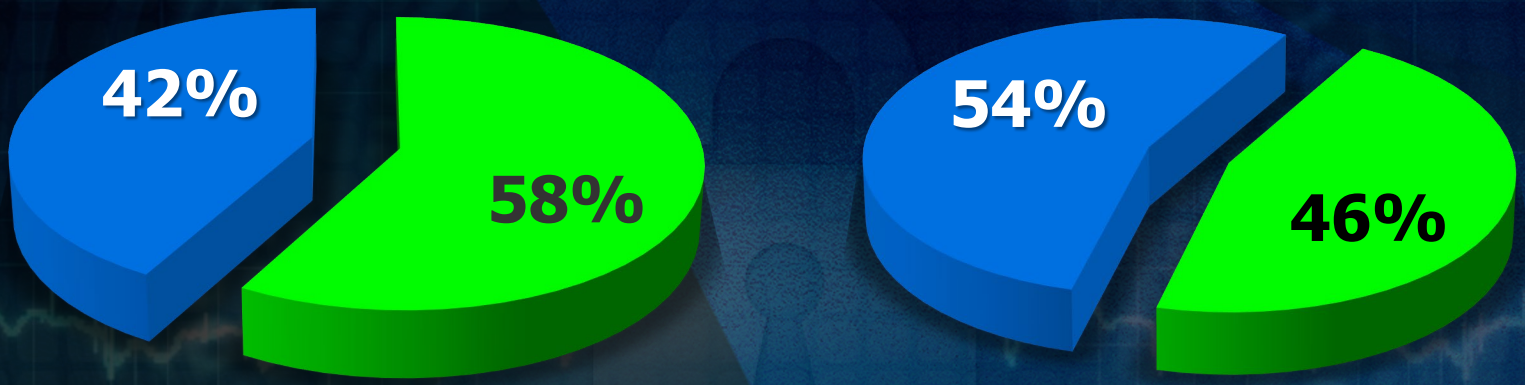
Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Number of Clock Domains Increases with Design Size



Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Designs Projects Implementing Security Features



ASIC/IC Projects

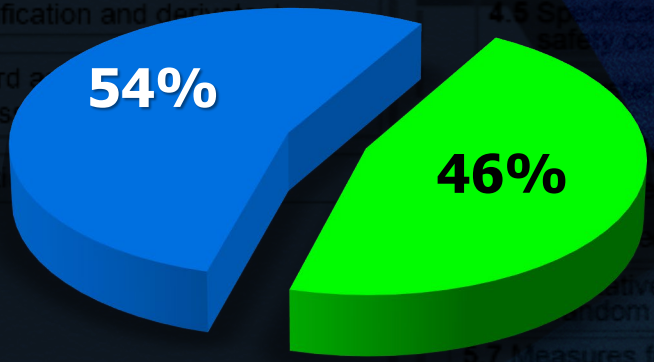
FPGA Projects

Security Features

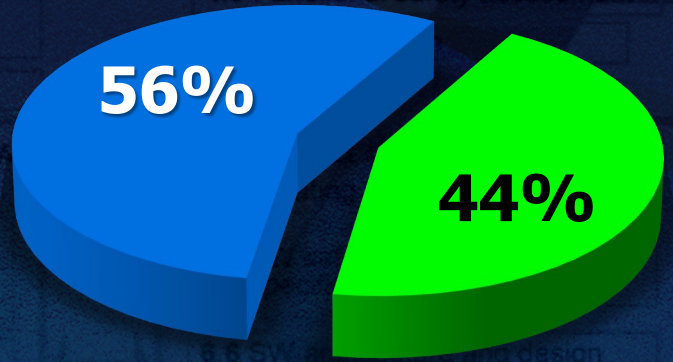
No Security Features

Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Projects Working on Safety Critical Design



ASIC/IC Projects



FPGA Projects

Safety Critical Design

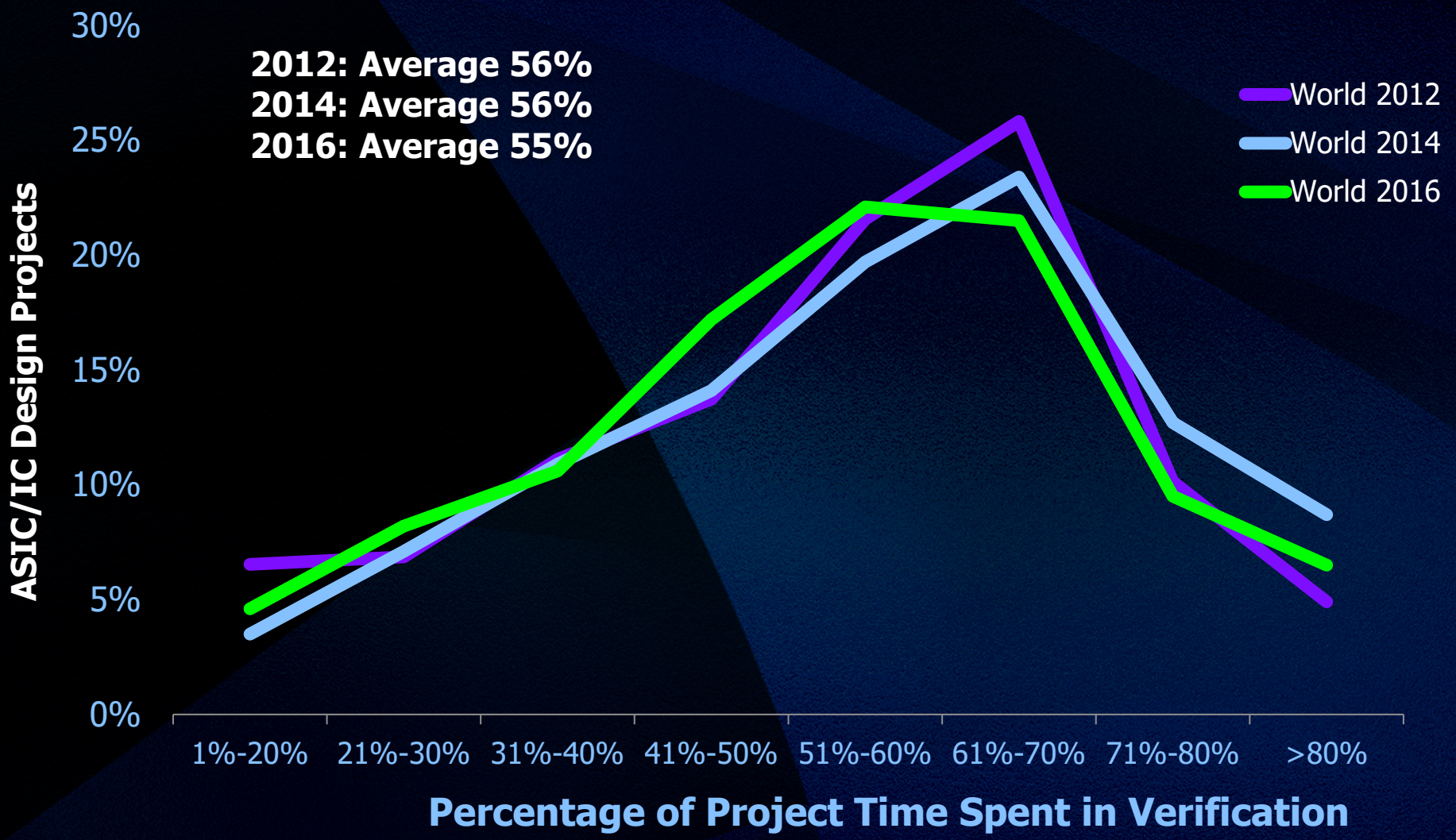
Not Safety Critical

DO-254, ISO26262, IEC60601, IEC61508, etc.

Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

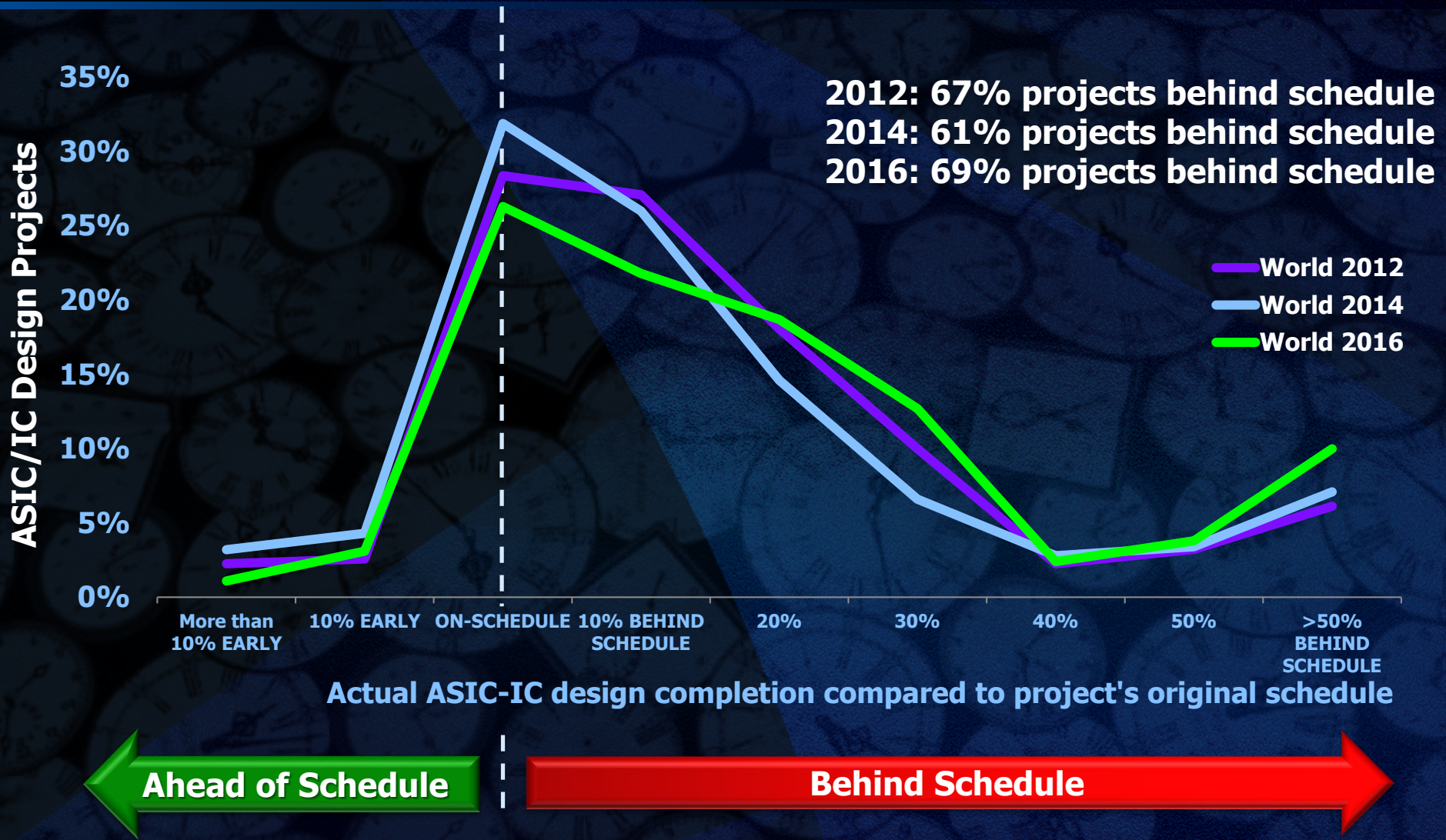
IMPACT OF RISING COMPLEXITY

Verification Project Time



Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Project Completion to Original Schedule

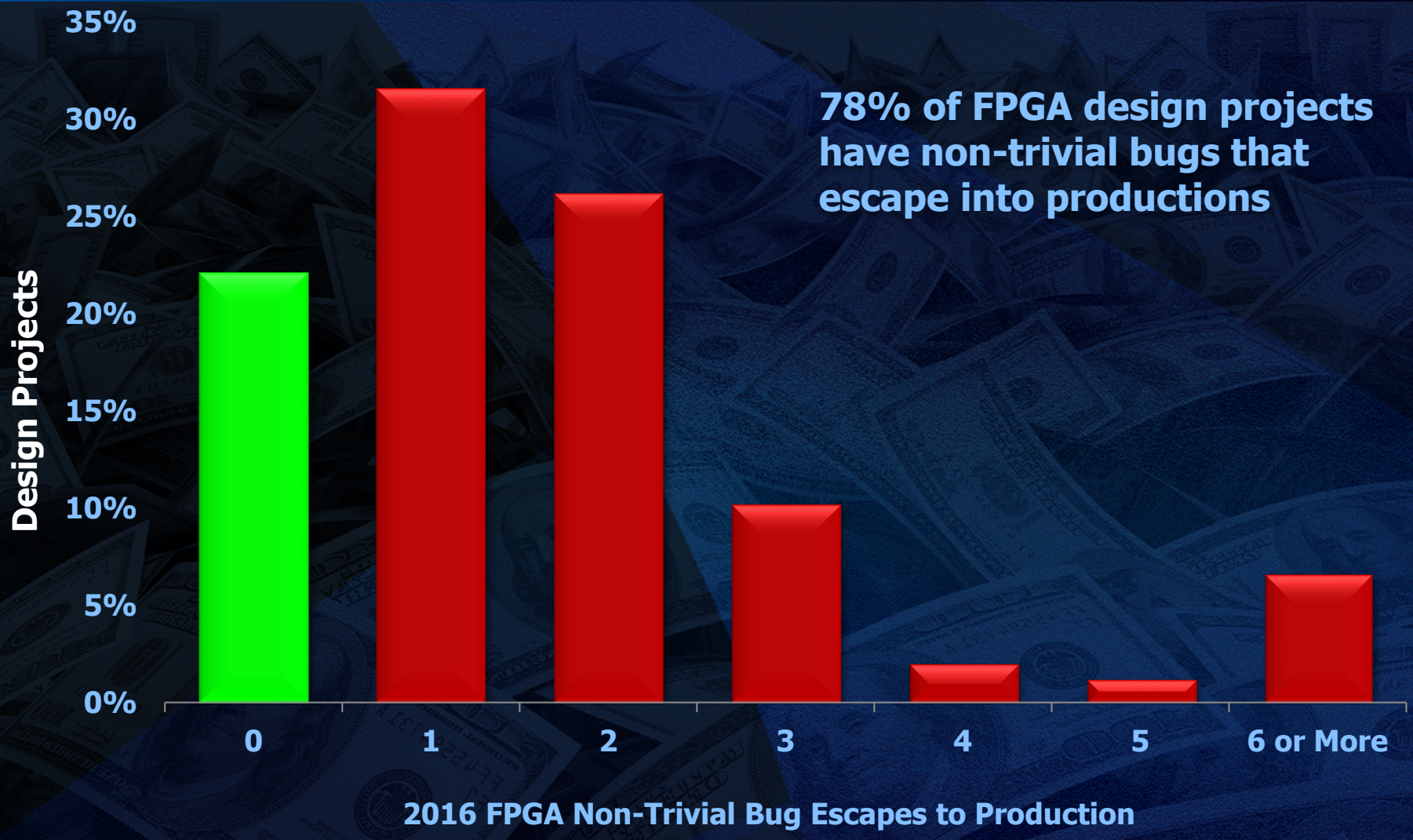


Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

Number of Required Spins Before Production

Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

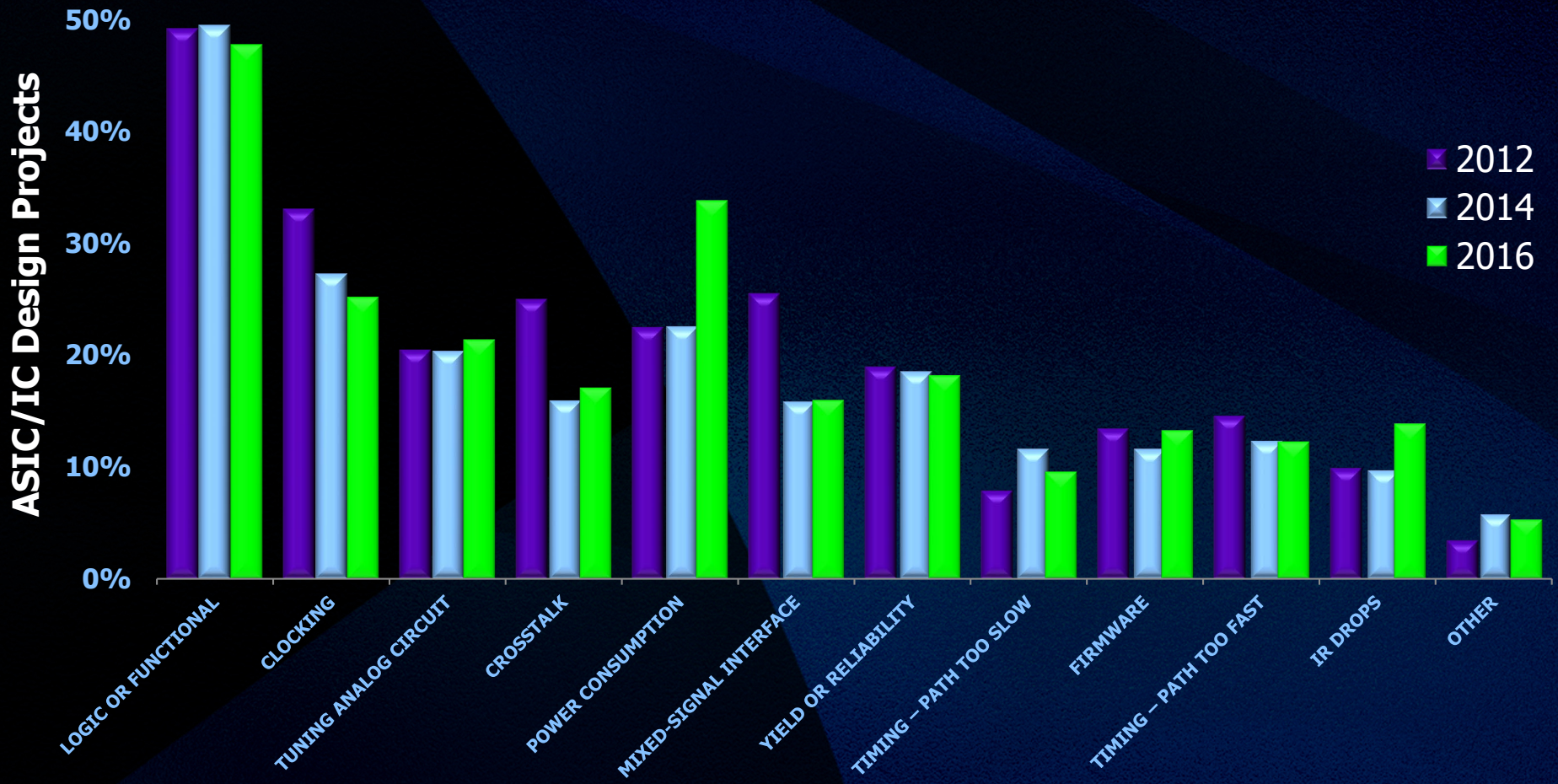
Number of FPGA Bug Escapes to Production



78% of FPGA design projects have non-trivial bugs that escape into productions

Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Flaws Contributing to Respins

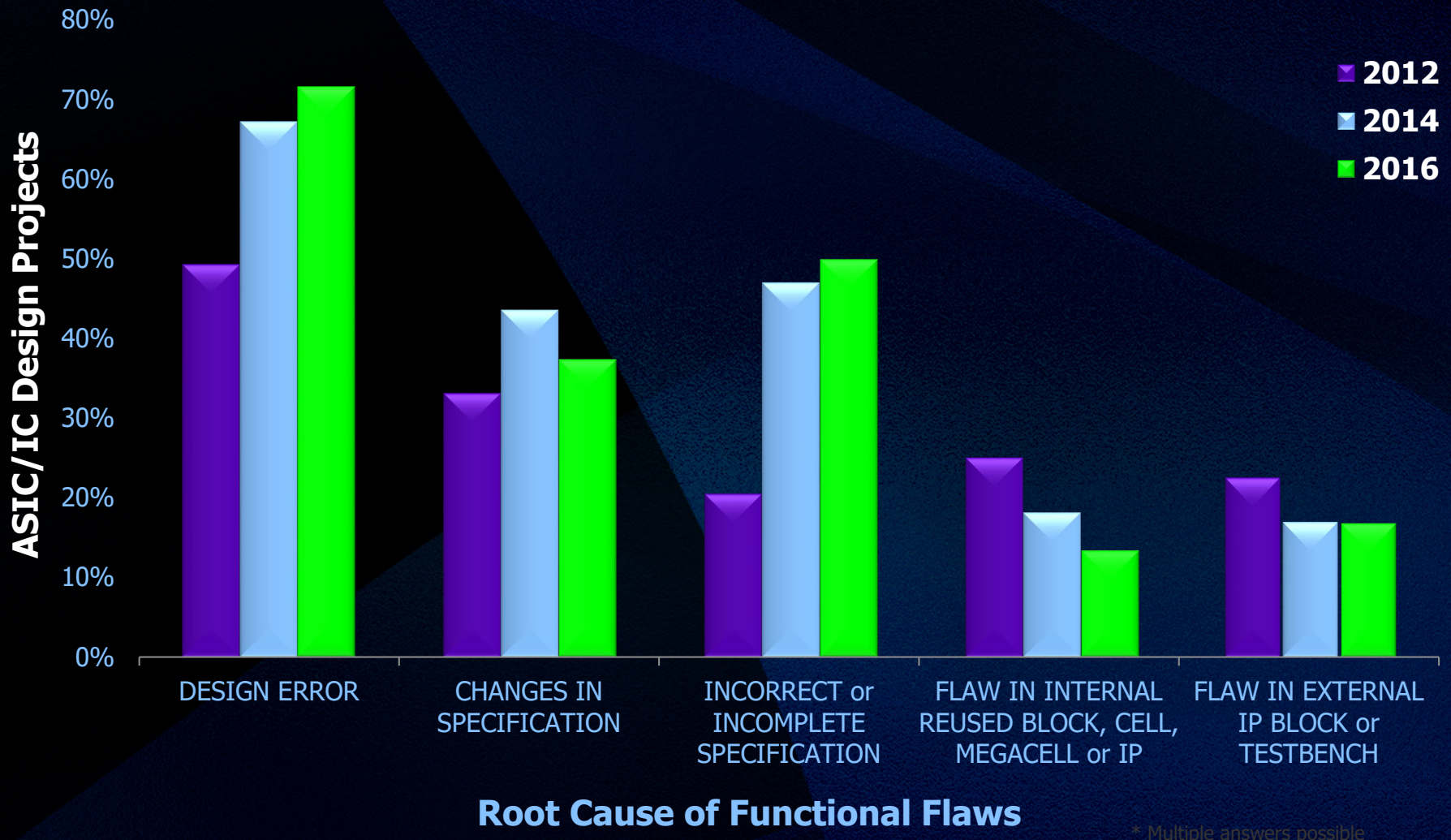


Trends in Types of Flaws Resulting in Respins

* Multiple answers possible

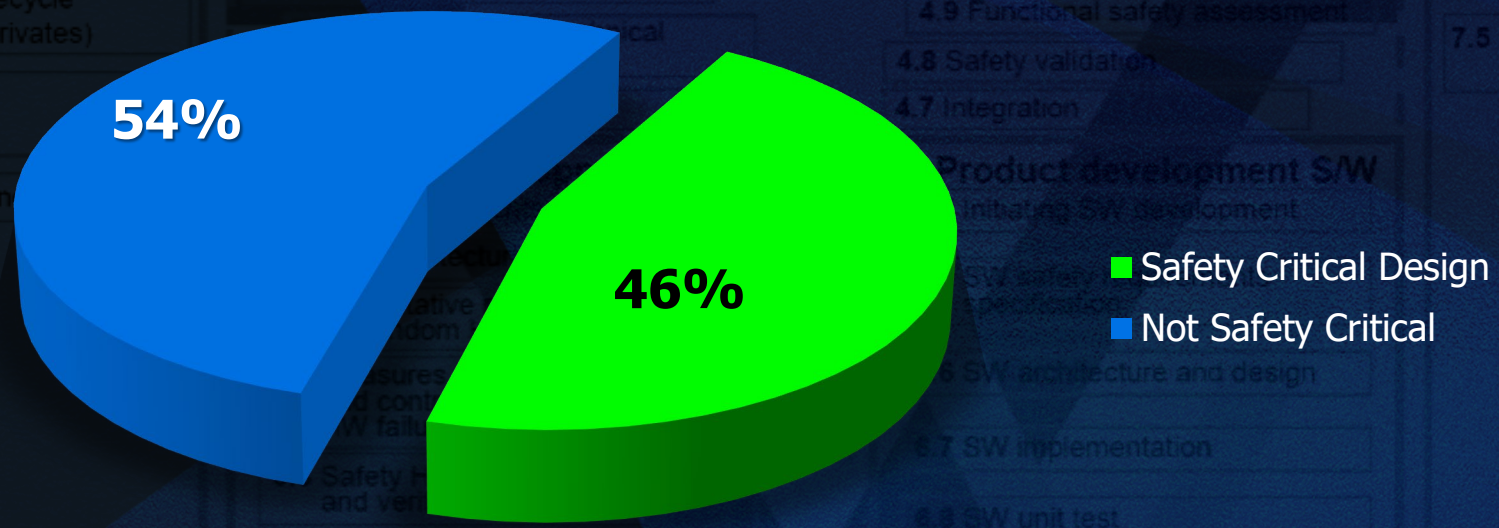
Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Root Cause of Functional Flaws



Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Projects Working on Safety Critical Design

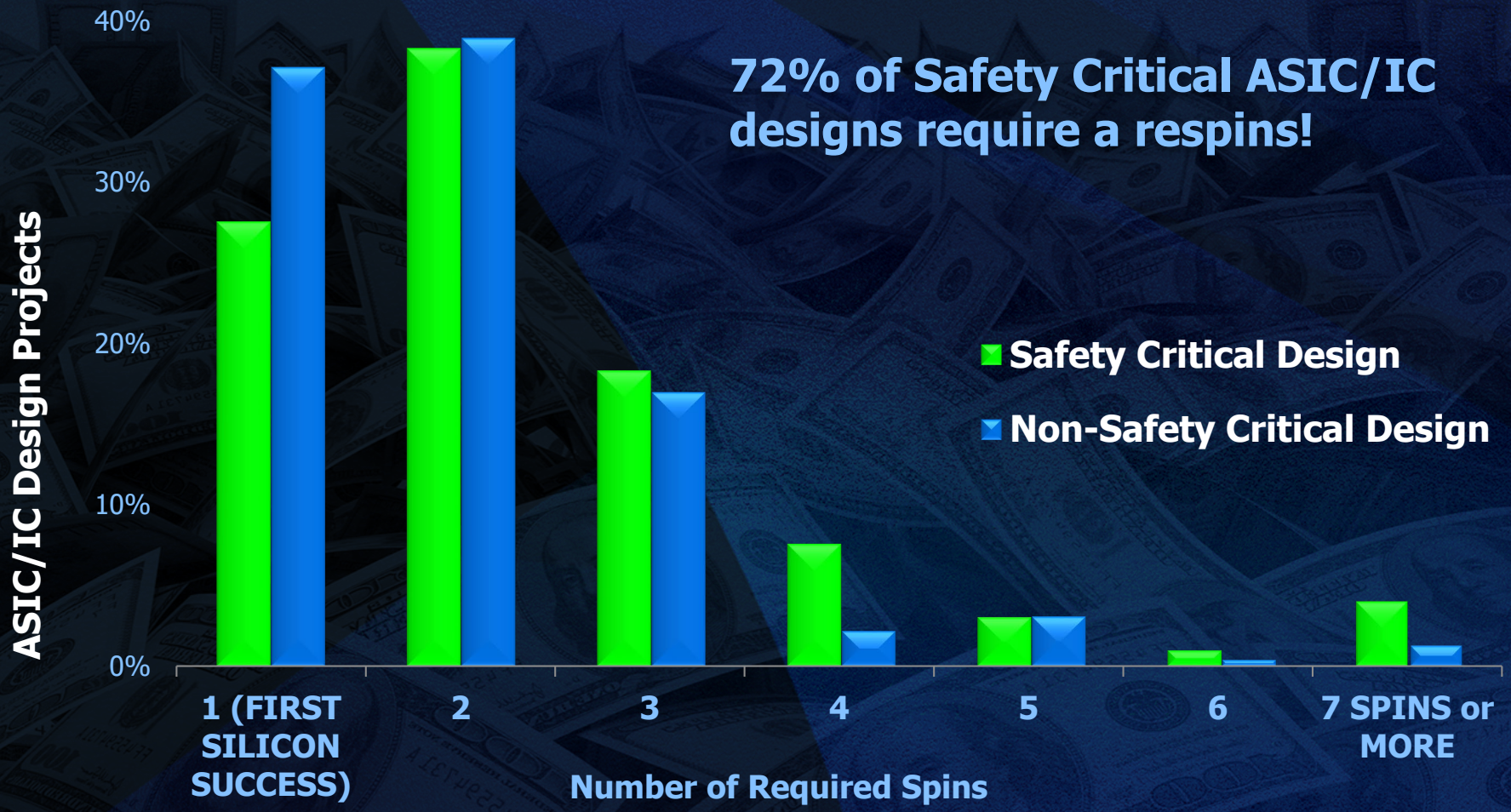


ASIC/IC Projects

DO-254, ISO26262, IEC60601, IEC61508, etc.

Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Required Spins for Safety Critical Designs

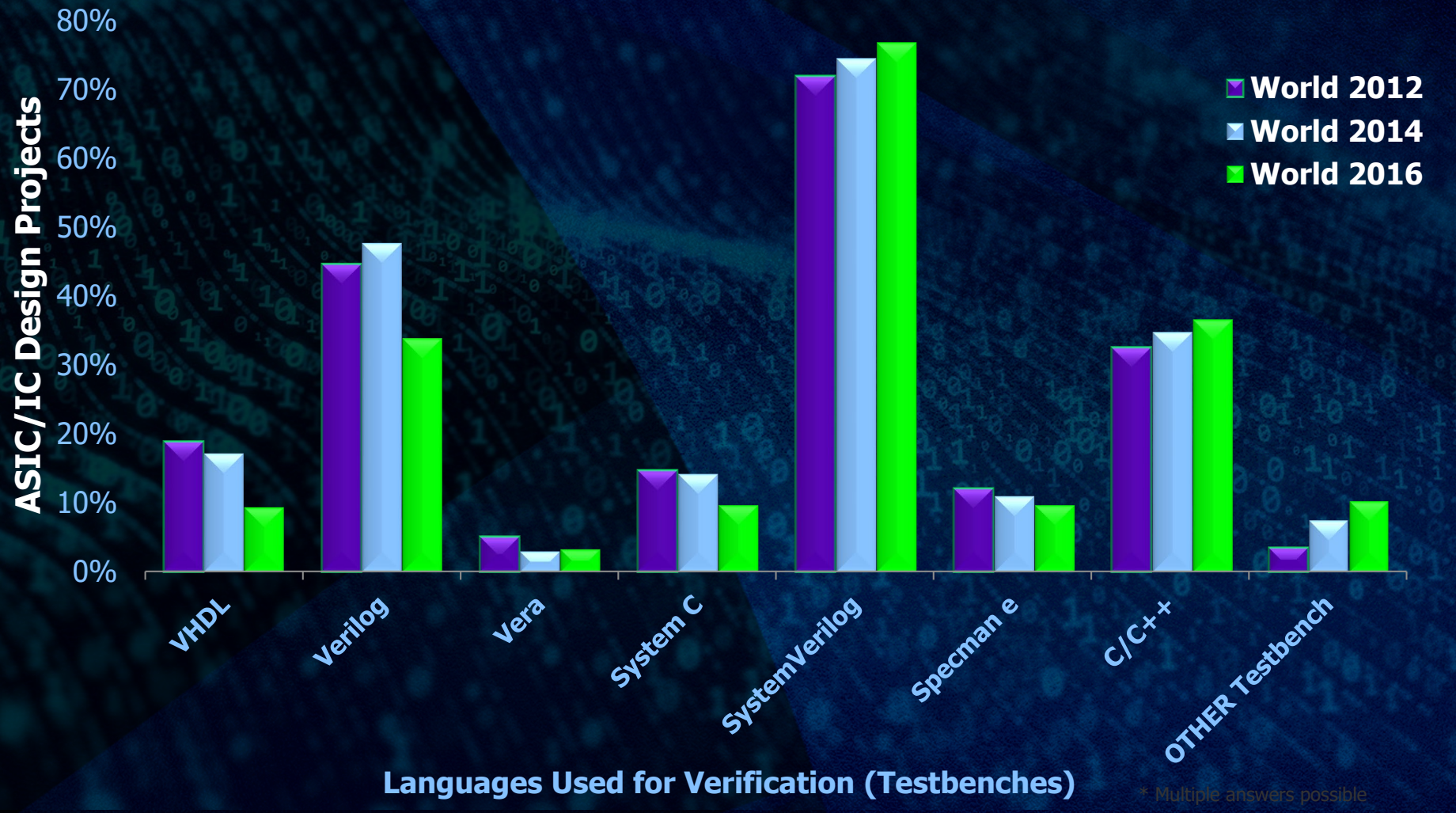


DO-254, ISO26262, IEC60601, IEC61508, etc.

Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

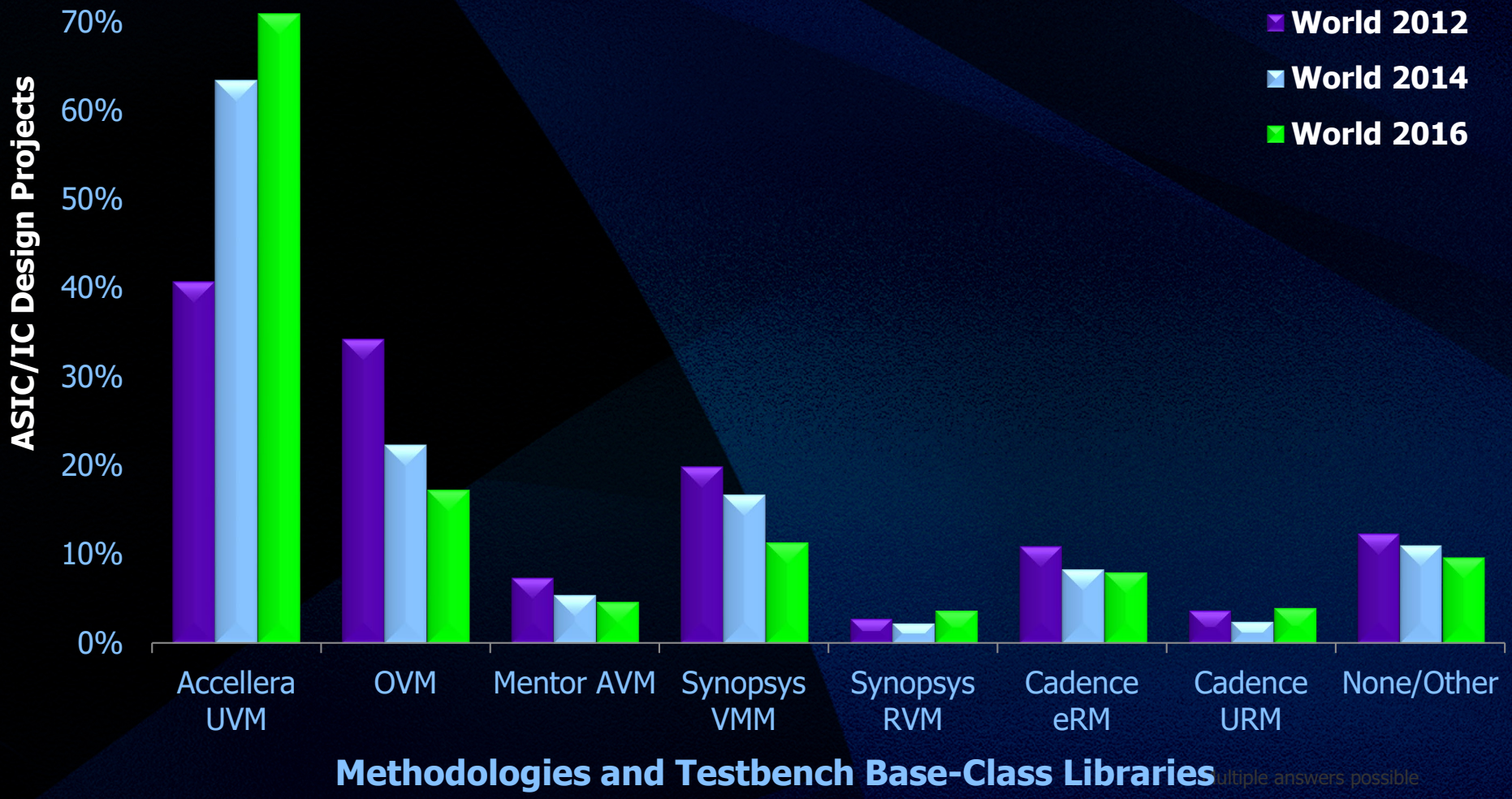
LANGUAGES & METHODOLOGIES

Verification Language Adoption Trends



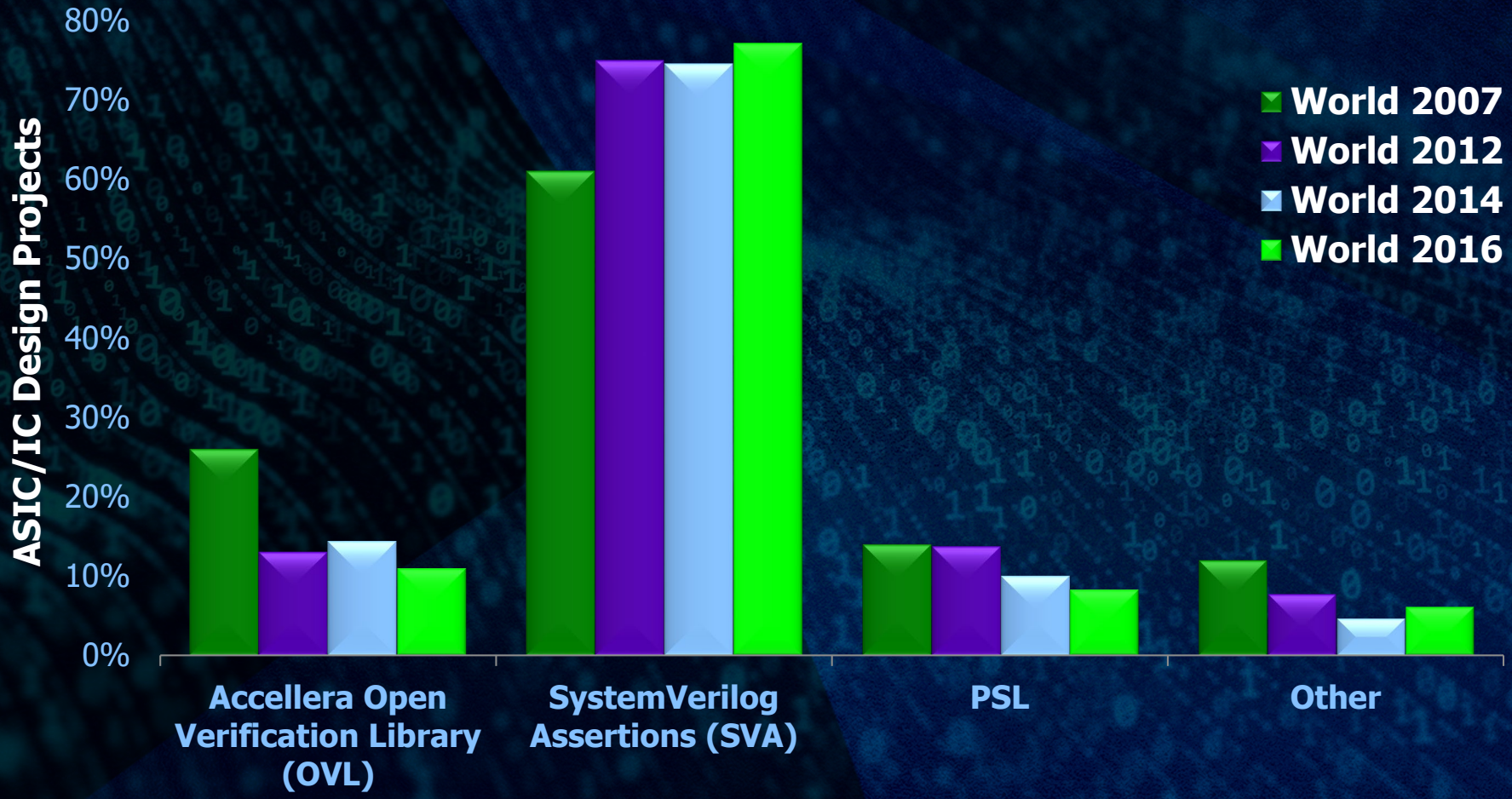
Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Testbench Methodology Adoption Trends



Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

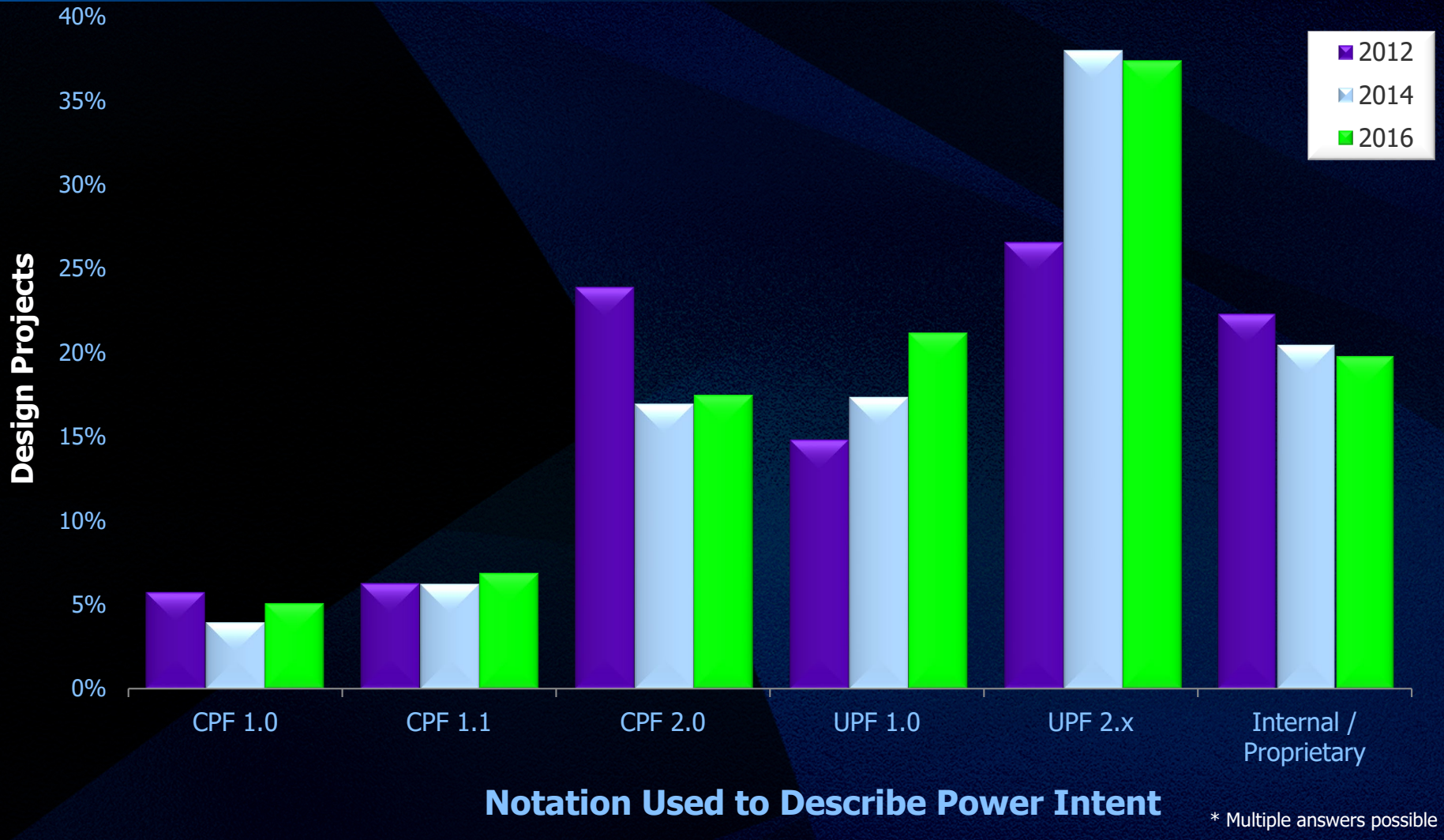
Assertion Language Adoption



Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

* Multiple answers possible

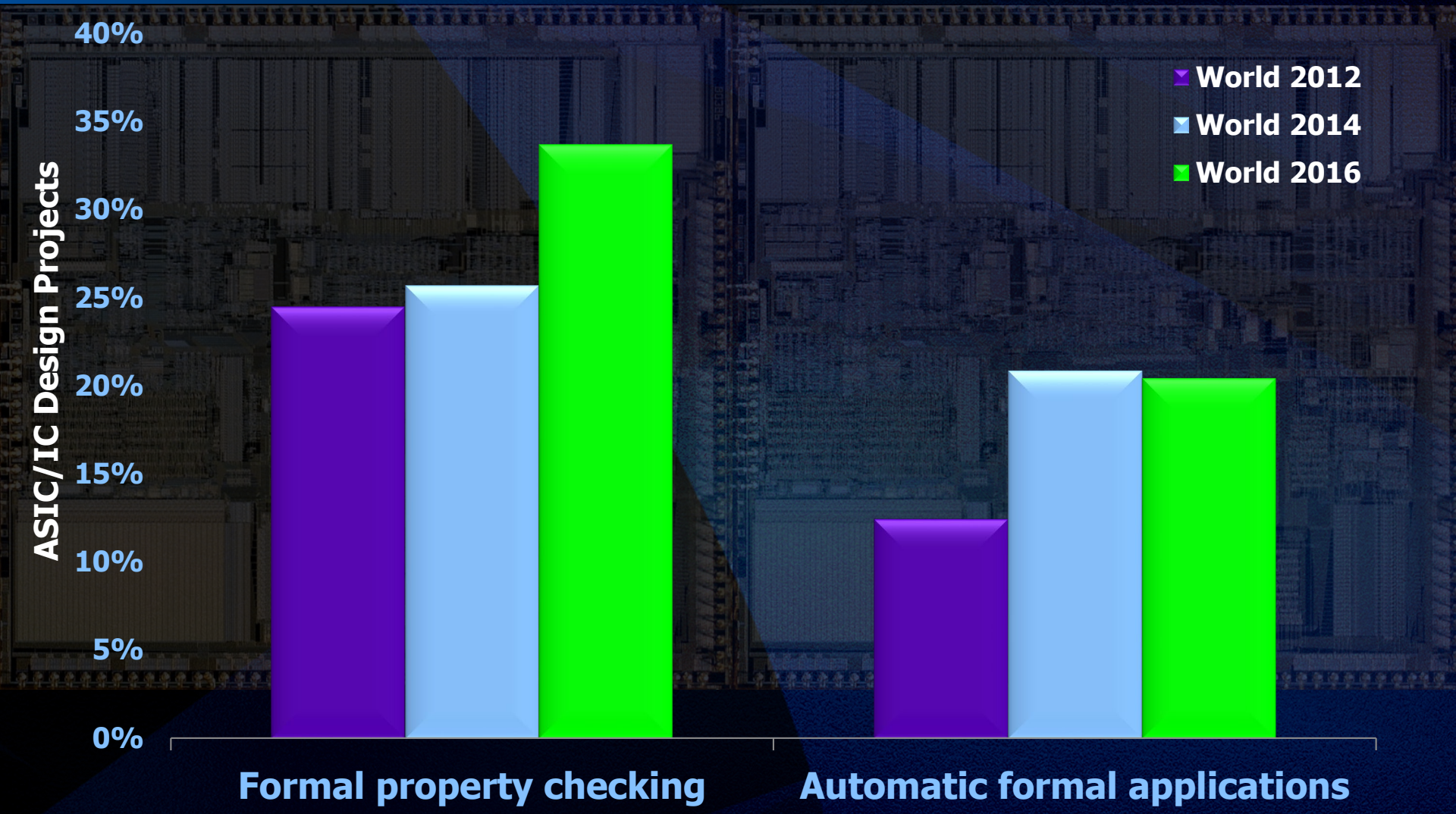
Power Intent Standards Trends



Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

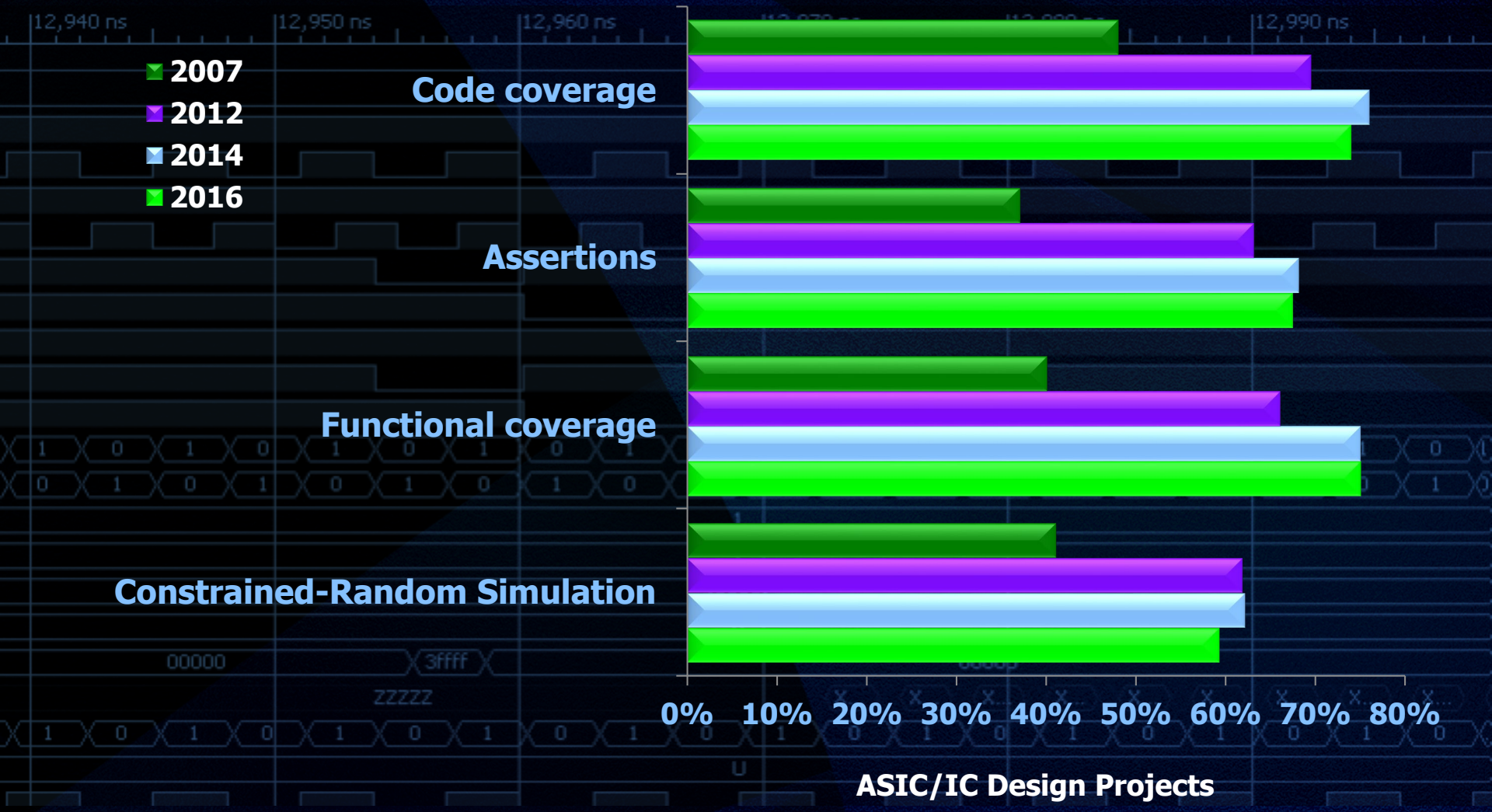
VERIFICATION ADOPTION TRENDS

Formal Technology Adoption Trends



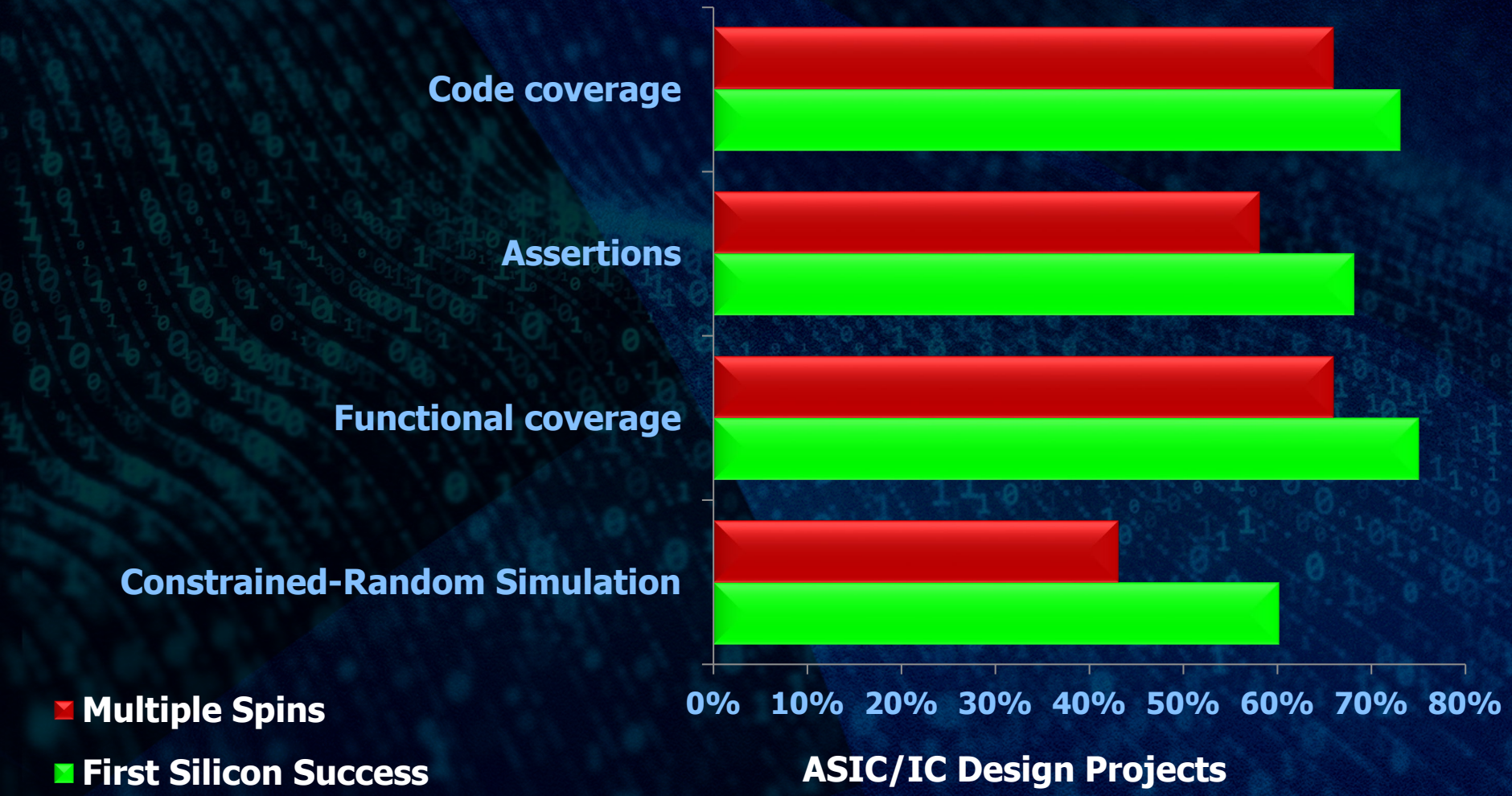
Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Dynamic Verification Adoption Trends



Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

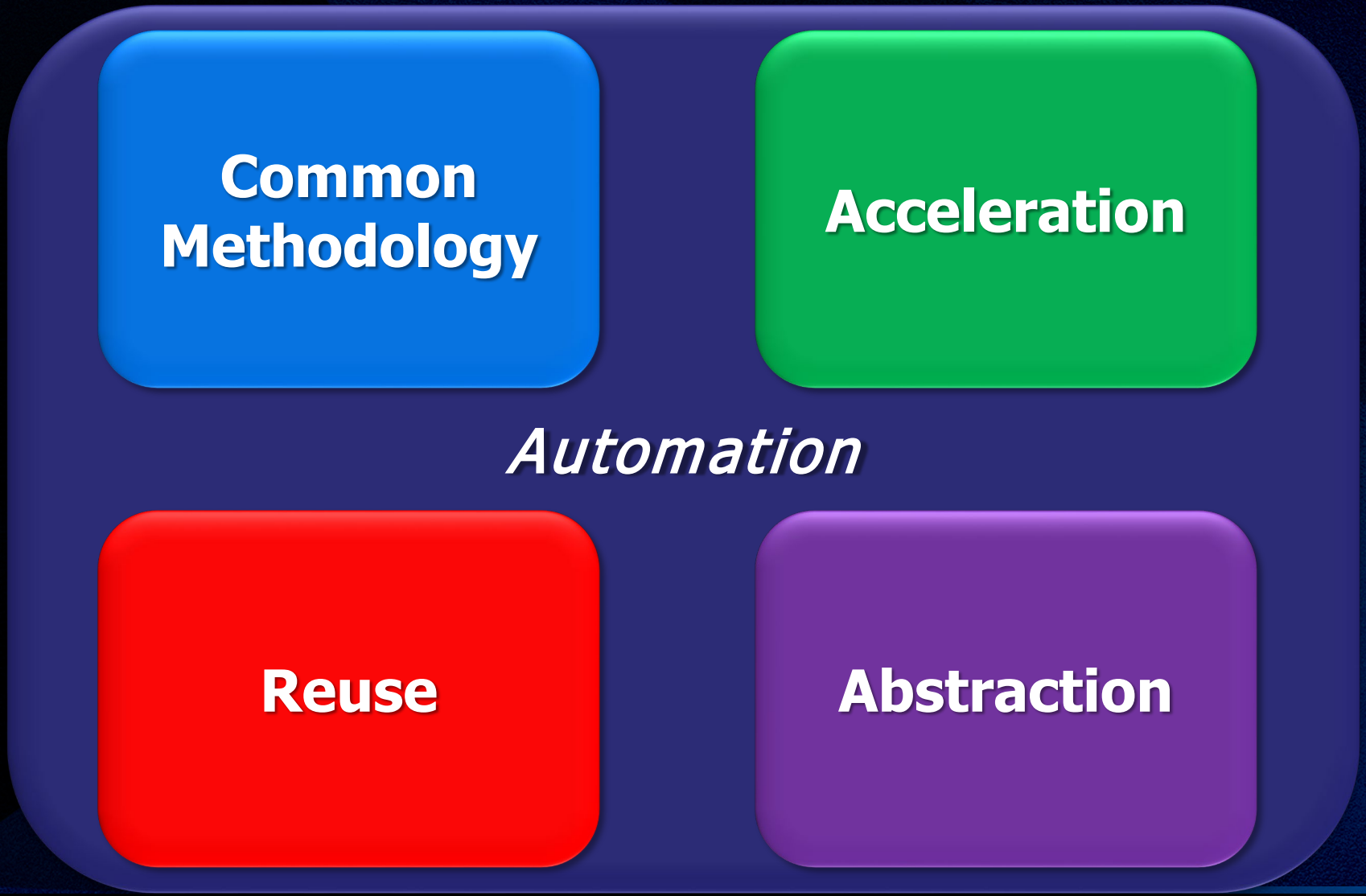
Comparing required spins, and project maturity in adopting various verification techniques.



Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

CLOSING THE VERIFICATION GAP

Closing the Verification Productivity Gap



Summary

- The design productivity gap has been closed through the adoption of advanced automation and reuse methodology
  - What about the verification gap?
- The industry has matured its verification processes rapidly due to rising complexity
- Closing the verification productivity gap will require…
  - The adoption of a common methodology, more reuse (VIP), acceleration, raising the abstraction level when possible, and automating verification to ease adoption and broaden usage

Additional Resources

- Paper accompany this talk in the DVCon proceedings

- See my blog for additional details related to this study
  - **http://go.mentor.com/4Qa1S**
  - Includes both ASIC/IC and FPGA findings

www.mentor.com