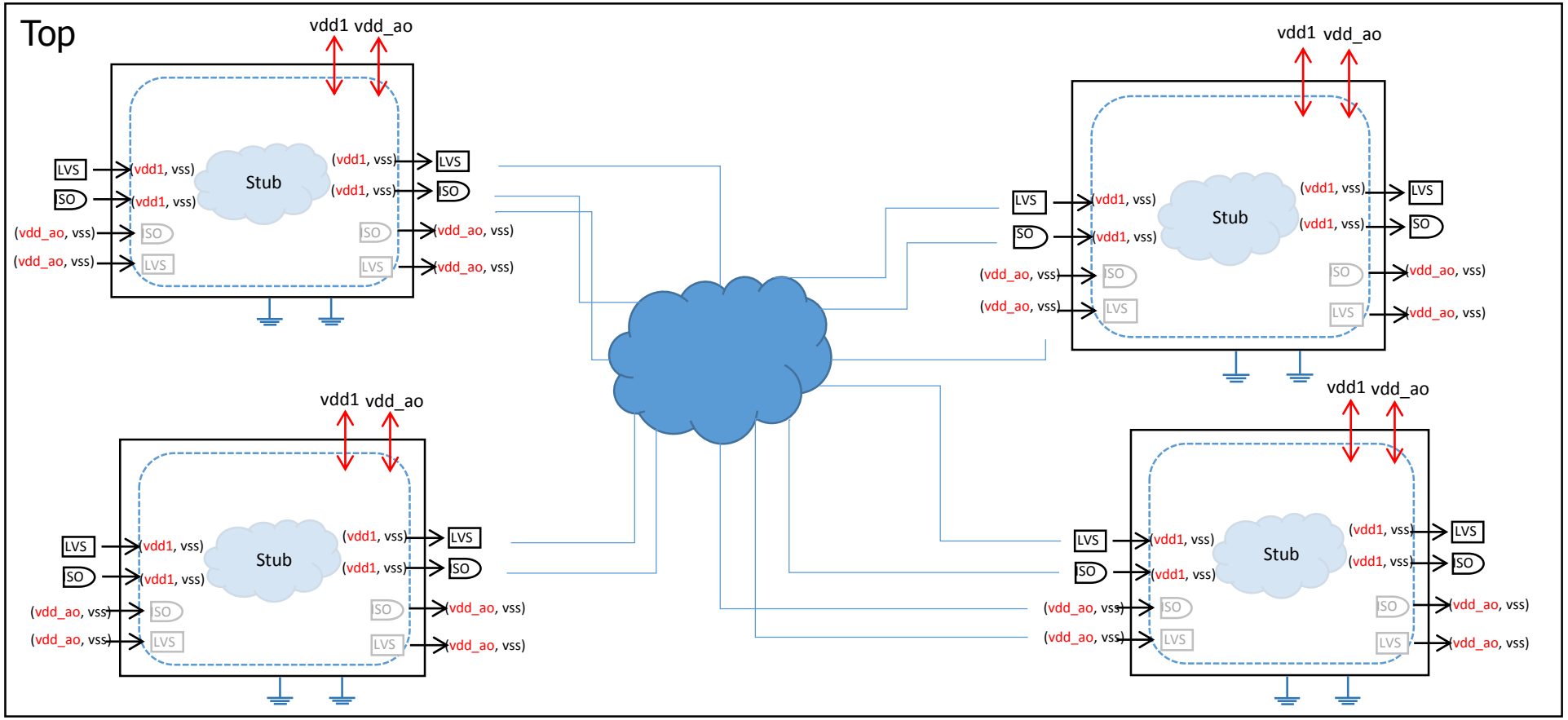
Traditional top level static low power rule check

- Top level check requires complete block level design and supply structures.
  - Requires lots of efforts to clean up block designs.
  - Top level check is not available until block design and UPF are complete.

- Sub-design Interface Aware top only flow enables early stage low power rule check of top level to block interfaces.
  - Only block boundary ports and supply constraints are required.
  - Top level check is available at the early stage of implementation with properly constrained power intents.

Sub-design interface aware static low power check

- Takes advantage of supply of boundary port in low power rule check

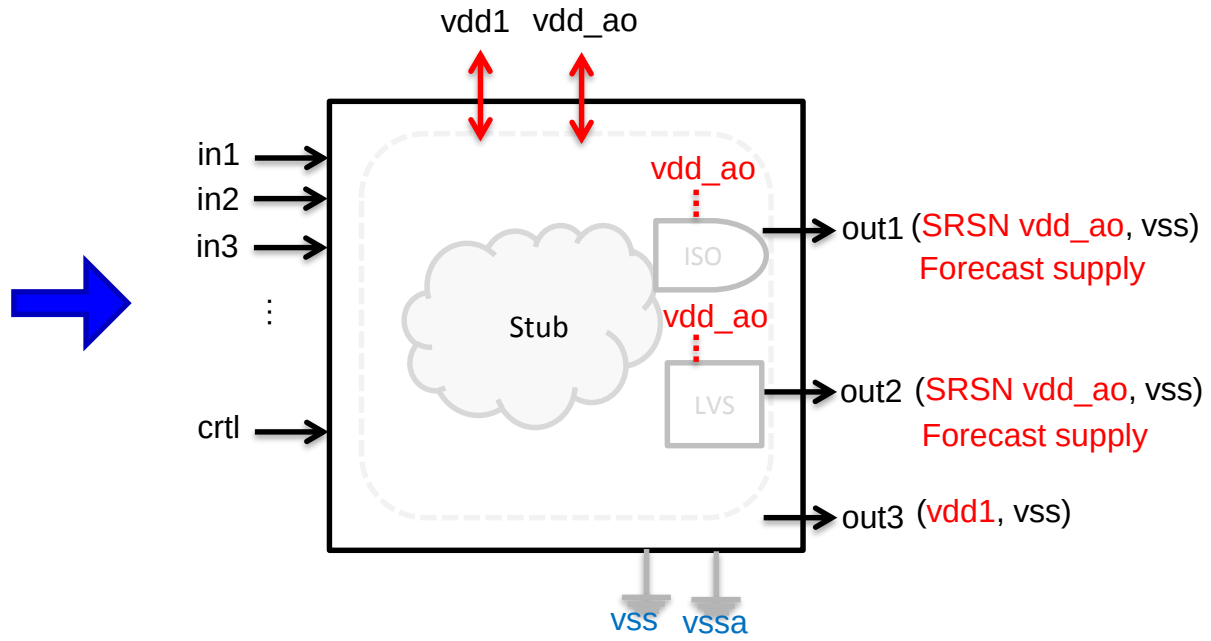


Supply constraints of boundary port

- User can apply “forecast” supply to sub-design interface ports

Sub.upf

```
set_related_supply_net –power {vdd_ao}
–object_list { \
            to_be_implemented_port_d
            to_be_implemented_port_e }
 ------------------------------------------------------------
set_port_attributes –driver_supply ss_vdd1
 –elements {in*}
set_port_attributes –receiver_supply ss_vdd_1
-elements {out*}
```



Tool methodology

```
VC LP Script:

set search_path ..
set link_library ..
set_app_var <configuration> true

# Sub-design interface aware flow.
# VC LP preserve boundary ports and associated UPF power strategies at the
interface level between sub-designs and top logic.
set_blackbox -designs { BLK_AON BLK_BUS1 BLK_BUS2 BLK_FUNC1 BLK_FUNC2 BLK_FUNC3
BLK_CPUX BLK_CPUY BLK_FUNC4 BLK_FUNC5 BLK_FUNC6 BLK_FUNC7 BLK_FUNC8 BLK_FUNC9
BLK_FUNC10 BLK_GLOBAL BLK_MEM BLK_FUNC11 BLK_FUNC12 BLK_FUNC13 BLK_FUNC14
BLK_FUNC15 BLK_FUNC16 BLK_FUNC17 BLK_PERIPHERAL BLK_FUNC18 BLK_FUNC19 BLK_FUNC20
}

Read_file -format verilog -netlist -top S*E_fullchip <top netlist + block
netlists>
Read_upf <top upf + list of sub upfs> # VC LP preserves supply const. of boundary
```

Rule check comparison on UPF

- Consistent results at UPF checks

Violation Tag	Counts	Description
PST_STATE_MULTIPLE	134	Same power state
UPF_CSN_LS	2088	LS pg pin requires CSN.
UPF_CSN_PAD	1516	PAD pg pin requires CSN.
UPF_SUPPLY_MISSING	65	UPF supply never present in PST.
PST_SUPPLY_MULTIPLE	6	Same supply did not appear in the power state table.

Rule check comparison on UPF

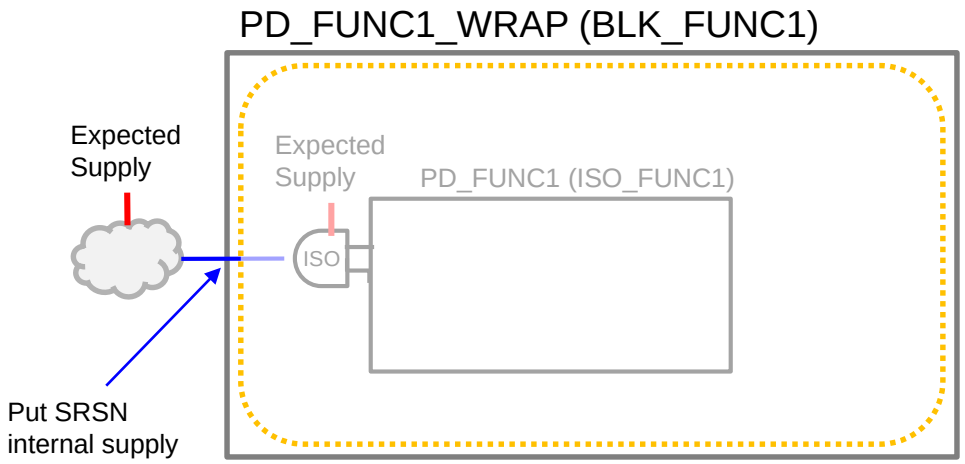
- Inconsistent results at UPF checks due to improper supply constraint

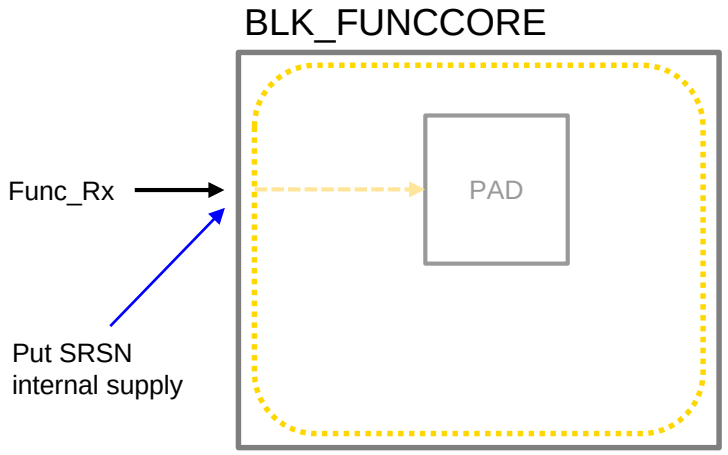
Violation Tag	Unique cases	Description
ISO_STRATEGY_MISSING	2	UPF is missing isolation strategy for a crossover
LS_STRATEGY_MISSING	1	UPF is missing level shifter strategy for a crossover
UPF_SUPPLY_NO_STATE	1	Created supply not registered in the PST
UPF_SUPPLY_UNCONN	1	UPF Supply does not have any driver
UPF_SRSNSUPPLY_MISMATCH	-	SRSN supply is not identical to driver/load supply/SRSN
UPF_SUPPLY_UNUSED	1	Declared supply not used anywhere in UPF

Rule check comparison on UPF

- Inconsistent results at UPF checks due to improper supply constraint

Violation Tag	Unique cases	Solution
ISO_STRATEGY_MISSING	2	SRSN internal supply on the interface port

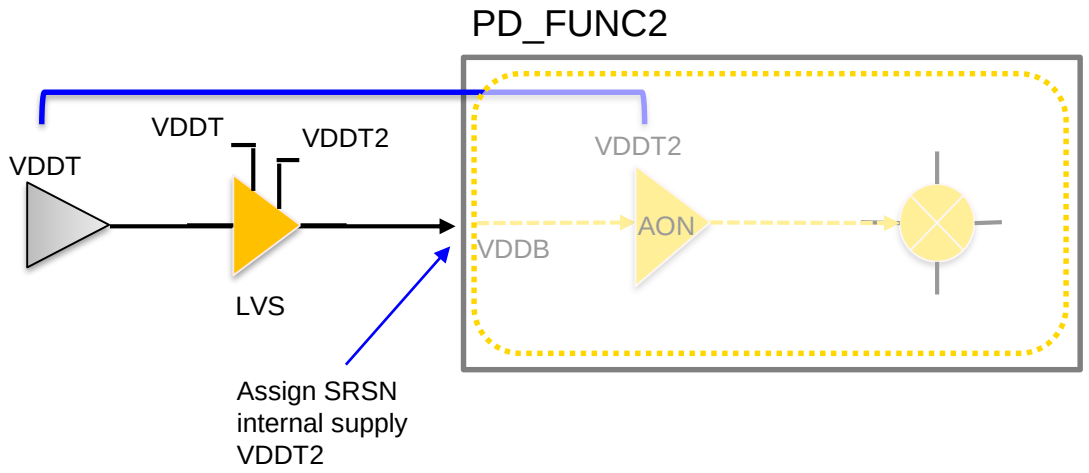




Rule check comparison on UPF

- Inconsistent results at UPF checks due to improper supply constraint

Violation Tag	Unique cases	Solution
LS_STRATEGY_MISSING	1	SRSN internal supply on the interface port



Rule check comparison on design

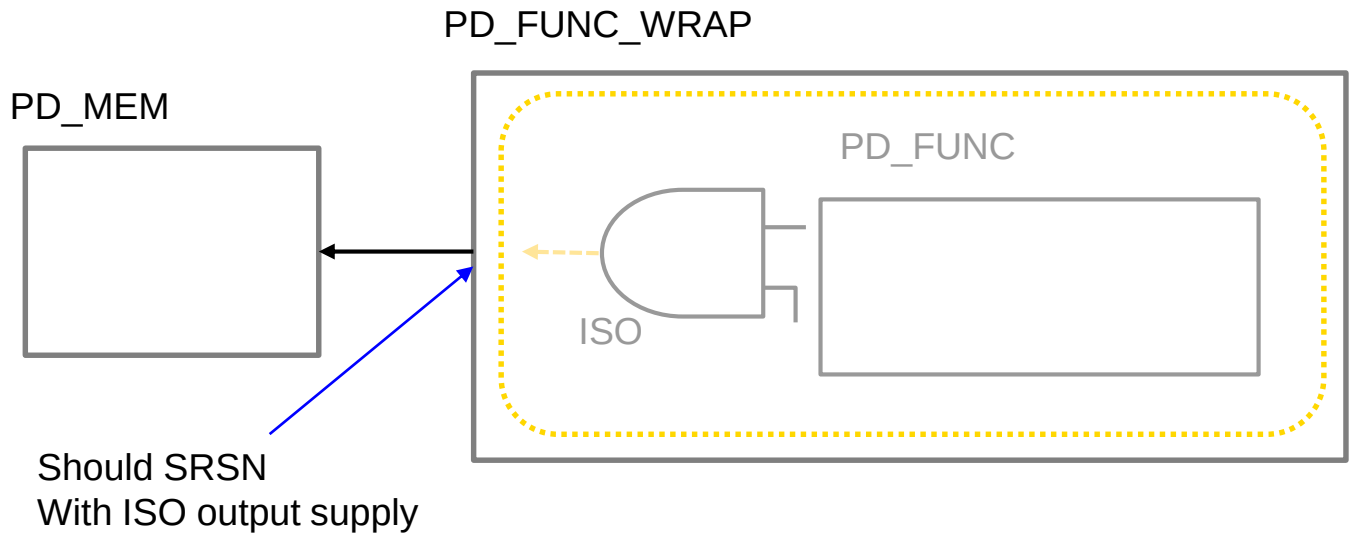
- Inconsistent results at design checks due to improper supply constraint

Violation Tag	Unique cases	Description
ISO_INST_MISSING	4	Isolation instance is missing from source to sink crossover
SINK_SUPPLY_LEAKAGE	1	Sink logic is ON where driver is OFF
LS_INPWR_CONN	1	Input power of level shifter is not compatible to source power
LS_OUTPWR_CONN	1	Output power of level shifter is not compatible to sink power
ISO_STRATEGY_UNUSED	1	No isolation cell present for a isolation strategy
ISO_OUTPUT_UNCONN	1	Isolation instance output is unconnected
ISO_DATA_CONSTANT	1	Isolation instance is driven by constant TIE
ISO_DATA_UNCONN	1	Isolation data pin is unconnected

Rule check comparison on design

- Inconsistent results at design checks due to improper supply constraint

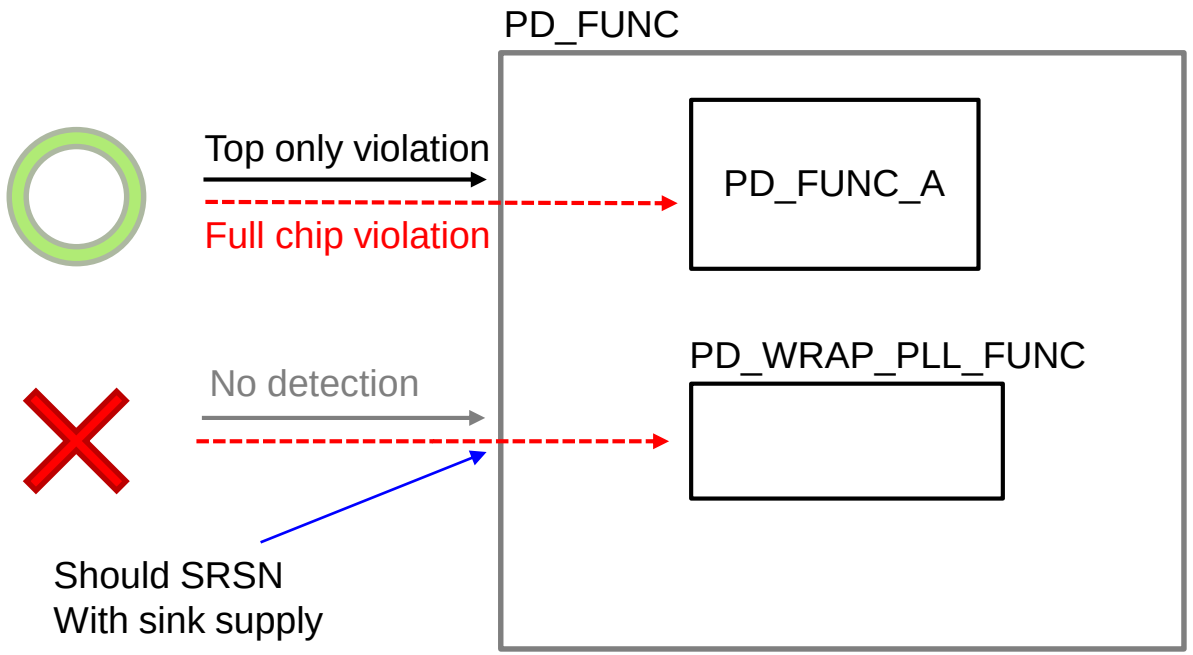
Violation Tag	Unique cases	Solution
ISO_INST_MISSING	4	Put SRSN with ISO output supply to the interface port



Rule check comparison on design

- Inconsistent results at design checks due to improper supply constraint

Violation Tag	Unique cases	Solution
ISO_INST_MISSING	4	Put SRSN with the supply of PD_WRAP_PLL_FUNC



Rule check comparison on design

- Inconsistent results at design checks due to limitation

Violation Tag	Unique cases	Description
LS_INST_REDUND	1	Level shifter instance not required