

Towards Early Validation of Firmware using UVM simulation framework

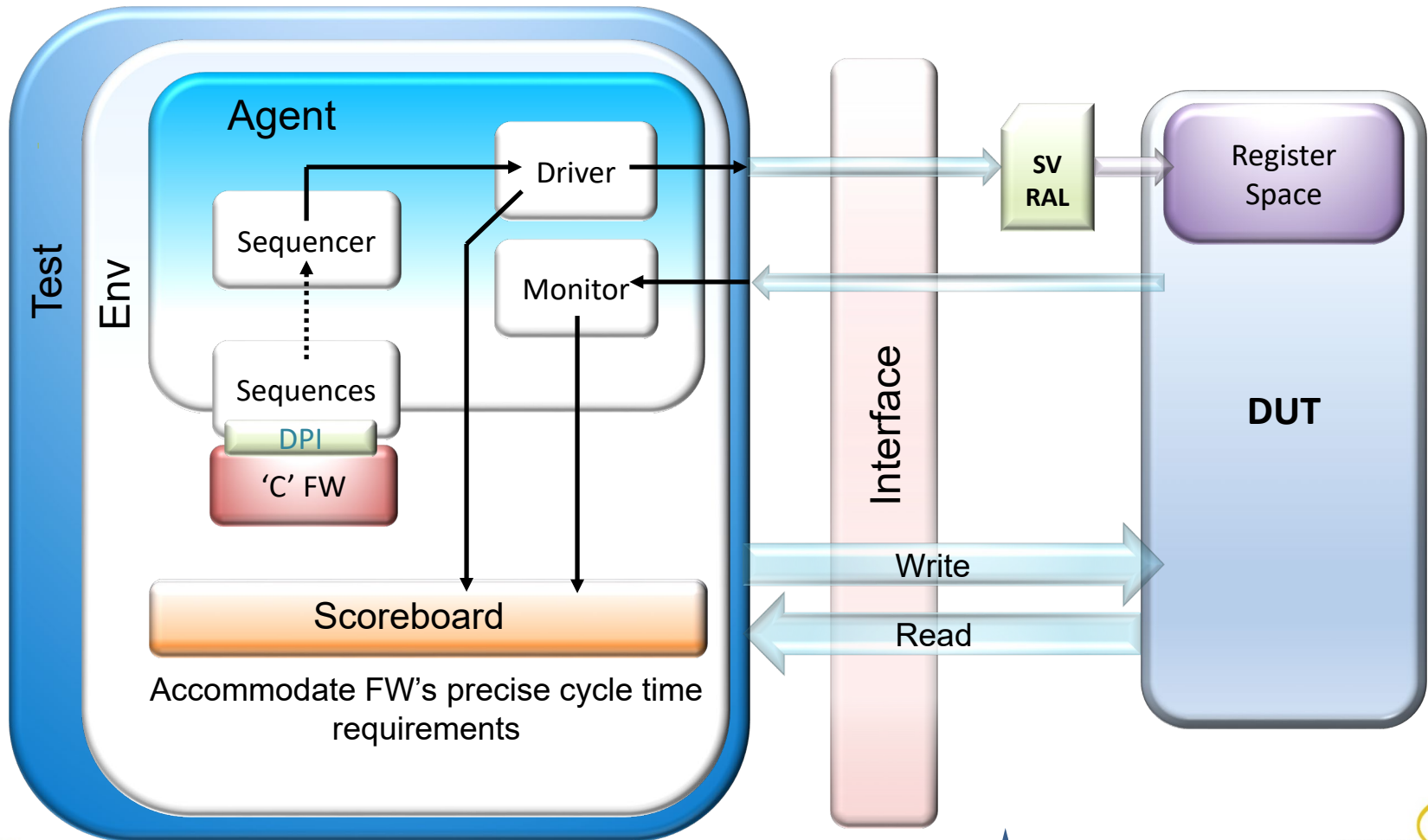
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AGENDA

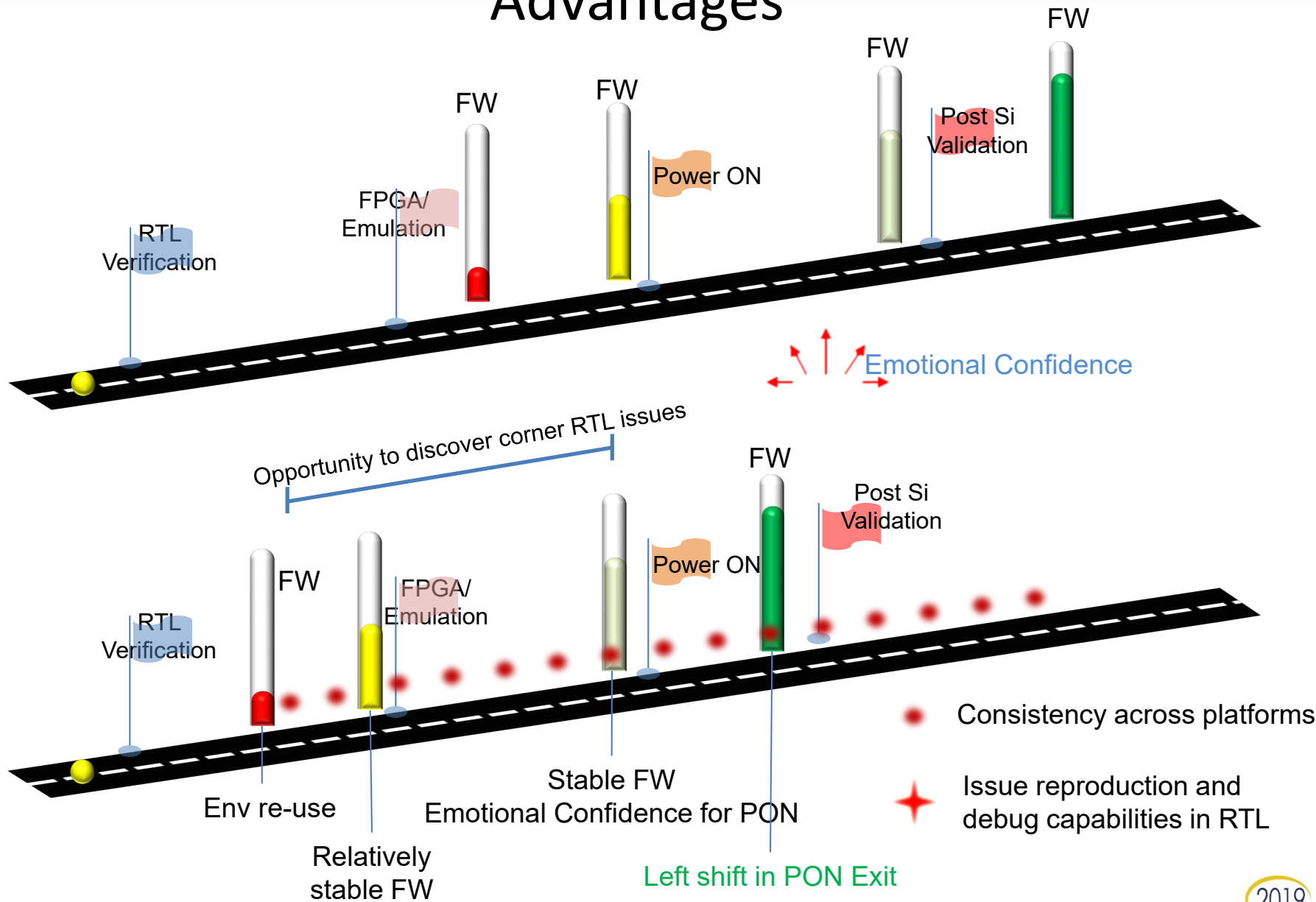
- Firmware in simulation – UVM framework
- Advantages of “Firmware in simulation”

Firmware in Simulation – UVM Framework

- UVM and Firmware Amalgamation



Advantages



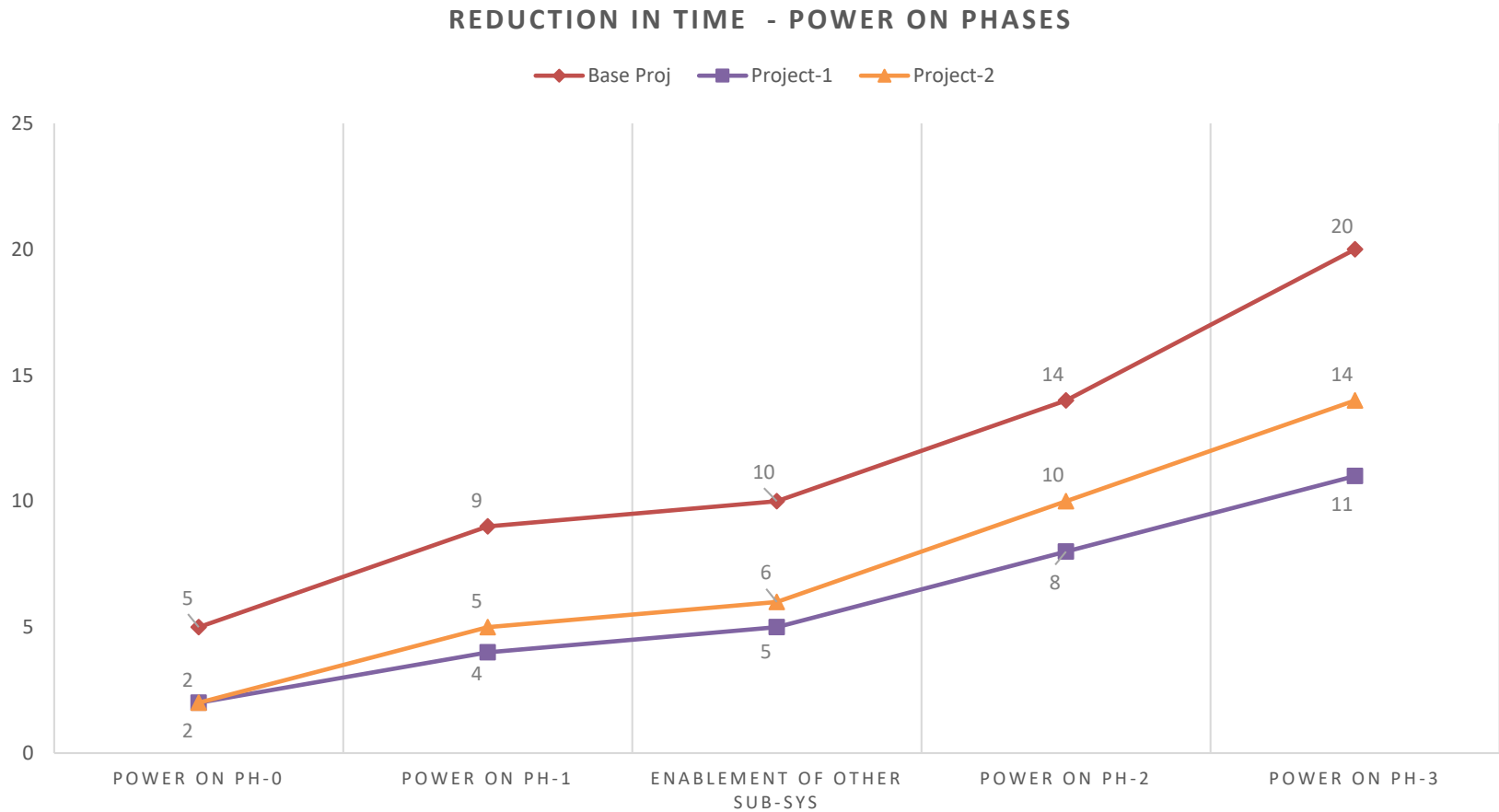
Advantages

- Reduction in time-to-revenue

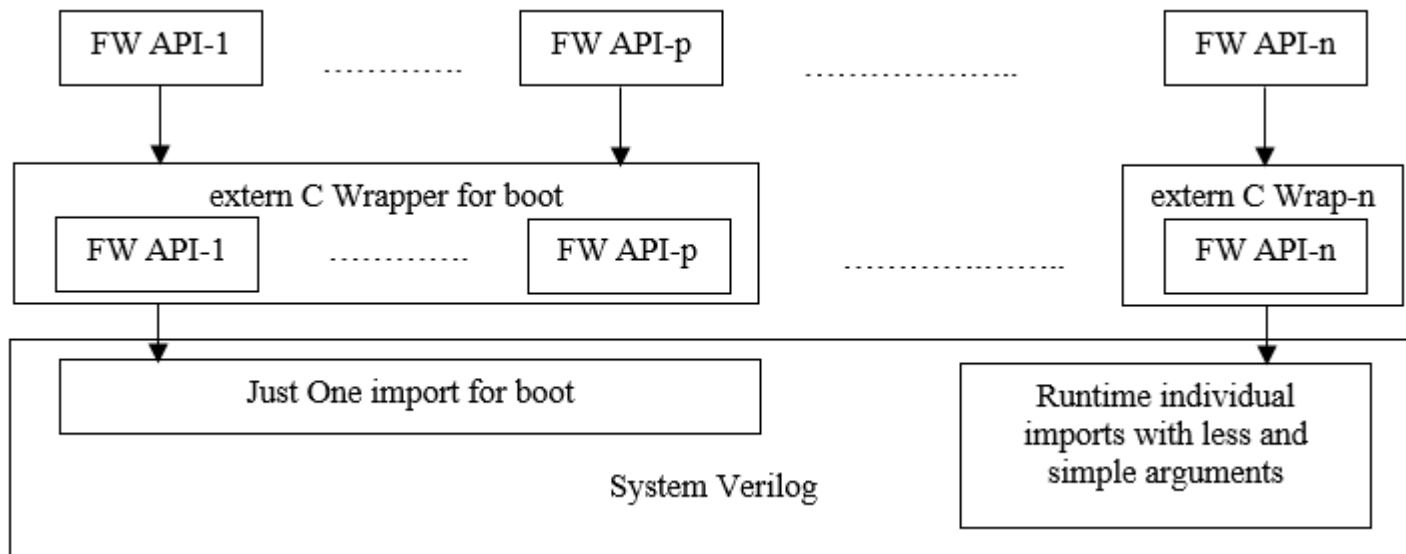
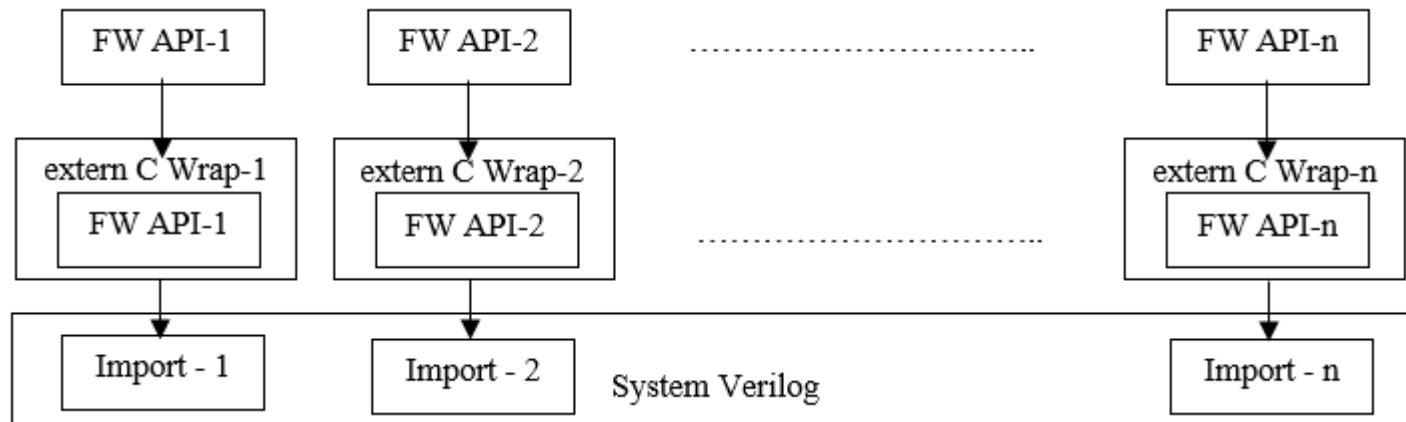
Projects	# of lines of code before silicon	# of lines of code changed after silicon until power ON	% of change done after silicon
Base Project (no firmware validation during RTL simulation, only partial validation in emulation)	3432	921 (addition of APIs/sequences, changes in APIs/sequence orders, deletion of sequences, changes in register setting values, change in array sizes)	27%
Project-1 (with firmware validated during RL simulation)	3201	195 (Addition of code to support specific PHY pad trainings for an issue root caused during ATE characterization, changes in some register settings after assessment of silicon behavior)	6%
Project-2 (with firmware validated during RTL simulation)	4350	519 (Code change due to introduction of new frequency plan for some customers, change in other register settings)	12%

Advantages

- Faster Power ON exit



- Firmware abstraction layer



Questions