Timing-Aware high level power estimation of industrial interconnect module

Amal Ben Ameur[1], Antonio Genov[1,2], François Verdier[1], Loic Leconte[2]

(1)University of Cote d'Azur, LEAT, Sophia Antipolis, France

(2)NXP SEMICONDUCTORS, Mougins, France

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Context and Motivations

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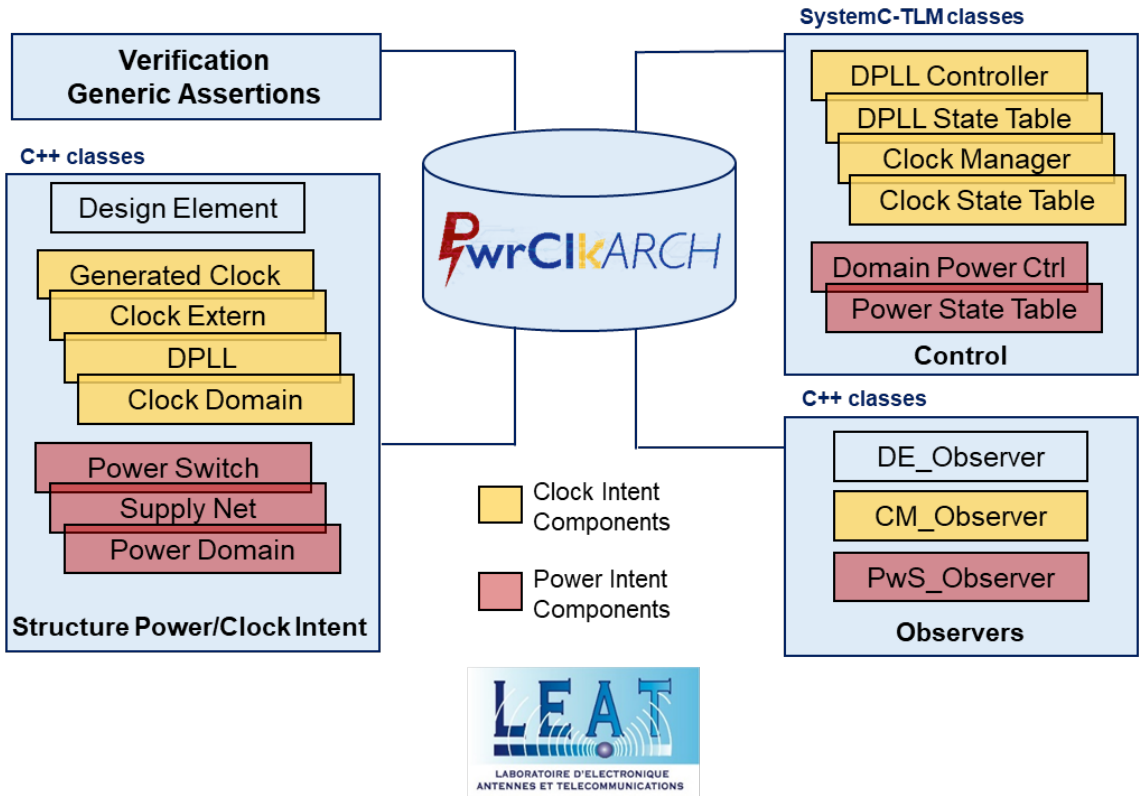
PwClkARCH library

- C++/SystemC-TLM library inspired from the **UPF** standard
- Based on the **co-simulation** between a power model description and a SystemC-TLM based virtual prototype
- Ensures the **estimation** of the power metrics dynamically, and the application of **hardware power management strategies** (clock gating, power gating, DVFS, etc.)



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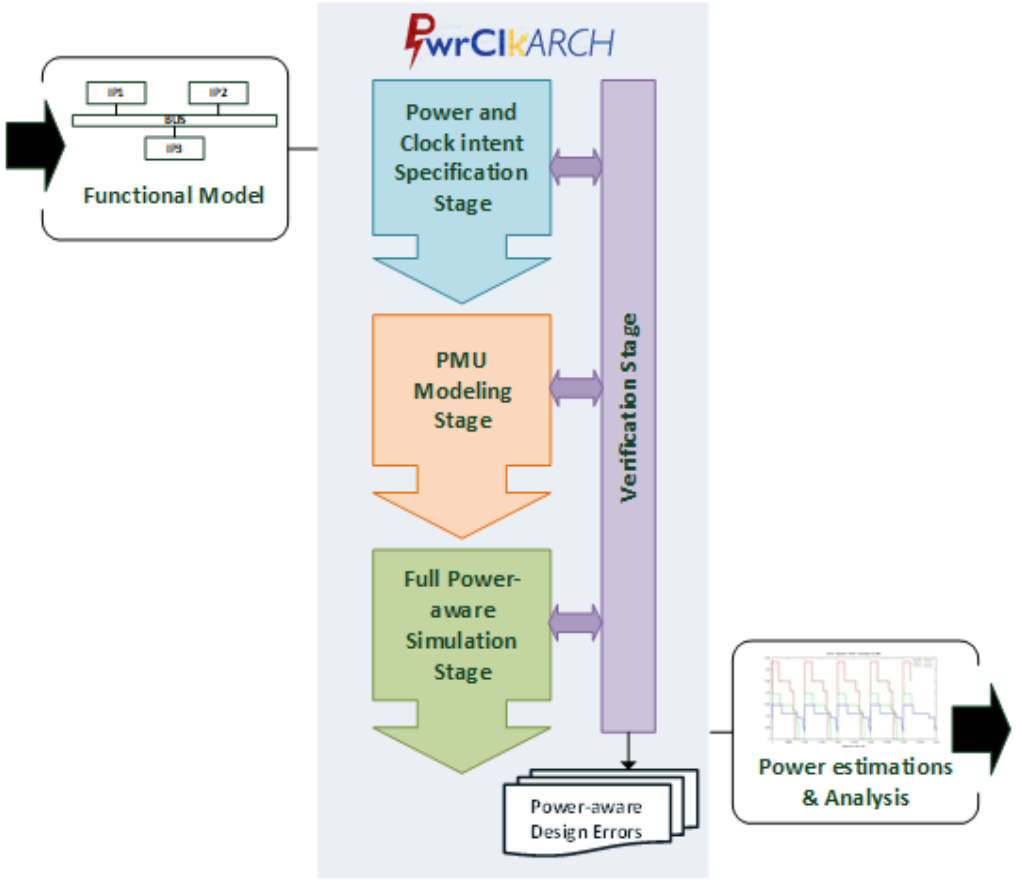
PwClkARCH library

1. Decomposition of the architecture into different **power domains** and **clock domains.**
2. **PMU** implementation in SystemC-TLM that interfaces the functional and the power models.
3. **Simulation** of the complete architecture and the generation of power results.
4. **Verification** of the **consistency** between the power management properties and the functional behavior.



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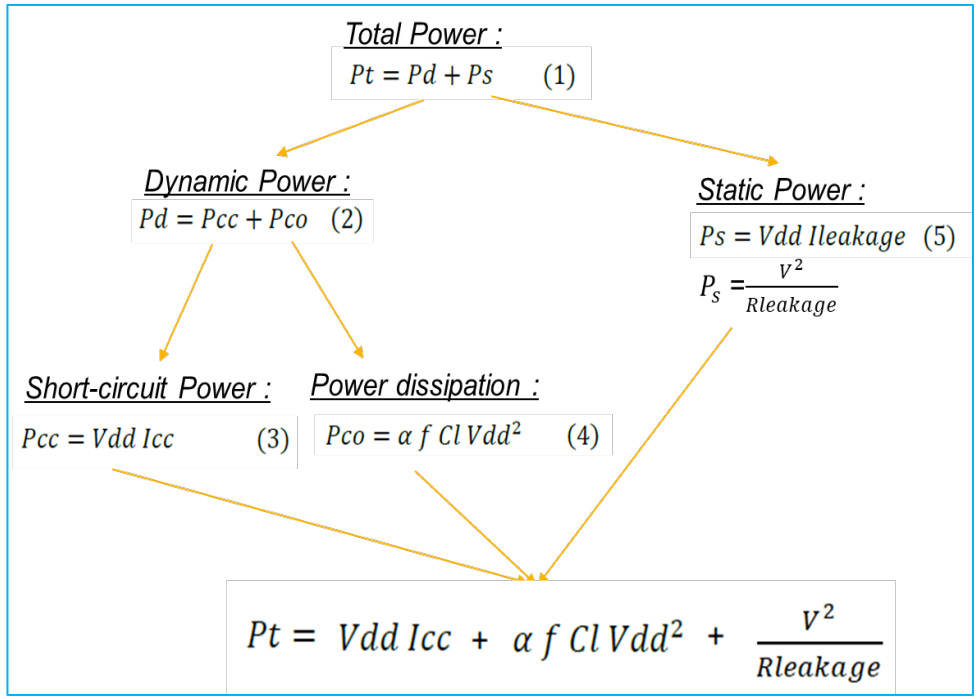
PwClkARCH library

```
SC_HAS_PROCESS(Interconnect);
Interconnect(sc_core::sc_module_name name,protocol::bus_type UsedProtocol,
        arbitration::ArbiterSettings arbiter_settings, sc_core::sc_time clk_period)
{
  #ifdef PWARCH
  sc_core::sc_object& obj = dynamic_cast <sc_core::sc_object&>(*this);
  m_PowObserver = new Observer<sc_core::sc_object>(obj,"_ob");
  this->attach(*m_PowObserver);
  de = Design_elem::get_DE(obj);
  SC_THREAD(checkActivity);
  #endif
}
```

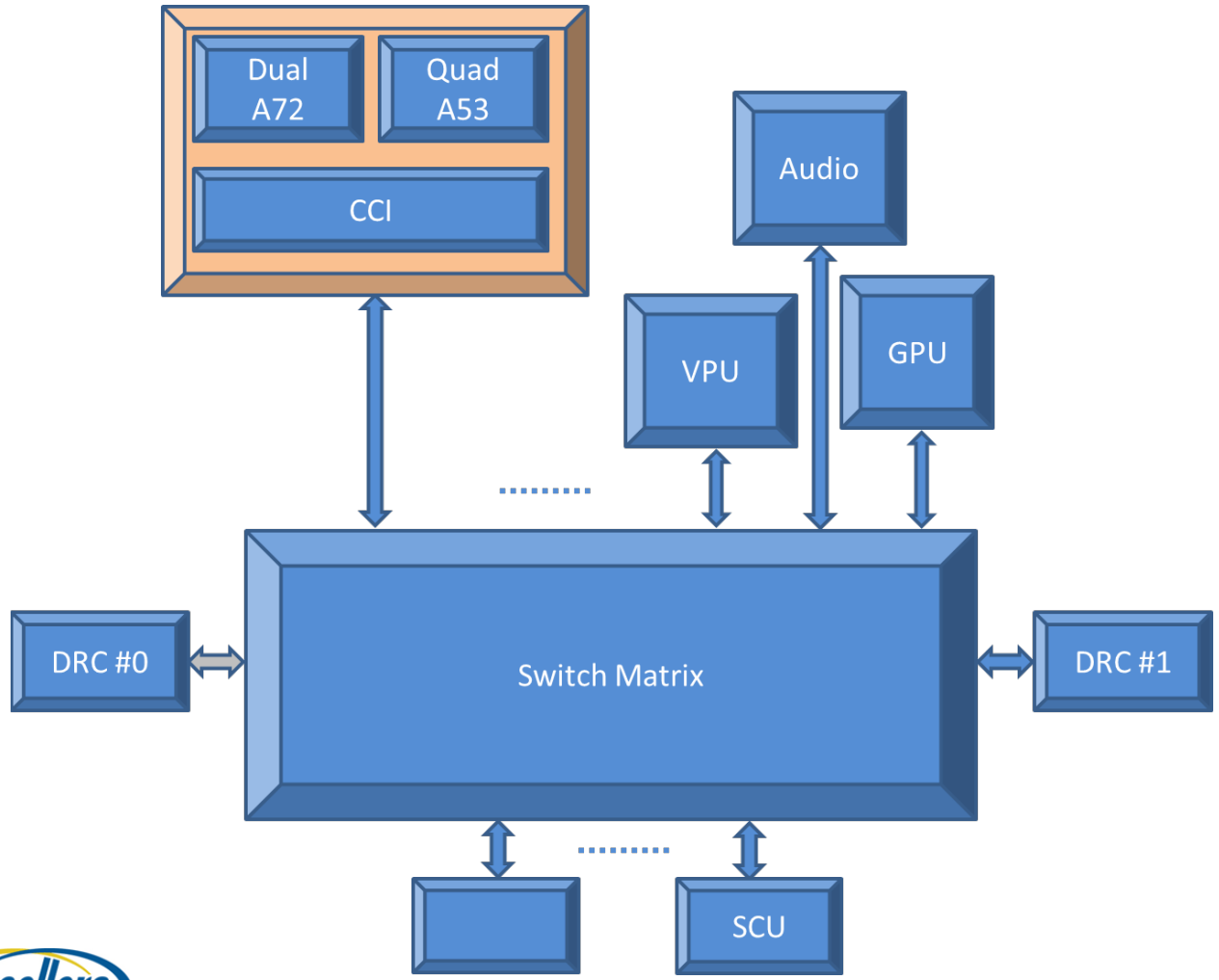
```
void checkActivity()
{
        while(true)
        {
                wait(m_ActivateEvent);
                de->set_functional_state(false);//ACTIVE
                de->Update_dpow(1.0);//Set the activity factor

                wait(m_DeactivateEvent);
                de->set_functional_state(true);//IDLE
        }
}
```



Design Element

If consumption changes
Then update power

Design under test - description



- NXP i.MX8QM SoC
- Many Subsystems
  - Audio, VPU, GPU, CPU, SCU …
- **Switch Matrix** – Connection of all subsystems

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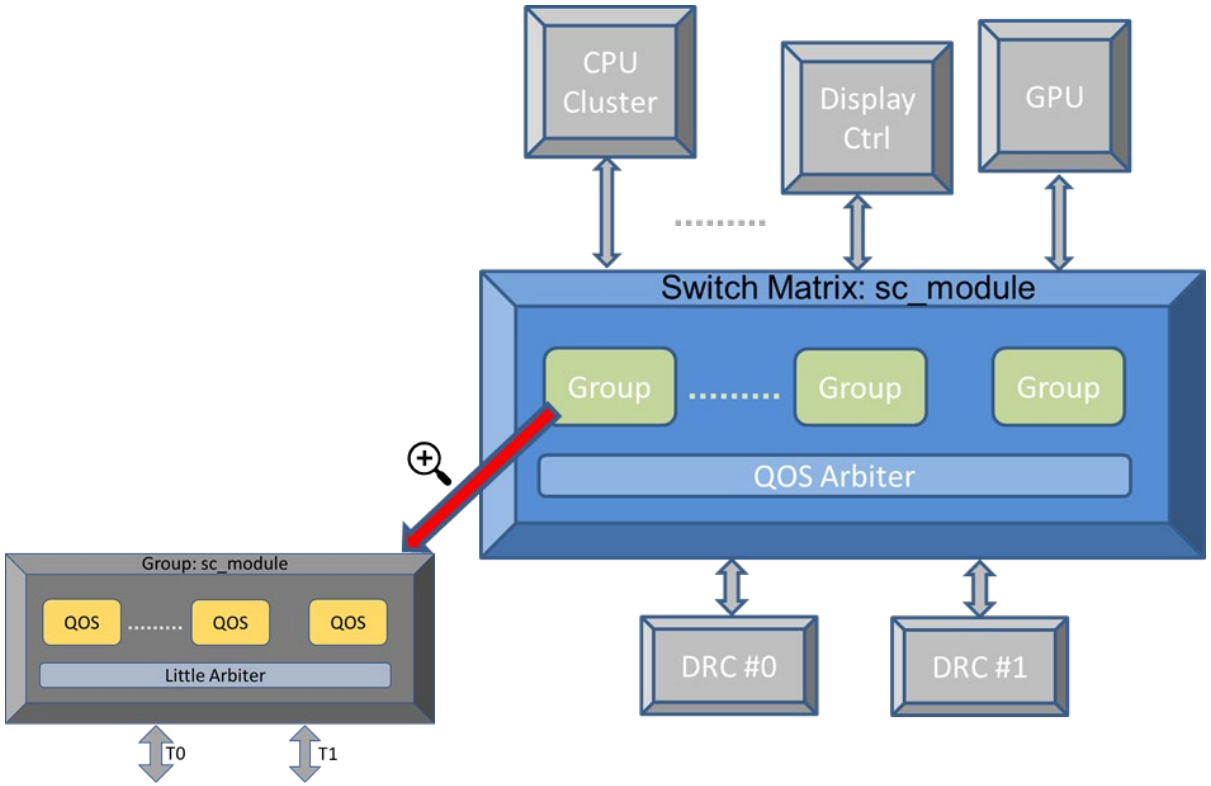
Design under test - description

Switch Matrix



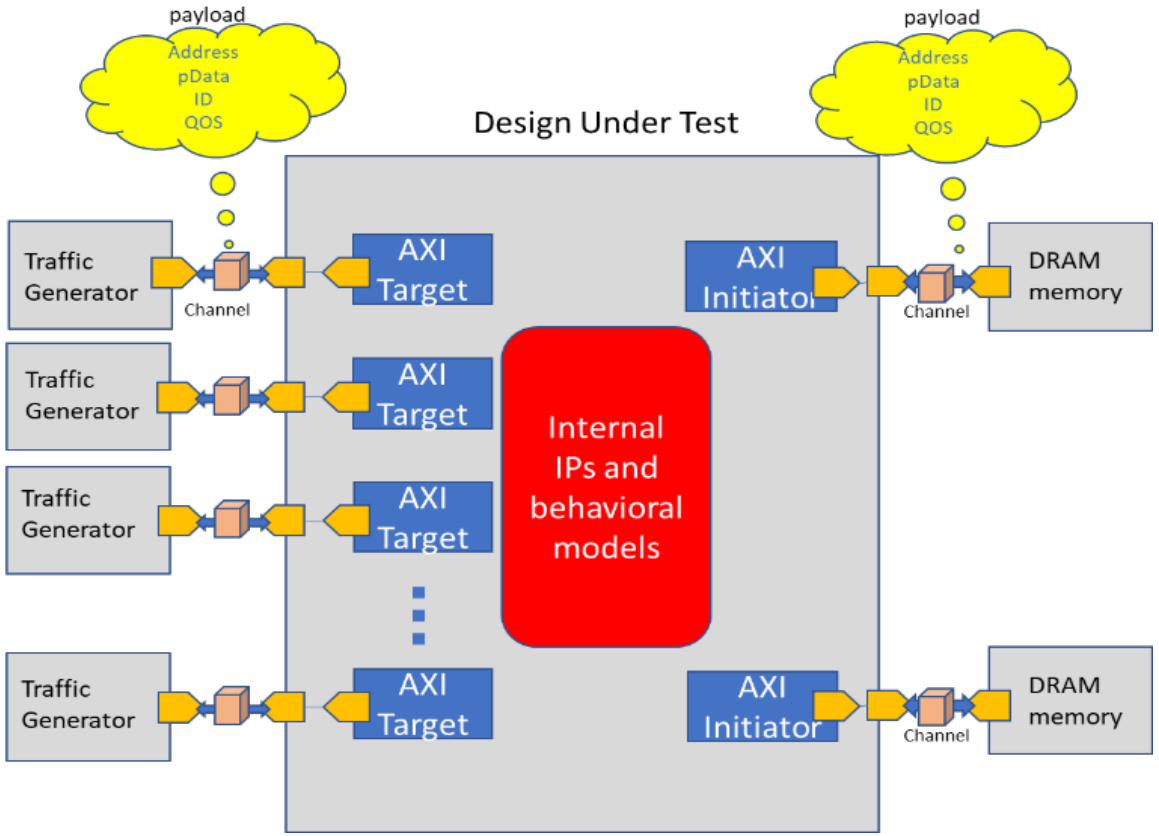
- Interconnection module
- Implements multiple QoS and routing algorithms
- Contains multiple sub-blocks
- **~5** power domain
- More than **25** clock domains

auto clock gating

+

power gating

Design under test - testbench



- The stimuli come from generic or application-specific Traffic Generators (SystemC initiator modules)
- Two DRAM memory models

DRAMPower

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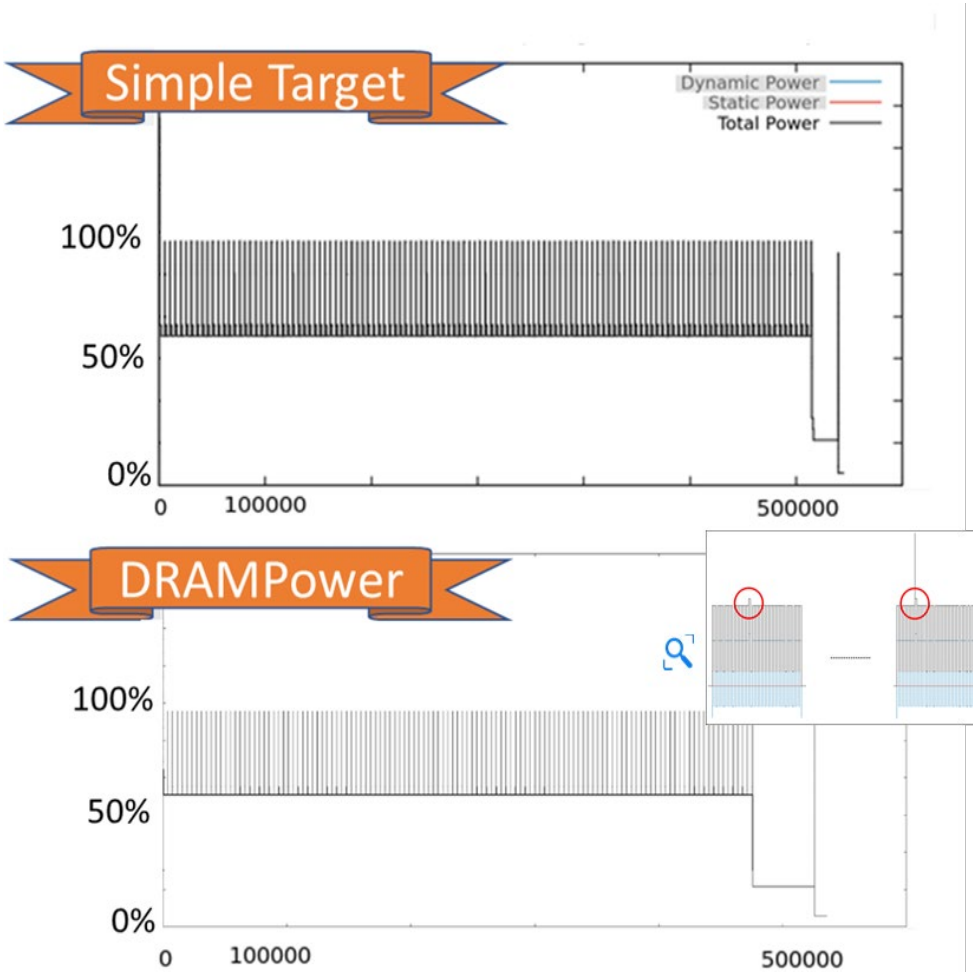
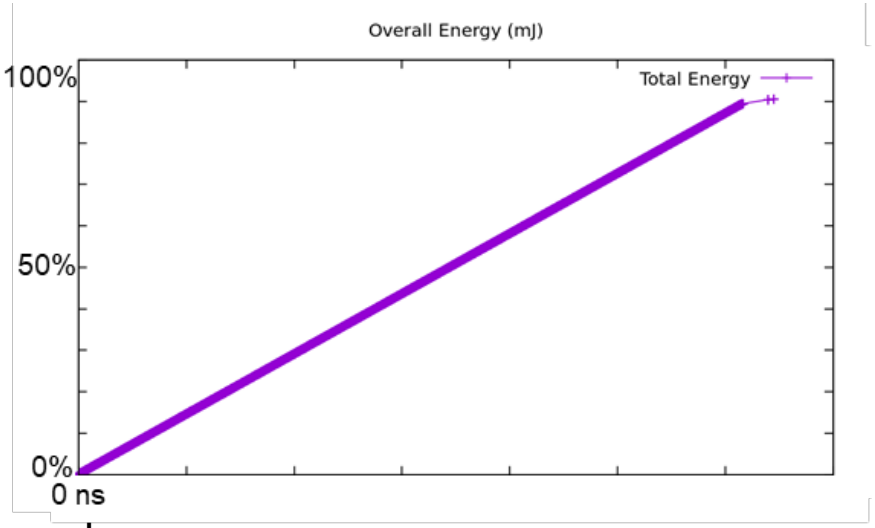
MemCopy 256KB





- 256KB DRC read accesses
- Each data access is 16 bytes
- Sequential memory accesses (prev_addr+32bytes).
- 4K interleaving applied in order to optimize the memories usage.
- The spikes come from the moments of interleaving between the two memories.

- Good power consumption silicon correlation

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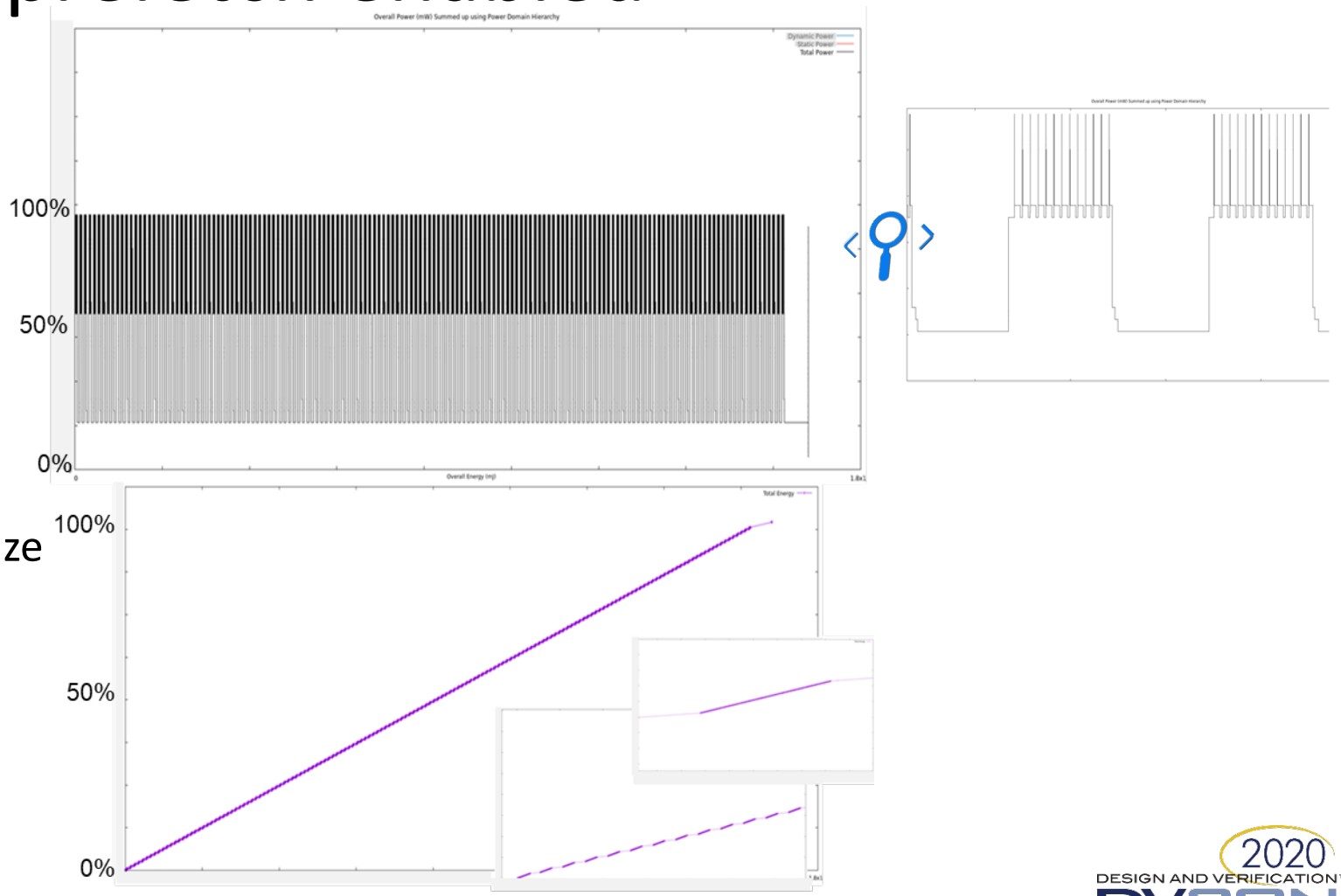
Display Refresh HD1080-1920x1080@60-32b with DC prefetch enabled

- One frame of transactions.
- Only one Group/QOS is used.
- Data paths are 256 bits.
- Pixel size 32 bits.
- Pixel frequency 138.5 MHz.
- Refresh rate 60Hz (Frame rate 60fps).
- Each data access is 32 bytes and we consider sequential memory accesses.
- 4K interleaving applied in order to optimize the memories usage.



- Good power consumption silicon correlation

Silicon correlation

Power distribution	Silicon/Simulation correlation
Switch Matrix dynamic power	85 - 99.5%
Switch Matrix static power	85 - 90.9%
2 DRC dynamic power	90 - 99.9%
2 DRC static power	90 - 96.1%
Total power under 1.1V	88% – 98%

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Conclusion

Comparing to previous PwClkARCH utilization:

1. Complexity of the functional model is tripled.
2. The number of design elements and clock domains is significantly increased.
3. Timing-aware functional model - Approximately-Timed (AT) Transaction Level Model (TLM) coding style.
4. The extracted power related metrics present a promising correlation with silicon measurements.

PwClkARCH performances:

1. Easily implemented on complex NXP IP.
2. Promising early stage power consumption silicon correlation.
3. Quick bugs detection/evaluation/correction.

Importance of industrial collaborators for PwClkARCH:

1. Industrial testing and proof-of-concept.
2. Maturation.
3. Bugs detection and correction.
4. Further add-on ideas.

We are searching for more collaborators interested by this new technology (PwClkARCH)

Contact: francois.verdier@univ-cotedazur.fr

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Thank You!
Q&A