Test driving Portable Stimulus at AMD

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Agenda

- Why Portable Test and Stimulus Standard (PSS)
- Walk through an example scenario
- PSS guideline
- Observations and conclusion
Why Portable Test and Stimulus Standard (PSS)

• Ease of test creation
  – New test scenarios find bugs
  – Declarative syntax with procedural support, C++ description
• Formal system description
  – Constraints, input/outputs, resource and randomization
    • UVM but for system-level and better
  – Automation for test generation
• Close approximation of real world scenarios
  – Deterministic runs
  – Ease of issue reproduction on emulator and simulation
• We used PSS tool Perspec™ from Cadence Design Systems for this exercise
## Existing stimulus

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<tr>
<th>Post-silicon</th>
<th>Pre-silicon SoC</th>
<th>Pre-silicon IP</th>
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| • Generally OS-based tests  
• Longer debug time  
• Failures are difficult to bring to emulation or simulation for debug | • Simple directed feature tests  
• Difficult to manually create complex scenarios  
• Long run time for complex scenarios | • Excellent UVM-based constrained random testbench  
• IP initialization sequences not easily portable to FW or post-silicon tests  
• IP level tests lack system context |
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<th>Pre-silicon SoC</th>
<th>Pre-silicon IP</th>
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<tbody>
<tr>
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<td>• Smaller deterministic bare-metal tests</td>
<td>• Describe test intent with PSS</td>
<td>• Reuse SoC scenarios</td>
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<td>• Compose complex scenarios</td>
<td>• Automation helps with complex scenario composition</td>
<td>• Export initialization sequences to firmware and post-silicon</td>
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<td>• Easily bring debug to Emulation</td>
<td>• Reuse tests post-silicon</td>
<td>• Export IP specific scenarios to SoC</td>
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<td>• Generate large set of tests for regression</td>
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Test environment

• PSS generated tests run on UEFI BIOS
  - Test are loaded and started by uDREX
    - uDREX is a thin layer to abstract BIOS and provide services to PSS tests
• Emulator
  - Test and uDREX are backdoor loaded into DRAM
• Post silicon
  - Test are copied in a known location on disk
  - uDREX finds and starts test on all enabled threads
Example test scenarios

• Processor C-states scenarios
  – Transition all cores in all complexes to a C-state at same time
  – Transition one specified core to a C-state
  – Sequentially transition cores to a C-state on all complexes
  – Transition cores in and out of a C-state at specified duty cycle
This timeline shows all interesting points an interrupt can arrive during C-state transitions. All these points matter for system-level power scenarios.
Generic power down core activity

```plaintext
action power_down_core {
    rand int in [0..NUM_CORES-1] core_num;
    rand bool wakeup_core;
    rand bit[32] usr_delay_ms;
    rand cstate_e in [CoreC1, Core_C2] goal_cstate;

    activity {
        sequence {
            do observe_system_state;
            do enable_cstate with {
                core_num == this.core_num;
                goal_cstate == this.goal_cstate; }
        }
        parallel {
            do power_down_thread with {
                core_num == this.core_num;
                thread_num == 0; }
            do power_down_thread with {
                core_num == this.core_num;
                thread_num == 1; }
        }
    }
}
```
Four cores transition to a C-state then wake-up at same time.

Timer count was constrained by PSS tool based on current clocks.
Generating Test Code

void core0_thread0_main() {
    for (i=0; i<50; i++) {
        enable(Core_C1);
        program(18);
        set_timer(32);
        asm("hlt");
    }
}

void core0_thread1_main() {
    while (!end_of_loop_body) {
        set_timer(32);
        asm("hlt");
    }
}

exec body C = """
enable({goal_state});
program({val});
"""

exec body C = """
set_timer({delay});
"""

exec body C = """
asm("hlt");
"""
action sweep_scenario {
    rand int in [0..NUM_CORES-1] core_num;
    rand int in [1..10000] range;
    rand int in [1..1000] step;
    rand int in [1..1000] base_delay;
    activity {
        parallel {
            replicate (i: NUM_CORES) {
                if (i != this.core_num) {
                    do power_down_core with {
                        core_num == i;
                    };
                };
            }
        }
        repeat (phase: range / step) {
            repeat (2) {
                do power_down_core with {
                    core_num == this.core_num;
                    goal_cstate == CPU_C1;
                    transition_case == SWEEP;
                    wu_delay == base_delay + phase * step;
                };
            }
        }
    }
}
Power-state transition measurement
PSS Modeling Guidelines

- Create actions to bring system to known state
  - Encapsulate known state into state object
- Activities that depend on a system feature need to enable the feature using *inputs* or by explicitly using an action
  - All generic actions in library should come with control knobs that have sensible defaults
- Project configurations should come from static configuration files
- Separate generic PSS code from project specific PSS
PSS - Real world observations

• Generic action/activity can be complex to create
  – May need procedural description
• Input/output for activities not available yet
• PSS tests prefer complete control of system
  – Baremetal environment
  – Statically allocated and scheduled tests
• Randomization should be carefully thought through
  – Test generation time has potential to increase exponentially
• Constraint solver errors can be terse
• Multi-discipline team collaboration needed to create baremetal library
PSS - Conclusions

• Excellent capability for composing test scenarios
  – Lab bring-up engineers or architects can easily craft scenarios and compose them quickly
    • Ease of creating scenarios with PSS declarative syntax leads to many new scenarios

• Partial scenario description of activity
  – A test creator doesn’t need to know all prerequisites

• Runtime and test generation time coverage reports
  – Very helpful in closing coverage gaps

• Constraints in PSS
  – Provide a concise and precise way to specify system and tests

• Augmented power management firmware tuning tests in lab with new scenarios from PSS
  – Quickly generated new scenarios in lab
  – Improved power management algorithms

• We can use PSS beyond power management verification and tuning
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