2019 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

Taking RNM Model to the Next Level: Power-Aware Verification of Mixed-Signal Designs

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accellera SYSTEMS INITIATIVE

Agenda

- Introduction
- Low power verification challenges
- Traditional verification approach
- RNM-based approach
- Bugs found
- Conclusion

Introduction

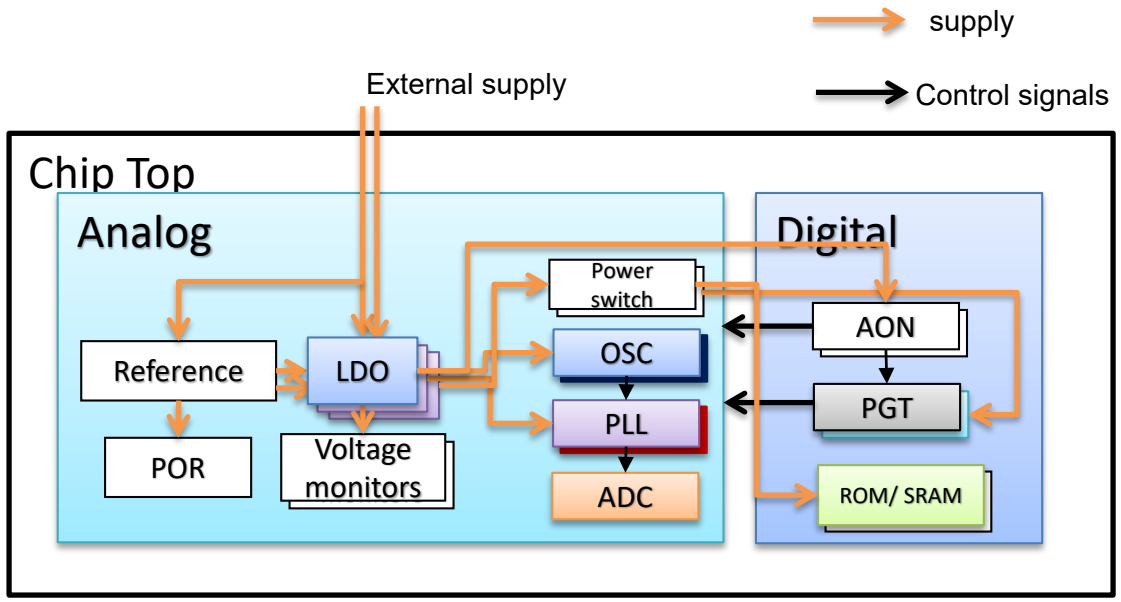
- Every new generation of electronic devices requires higher performance and more sophisticated power management.

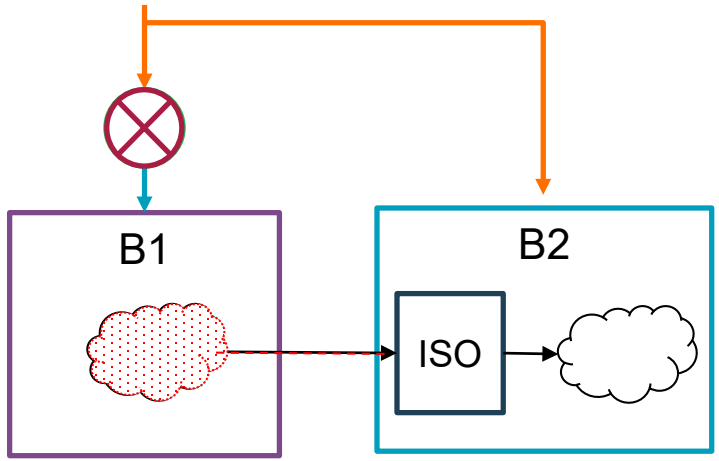
- This poses an exponentially growing verification challenge, especially in the mixed-signal domain

LOW POWER VERIFICATION CHALLENGES

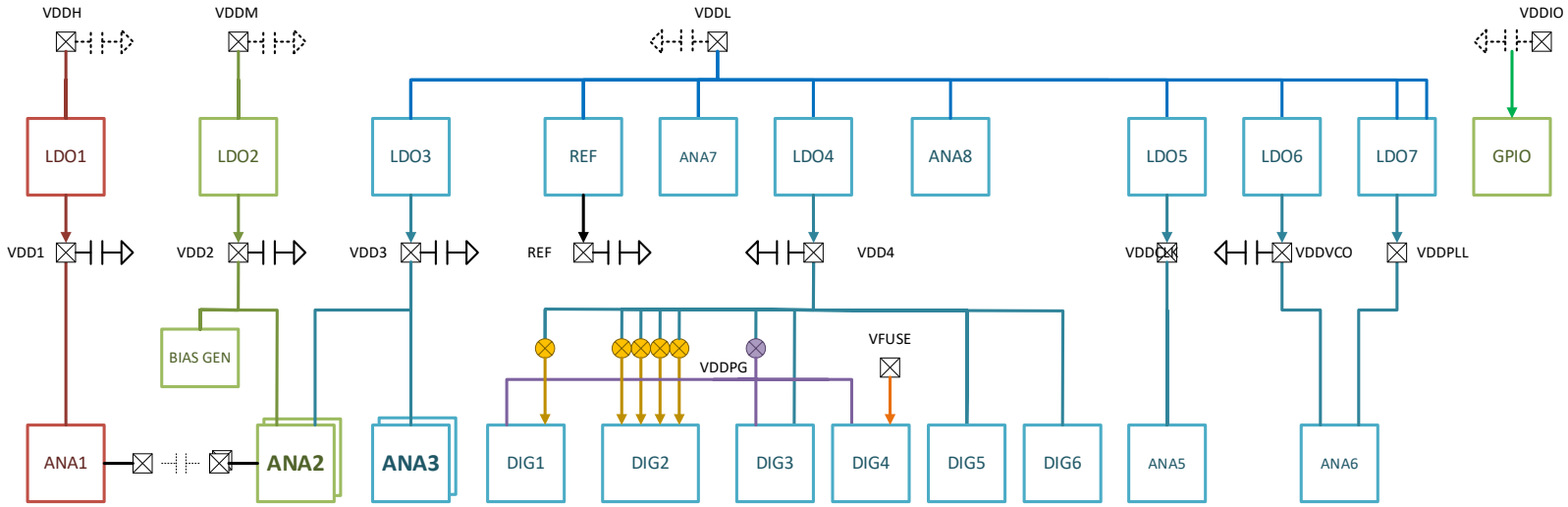
Mixed Signal Interactions

- Interactions of digital controllers with analog blocks such as
  - References, LDOs, Voltage monitors, Analog Power Switches
  - Power-on circuitry, Clock sources, etc.
- Isolation/Clamp values of the control signals during power up and other power modes must be carefully selected and verified





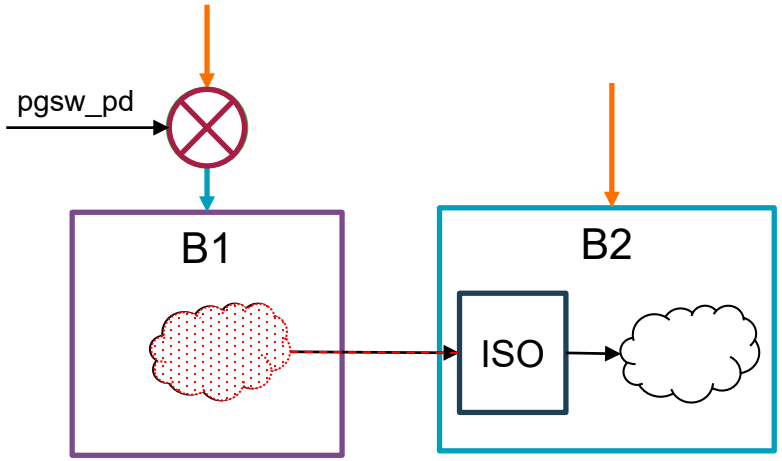
Complex Power Mode Transitions

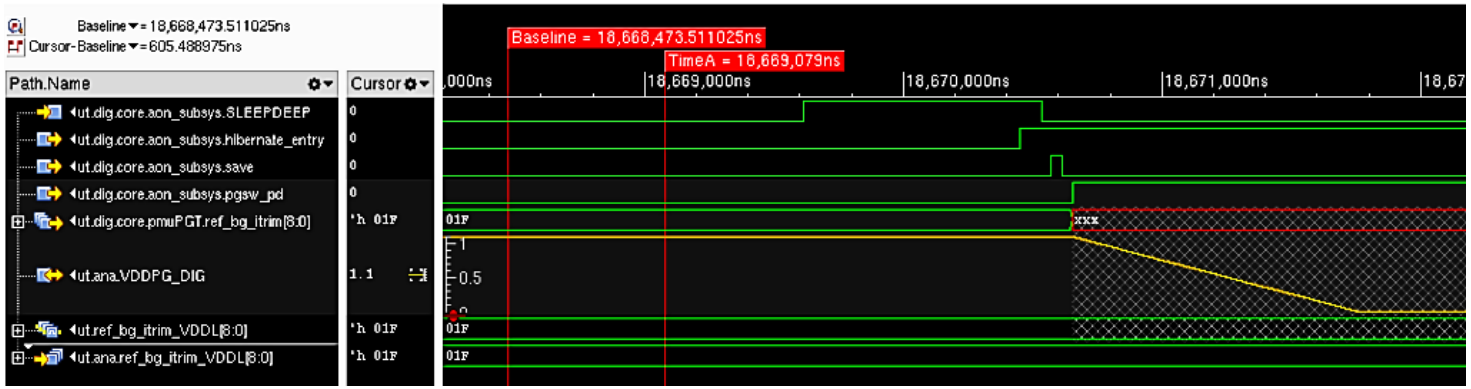


TRADITIONAL VERIFICATION APPROACH

Digital simulations

- CPF/UPF power aware simulation
- Simple non-pin compatible Verilog model for analog
  - Effects of power transitions on analog is not verified thoroughly
  - Isolations between analog power domain is not verified



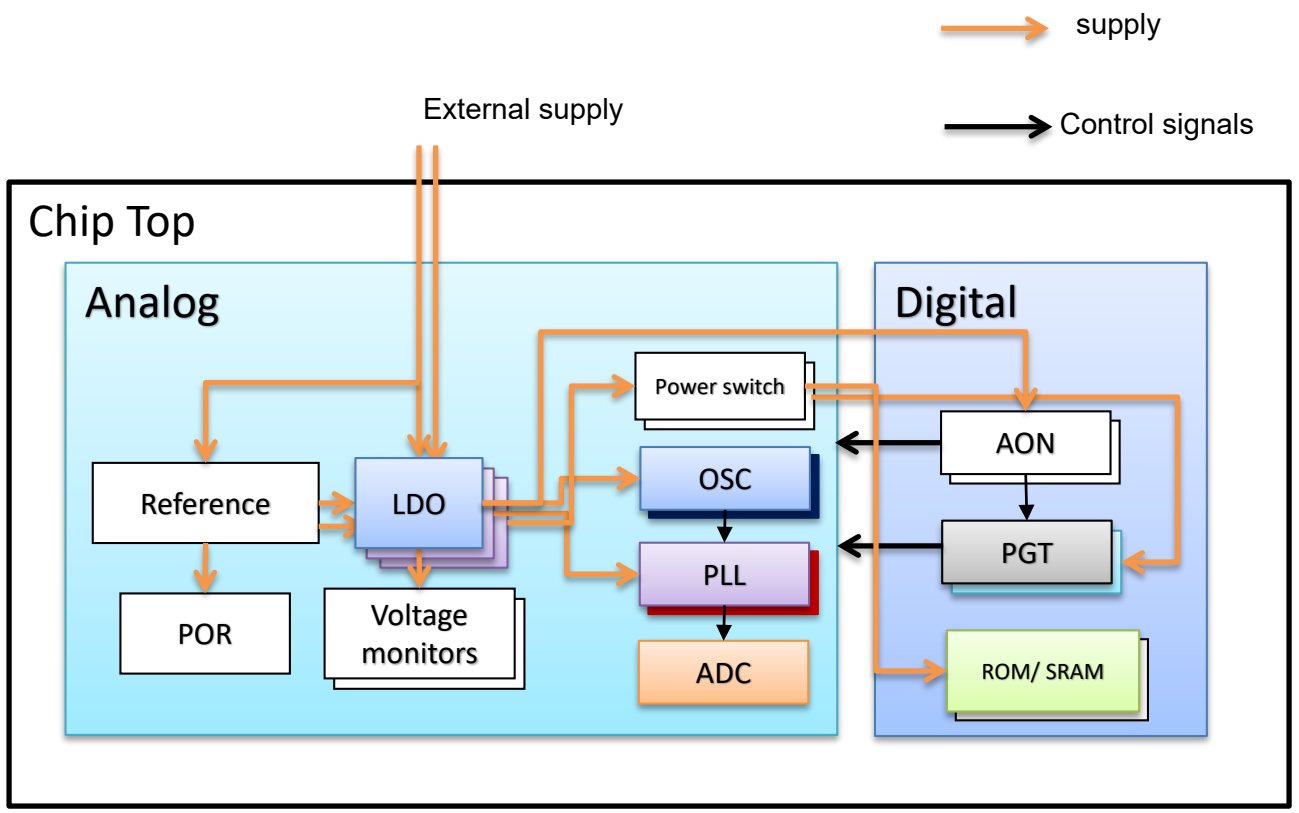


Reliance on Cosim

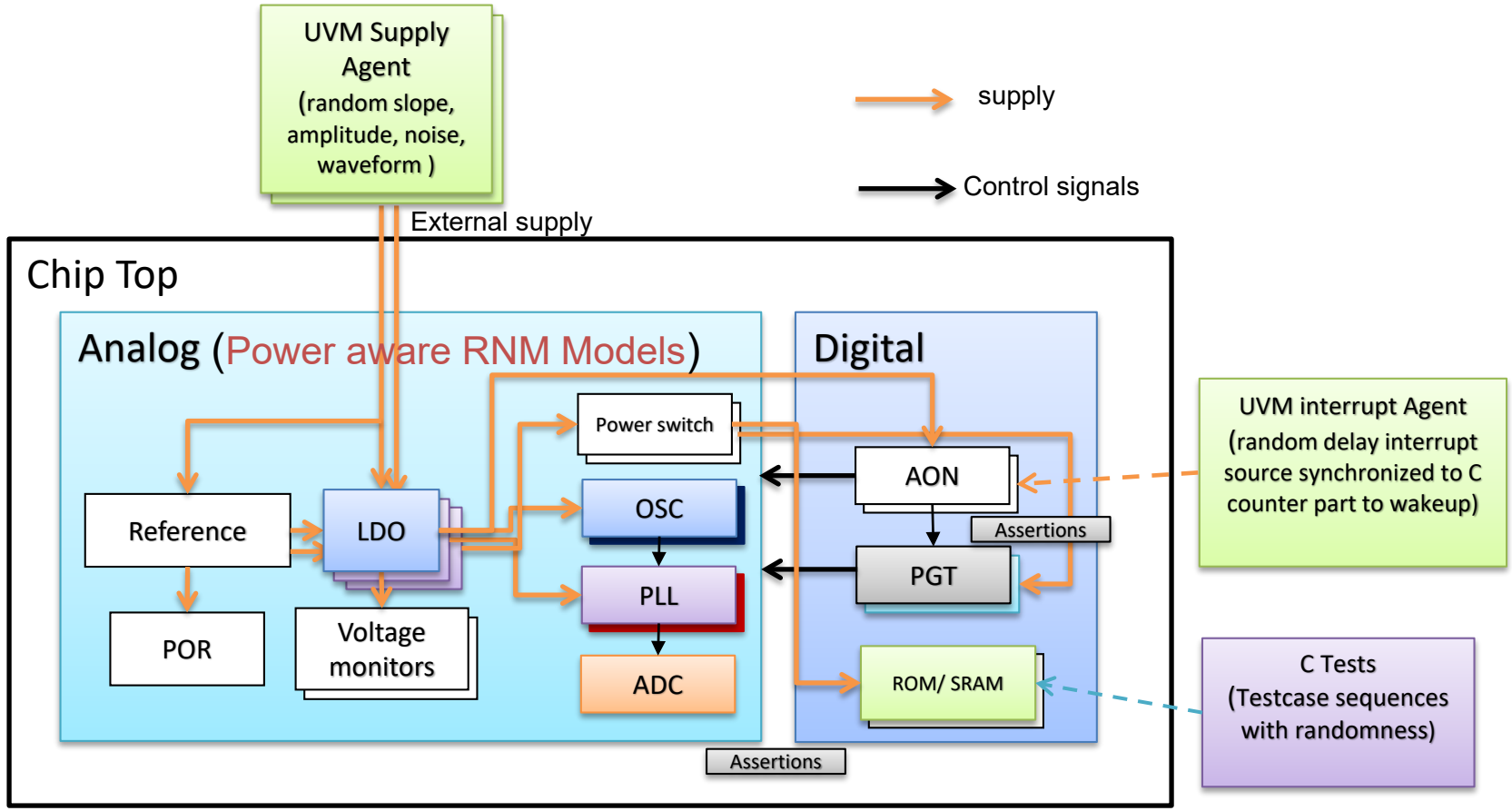
- Cosim for signing of Low power(mixed signal) verification
  - Slower Bring-up of Cosim Verification Environment as compared to digital DV
  - Large turn-around time of cosim runs
  - Coverage closure can be achieved only after merging digital and cosim dumps
  - Finding bugs towards the end (one of the long pole in all previous projects)

RNM-BASED APPROACH

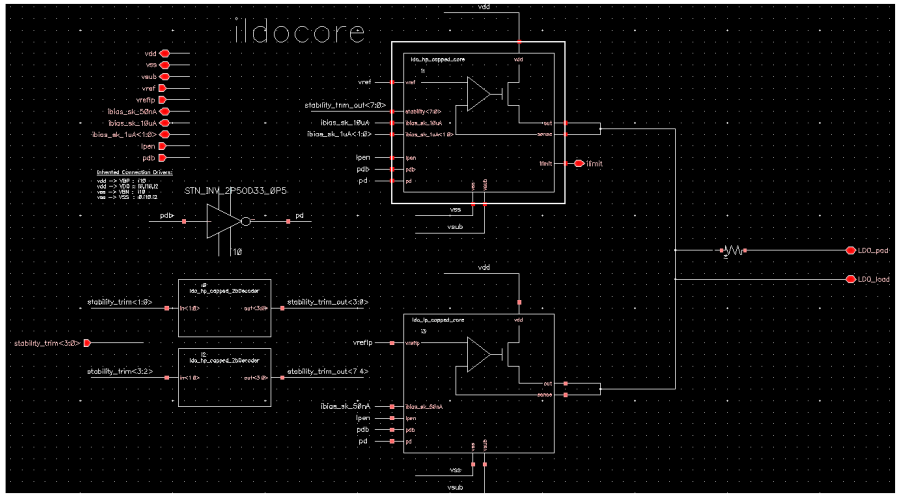
Simplified Design



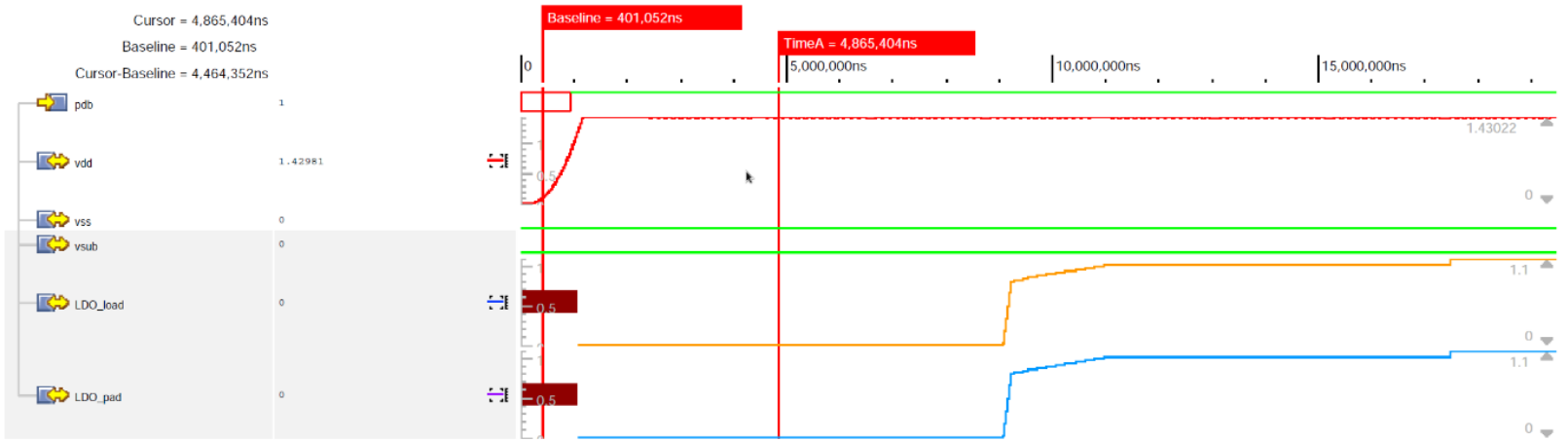
Verification Environment



Real number modelling



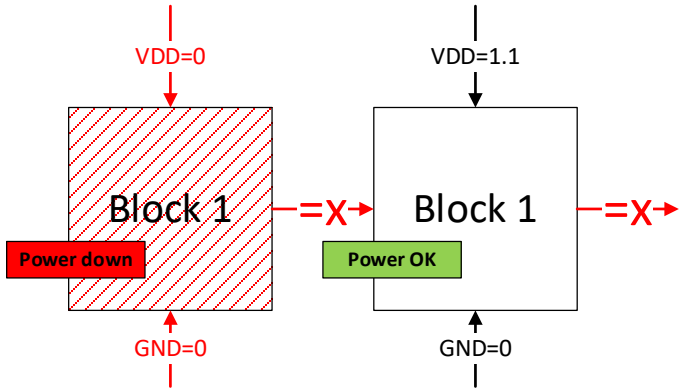

```
...
real out_int;
assign out_int = limit(out_int + I_ldo * step_size/Cl, .min(0.0),
.max(vref));
...
function real limit (input real in, input real min, input real max);
limit = (in > max) ? max : (in < min) ? min : in;
endfunction
```



Power awareness

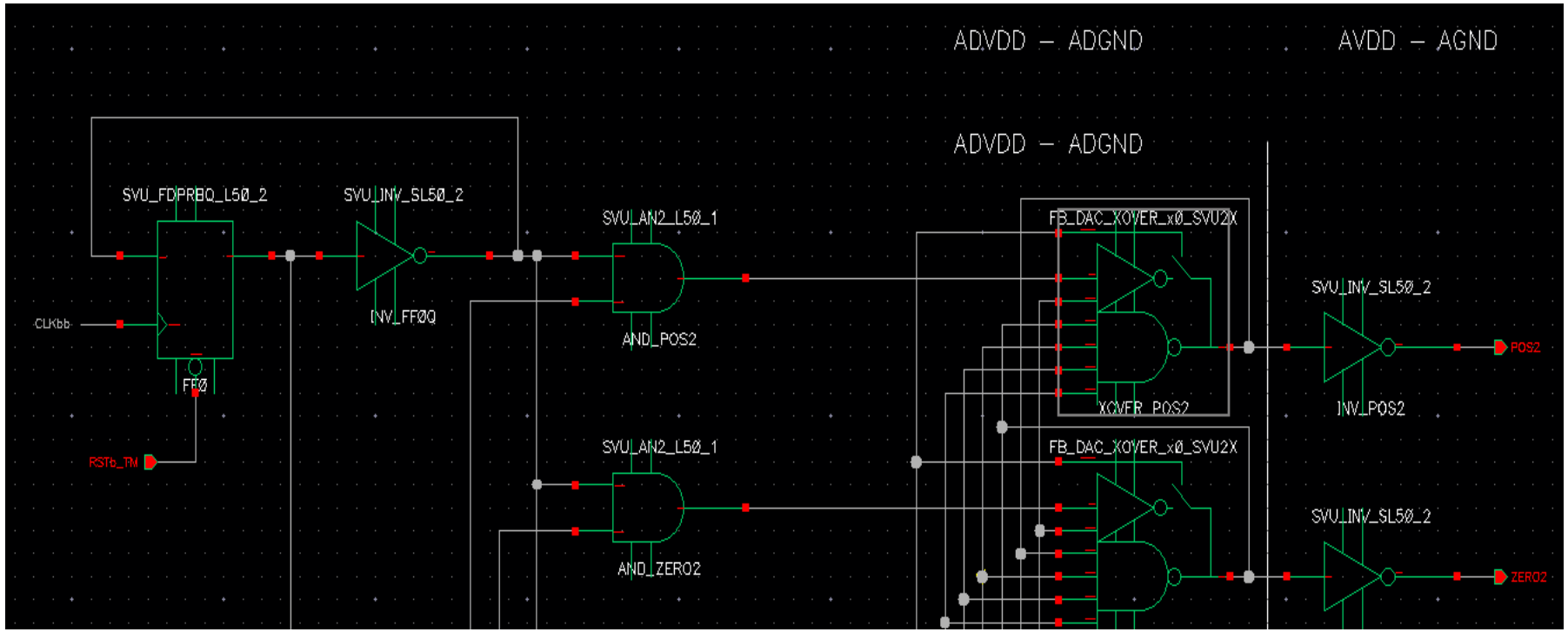
```
assign out_int = limit(out_int + I_ldo * step_size/Cl, .min(0.0), .max(vref));

assign out = (valid_inputs && bias_good && pwr_good) ?
             ( (pdb === 1'b1)? out_int : `wrealZState ): `wrealXState;

function real limit (input real in, input real min, input real max);
   limit = (in > max) ? max : (in < min) ? min : in;
endfunction
```

```
inout vdd;
cds_rnm_pkg::wrealsum vdd;
always @(*)
if ((vdd !== `wrealXState && vdd !== `wrealZState) && (vdd >= vddl_min)
                  && (vdd <= vddl_max) && !vss && !vsub )
   pwr_good <= 1'b1;
else
   pwr_good <= 1'b0;
```

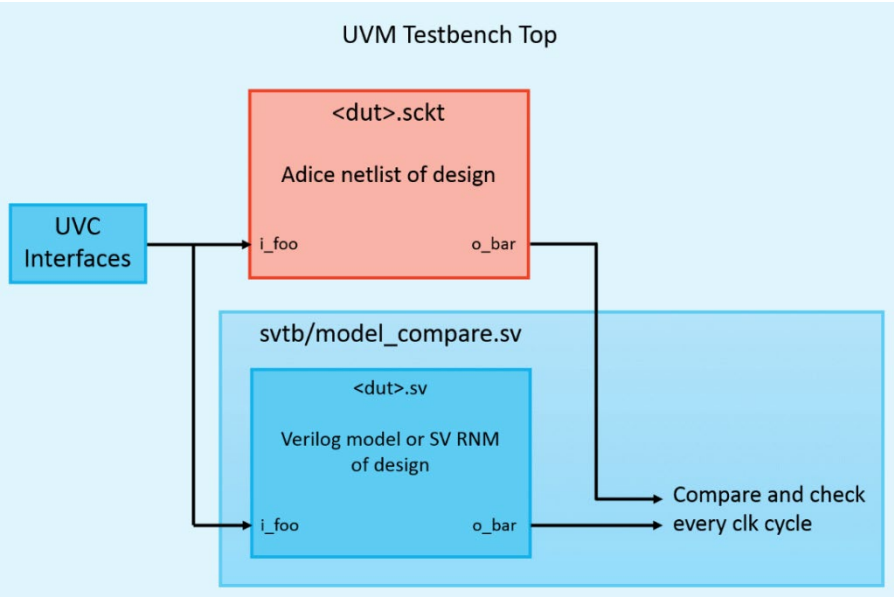


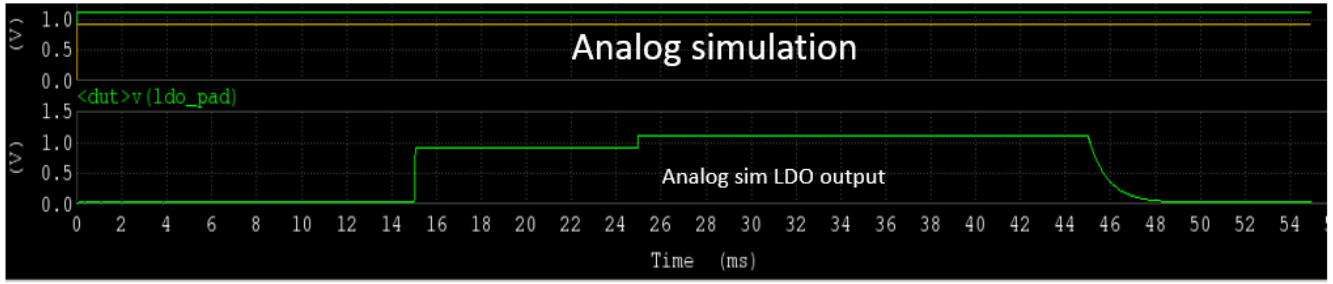
Netlisting

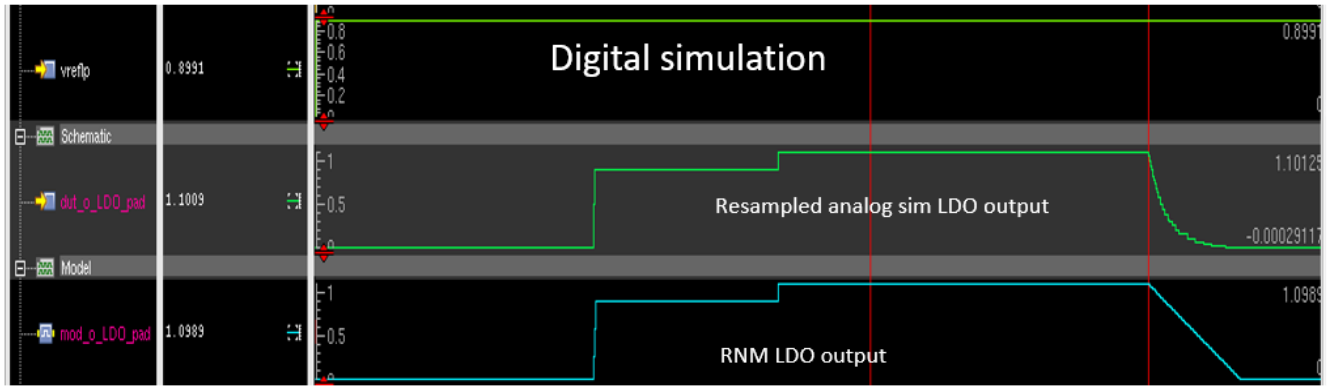
- Standard cell Netlisting , no modelling required



Model validation

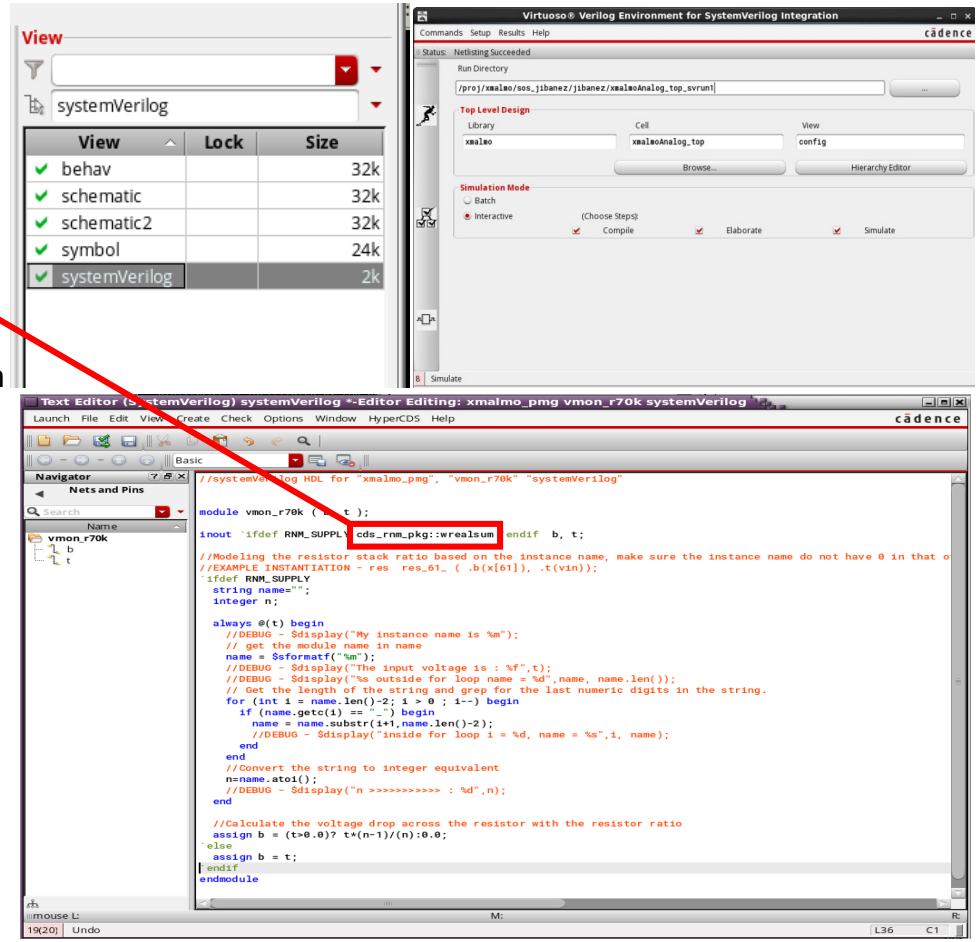




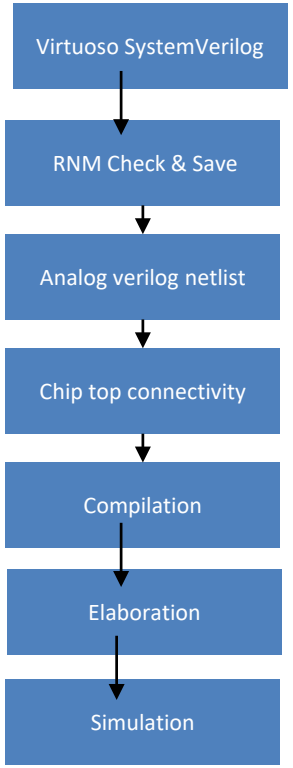


RNM Flow

- SV RNM stored in Virtuoso as “SystemVerilog” view
  - Usage of Cadence built-in nettypes from cds_rnm_pkg::wrealsum
- RNM Check & Save
  - Pin matching hierarchical checks
- Analog Verilog Netlist
  - Pin compatibility ensured during netlist process
  - Netlist using config views with Cadence SV Plugin
- Chip Top Connectivity
  - Updated through scripting, no human interaction
  - All digital islands exposed DMS hierarchy
- Compilation/Elaboration
  - Discipline resolution, datatype coercion and connect module insertion solved In order during elaboration.
- Simulation
  - Validation flow against Schematic
  - Model usage in DMS environment



Flow

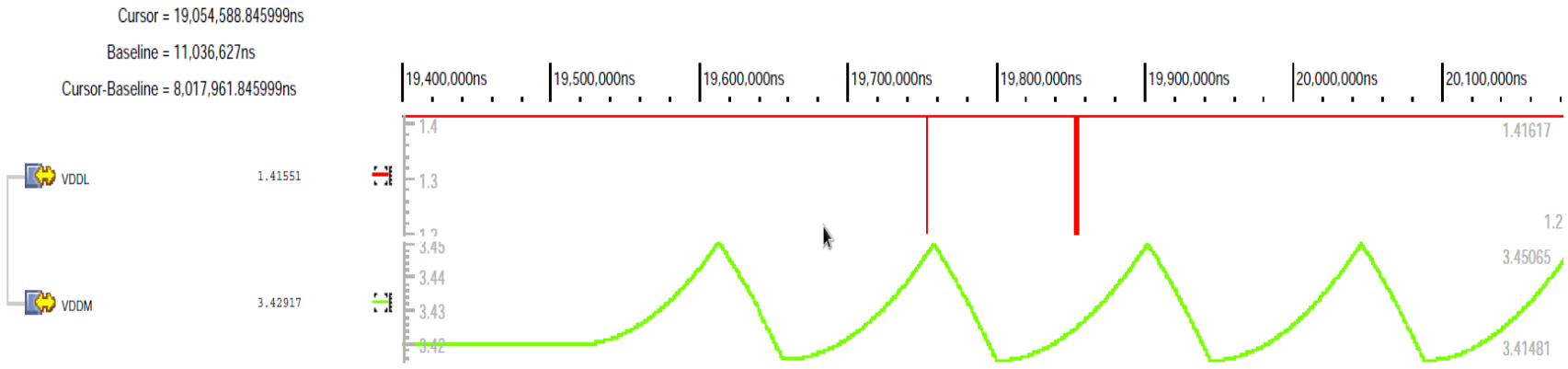


Integration of RNM with digital RTL

- Using datatype coercion
  - Connecting the models to the rest of design/testbench without worrying about the interconnects and their types.

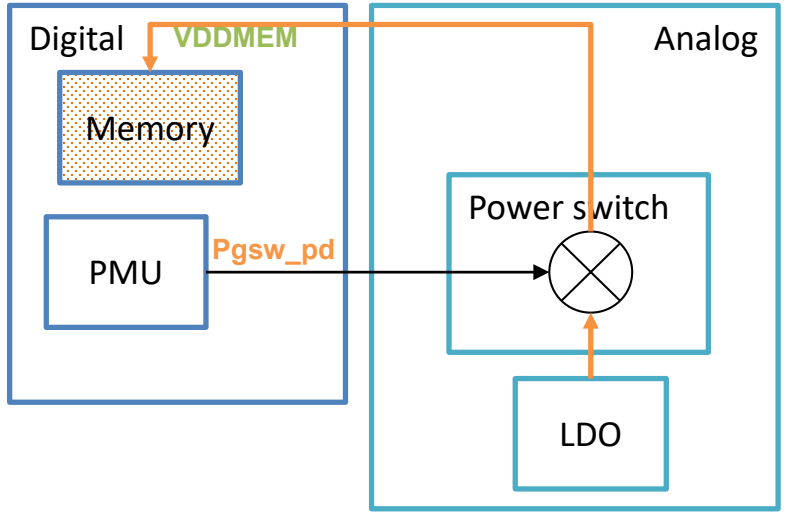
Driving supply from Testbench

- Supply agent generating glitches, over-voltage and under-voltage scenarios



Other techniques used

- Actual supply from the RNM model is used as a shutoff condition for a power domain.
  - more accurate behavior of power gating (timing wise).
  - Verification of analog logic from the power switch digital control to the actual output of the switch (LDOs in many cases).

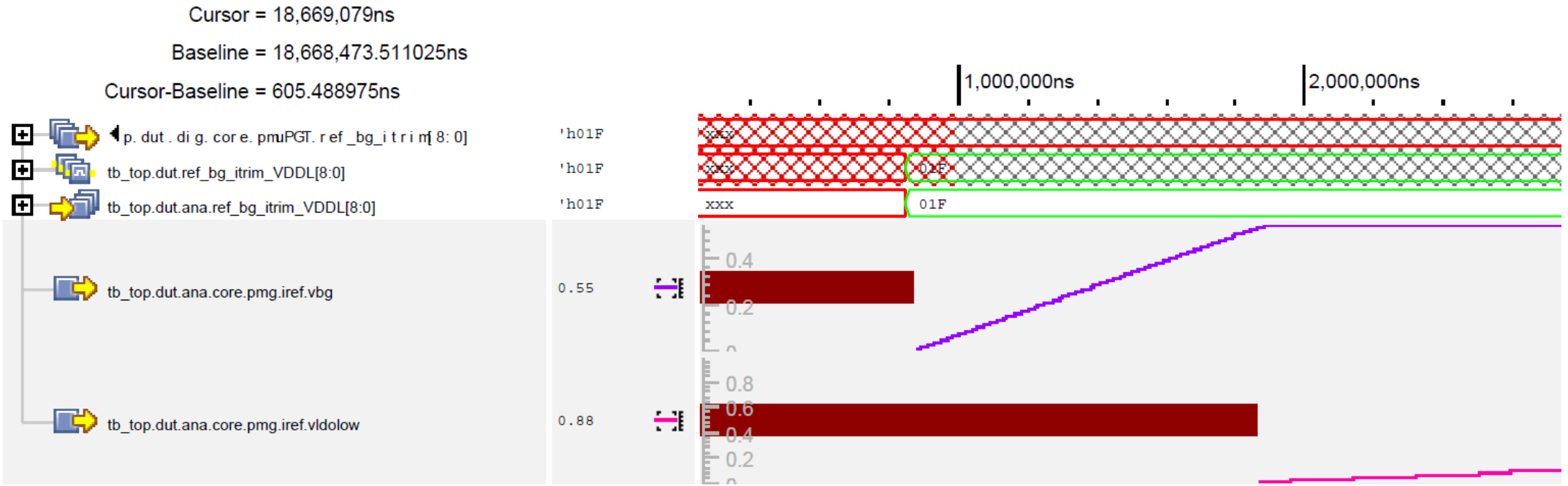



```
# Core domains
 if {$env(SIMULATION) == "false"} {
   create_power_domain -name PD_VDDMEM     -instances $Mem_Insts
              - shutoff_condition "!${dig_scope}pgsw_pd“

else {
   create_power_domain -name PD_VDDMEM     -instances $Mem_Insts
              - shutoff_condition "!${dig_scope}VDDMEM"
}
```

BUGS FOUND

Wrong isolation values

- Wrong isolation values leading to POR or wake from sleep failures.



Analog block sequencing

- Wrong analog block sequencing leading to power mode transition failures.
  - PLL not working after a power mode wakeup
  - Digital power failure on one of the power mode transition.

ADVANTAGES IN THE NEW FLOW

Exhaustive Isolation Verification

- Power aware RNM model are really powerful to catch most of isolation issues in functional simulation. Including the analog to analog isolation.
  - Wrong isolation values on TRIMs, LDO controller delays etc.
- Isolation assertion generated from spec (isolation spreadsheet)
- Isolation toggle coverage
  - Auto-generated from the isolation spreadsheet

	Block name	Pin name	Default state with with input supply absent	Power-gated blocks ISO / CLAMP cell power domain	Isolation enable signal	POR State of Signal	Load	Drive Buffer Type	STA Reference Clock	Sync Method	Debouncer / deglitch logic	Scan Controlled?	Scan Value
12	<Block1>												
17	<Block2>												
34	RX												
99	TX												
108													
109		hfosc_aon_clk_24meg_VDDCORE	Low		NA	1'b0				no sync	N/A	Yes	1'b0
110		hfosc_dig_clk_24meg_VDDCORE	Low		NA	1'b0				no sync	N/A	Yes	1'b0
111		hfosc_locked_VDDCORE	Low		NA	1'b0				no sync	N/A	Yes	1'b0
112		hfosc_aon_pdbar_VDDCORE	Low		vddpg_iso	1'b1			pclk	no sync	N/A	Yes	1'b1
113		hfosc_dig_pdbar_VDDCORE	Low		vddpg_iso	1'b1			pclk	no sync	N/A	Yes	1'b1
114		hfosc_pdbar_VDDCORE	Low		NA	1'b0				no sync	N/A	Yes	1'b0
115		hfosc_pll1_pdbar_VDDCORE	Low		vddpg_iso	1'b0			pclk	no sync	N/A	Yes	1'b0
116		hfosc_pll2_pdbar_VDDCORE	Low		vddpg_iso	1'b0			pclk	no sync	N/A	Yes	1'b0
117		hfosc_rstbar_VDDCORE	Low		NA	1'b0				no sync	N/A	Yes	1'b0
118		hfosc_freq_trim_VDDCORE	Low		vddpg_iso	8'h40			pclk	no sync	N/A	Yes	8'h40
119		hfosc_freq_tune_VDDCORE	Low		vddpg_iso	5'h08			pclk	no sync	N/A	Yes	5'h08
120		hfosc_test_en_VDDCORE	Low		vddpg_iso	3'h0			pclk	no sync	N/A	Yes	3'h0
121		pll1_out_dsp_40meg_VDDVCO	Low		adcpll_iso	1'b0			hfosc_clk	no sync	N/A	Yes	1'b0
122		pll1_spare_out_VDDPLL	Low		adcpll_iso	4'h0			hfosc_clk	no sync	N/A	Yes	4'h0
123		pll1_cp_pdbar_VDDPLL	Low		vddpg_iso	1'b0			hfosc_clk	no sync	N/A	Yes	1'b0
124		pll1_in_sel_VDDPLL	Low		vddpg_iso	1'b0			hfosc_clk	no sync	N/A	Yes	1'b0
125		pll1_lf_pdbar_VDDPLL	Low		vddpg_iso	1'b0			hfosc_clk	no sync	N/A	Yes	1'b0

Coverage Closure without Cosims

- Achieved 100% code and functional coverage

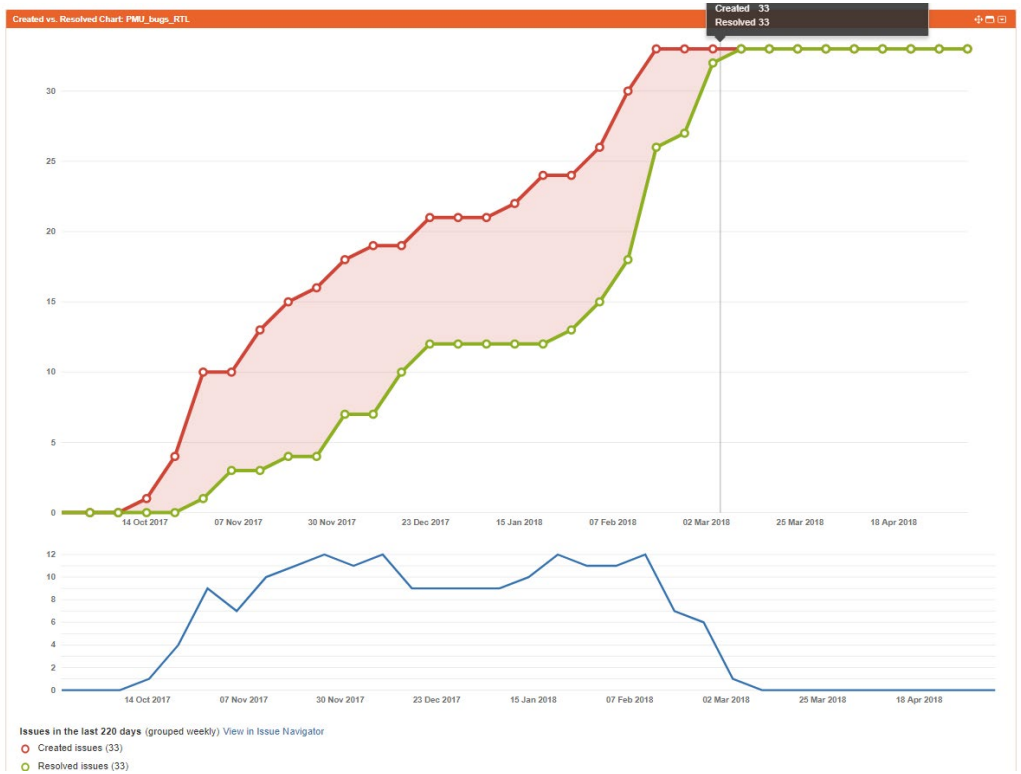
Name	Overall	Overall Covered	Block	Branch	Expression	Toggle	FSM	Transition	Functional	Assertion
aon_subsys	100%	4355 / 4355 (100%)	100%	100%	100%	100%	100%	100%	n/a	n/a
pmuPGT	100%	6748 / 6748 (100%)	100%	100%	100%	100%	100%	100%	100%	100%
u_A_D_ASSERTIONS	100%	9 / 9 (100%)	n/a	n/a	n/a	n/a	n/a	n/a	100%	100%
u_A_D_ISO_ASSERTIONS	100%	156 / 156 (100%)	n/a	n/a	n/a	n/a	n/a	n/a	100%	100%
u_A_D_POR_ASSERTIONS	100%	93 / 93 (100%)	n/a	n/a	n/a	n/a	n/a	n/a	100%	100%
u_A_D_scan_latch_assertions_immd	100%	436 / 436 (100%)	n/a	n/a	n/a	n/a	n/a	n/a	100%	100%
u_A_D_scan_latch_assertions_immd_prev	100%	83 / 83 (100%)	n/a	n/a	n/a	n/a	n/a	n/a	100%	100%
u_D_D_ISO_ASSERTIONS	100%	150 / 150 (100%)	n/a	n/a	n/a	n/a	n/a	n/a	100%	100%
u_D_D_POR_ASSERTIONS	100%	236 / 236 (100%)	n/a	n/a	n/a	n/a	n/a	n/a	100%	100%
u_HIBERNATE_SEQ_CHECK	100%	36 / 36 (100%)	n/a	n/a	n/a	n/a	n/a	n/a	100%	100%
u_POWERUP_SEQ_CHECK	100%	15 / 15 (100%)	n/a	n/a	n/a	n/a	n/a	n/a	100%	100%

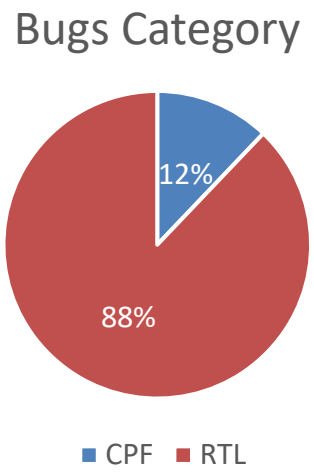
- 100% coverage on vplan and auto-generated vplan from CPF

Name	Overall	Goal	Overall	Planned Elements	Mapped Elements	Mapped Elements
pmu.vplan	100%	1	358 / 358 (100%)	112	112 / 112 (100%)	100%
Reference CPF Auto vplan	100%	1	538 / 538 (100%)	204	204 / 204 (100%)	100%

Results

- Verification closure by 3-4 month to tapeout
- Healthy silicon with zero bugs





Conclusion

- Proposed solution helped us in
  - Expose bugs early
  - Exhaustive verification of isolation (including analog to analog)
  - Exhaustive verification of Analog control sequencing.
  - Coverage closure without Cosims