Supply network connectivity: An imperative part in low power gate-level verification

Vinay Kumar Singh, Gabriel Chidolue
Mentor A Siemens Business

Divyeshkumar Dhanjibhai Vora
Arm

Abstract – Gate-level simulation is increasingly being used as part of the low-power verification process to verify low-power design behavior. It helps to boost confidence regarding the implementation of a design (typically represented in a gate-level netlist, with accompanying cell library made up of both Verilog cell views and Liberty views) and the power intent captured in UPF (IEEE 1801). Simulation corruption semantics applied when verifying such designs often depend on power related attributes defined in the Liberty views of the cells, such as related_power_pin, related_ground_pin, power_down_function or, in case of complex macro cells, the attributes could come from Verilog Power Aware models. These attributes are a function of the supply pin states of each of the cells, and as a result, ensuring that the power supply network is complete and accurate is fundamental to successful simulation of such netlists. While the UPF specification captures the abstract power distribution network, which defines how the supply nets and ports in the supply network get connected to single-rail cells (single-voltage standard cells)) and multi-rail cells (I/O cells, memory macros, and special power management cells for isolation, level shifting and retention), there are still gaps that may exist.

In this paper, we will give a conceptual overview of how gate-level netlist simulation is handled with a focus on illustrating the need for a proper supply network. And highlight the typical problems that can occur during simulation when supply connections are incomplete. We will also explain a methodology for automatic supply connections in the presence of incomplete or missing supply connections that is derived from the IEEE 1801 standard and leverages attributes contained within the Liberty views of gate-level cells, including different types of power management cells and macro cells that require multiple supply connections. We will discuss the corruption semantics consideration based on Liberty and Verilog Power Aware models. Using a real power management cell as a case study we will demonstrate results of applying the techniques. Our discussion will conclude with further work required in this area.

Glossary

IEEE1801 : Standard for specification of energy aware systems

UPF : Unified Power Format, a colloquial name for IEEE1801 standard

Liberty : An industry standard gate-level modeling format for timing, noise, power and test behavior

ELS cell : Combined Level shifter and isolation cell also known as enable level shifter

I INTRODUCTION

Low-power designs using power gating continue to be prevalent across the electronics industry, particularly in segments such as IoT, server and mobile. Gate-level low-power verification is required to uncover any power integrity issues early in the implementation process, rather than waiting until after place and route where the debug of such issues can be challenging.

At a higher abstraction, the power supply network and the simulated power-up and power-down behavior of RTL logic and UPF strategies are entirely specified in UPF, aside from any memory macro cells which

may need explicit connections in the UPF as well. However, as implementation tools transform these low-power designs into netlists, verification environments need to ensure that supply ports of cells are connected to the power supply network appropriately considering the type of cell, the power domain to which the cell belongs, the UPF strategy with which the cell is associated, or any explicit connection directives contained in the UPF. The various cell types include standard logic cells, single-rail and multi-rail special cells such as always-on buffers, isolation cells, level-shifter cells, combinatorial enabled level shifters, retention cells, special I/O cells and repeater cells. Typically, the supply network specification itself may still reside in the UPF specification.

UPF allows abstract policy definition to simplify the definitions of power strategy for complex low power design. For example, a design partitioned into four power domains PD1, PD2, PD3 and PD4 with signals crossing from PD1->PD2, PD1->PD3, and PD1 -> PD4 may have UPF either define explicit level-shifter policies for each domain crossing with input_supply and output_supply definitions, or define an abstract policy with respect to PD1 for all the signals crossing from PD1 to any other domain. Defining abstract UPF policies are much easier than explicit policies and are error-free because it allows the implementation tool to identify all the applicable domain crossings. In such cases, it is job of the tool to infer the correct supply network association with a given cell instance.

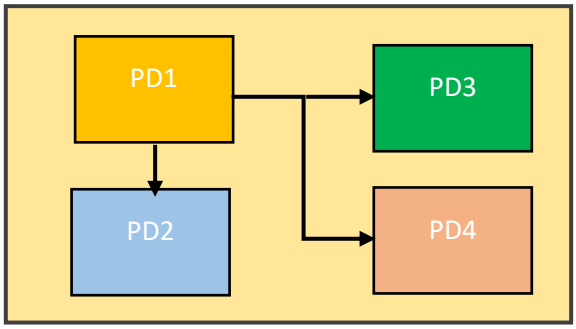

Figure 1: Example Power domain partition and signal crossing of a design

There are also cases for which UPF policies are not complete enough to provide all the required information by the verification tool. For example, policy specifies if a level-shifter should be inserted into the source or sink side domain, but it doesn't provide detail about whether the cell can sit in self, parent, sibling or other domain. Certain special cells such as always-on buffers and repeater cells may be inserted by implementation tools; however, these cells are not normally associated with any UPF strategy and therefore their supply connection will have to be explicitly added by the implementation tool, but it may not consistently reflect the changes it made to the design in UPF. The use of special combinatorial cells which combine the functionality of level-shifting and isolation requires special handling given that the level-shifter strategy may be missing the supply connection specification.

When adequate supply connections are not made, simulations fail prematurely. Designers have mitigated some of these issues by adding explicit connections in UPF, but this can be tedious to manage with large designs. At the other extreme, designers can force all unconnected supply ports to be always-on. This could mask real issues in the design that could have been addressed early if the appropriate supply connections had been made.

In section II we will explore the fundamental steps taken by gate-level simulation tools to prepare a complex low-power gate-level design for simulation highlighting the issues that can arise in the presence of incomplete supply connections. In section III we will propose a set of rules for automatic supply

connections that is derived from UPF and Liberty information. We will explore the impact of Liberty and Verilog cells on corruption semantics at the gate-level. Using a typical power management cell as a case study, we will show the results of applying our automatic supply connection rules in section IV and V and conclude with further work required in this area

II CONCEPTUAL UPF PROCESSING FOR GATE-LEVEL LOW POWER SIMULATION

Let us examine how typical simulation flows manage supply network connections. The typical gate level simulation process involves compilation of the netlist and Verilog cell libraries, design elaboration where UPF and Liberty are processed on the netlist to generate the extended design netlist that incorporates the implemented power architecture and then simulation of the extended design.

Typical gate level netlists will have some or all power management cells instantiated within the netlist with the supply network managed in UPF therefore the UPF processing step is largely concerned with identifying power management cells already in the netlist, matching them to appropriate power management policies i.e. power domains, UPF strategies and leveraging the supply information contained in the UPF policies to connect the appropriate supply ports of power management cells in the netlist to the UPF supply network.

A. Identification of cell types

Power management cells and Multi-voltage macro cells are identified using attributes contained in liberty views of the cells which are defined in a library. The liberty view also specifies the power pins, ground pins and any special data pins such as the isolation control port in an isolation cell or the enable port in an Enable Level Shifter (ELS) all of which aid in connection to the UPF managed supply network. All other single rail cells (standard cells) are partitioned based on the power domain they belong to and are connected implicitly to the primary supply of the power domain that they belong to. Liberty information pertaining to power is imported into a UPF based design as attributes with some Liberty attributes having corresponding UPF attributes [1].

B. Matching of cells to strategies and domains

Once power management cells have been identified, they are matched to UPF strategies and power domains based on different factors for example location of the cell in the netlist, control port connection, cell type, special pragmas specified in the netlist that match a cell to a strategy in UPF, option –instance of UPF strategy commands that indicates the instances in a netlist which implement the strategy or a combination of some of these factors. This step is necessary to ensure that the supply specified in the abstract UPF strategy is connected to the appropriate power management cell in the netlist. Furthermore, at this step the supply ports of the power management cells identified using the pg_pin and pg_type attributes are connected to the appropriate supplies specified in the UPF strategy they are matched with or through explicit `connect_supply_net` (CSN) UPF statements

This step is performed as part of the UPF processing at elaboration also. Any missing supply connection, UPF information or missing attribute that would facilitate supply connection would typically result in no supply connection being made or in other cases power is kept “always on” for that power management cell which in turn could result in unexpected simulation results. Since most designs today depend on Liberty (.lib information) to provide the attributes it is therefore necessary that design teams examine the UPF processing reports after design elaboration to ensure that all necessary attributes required for verification

are present. The authors recognize that verifying completeness of attributes and explicit supply connections in the UPF can be time-consuming, tedious and error prone at the gate-level because the verification engineers are not typically familiar with Liberty format, gate-level design netlists can be large and will typically have machine generated names differing from the original RTL.

Unfortunately, the UPF standard and its semantics for gate level design verification does not take full advantage of Liberty (.lib) attributes which could ease supply connections when UPF information is missing.

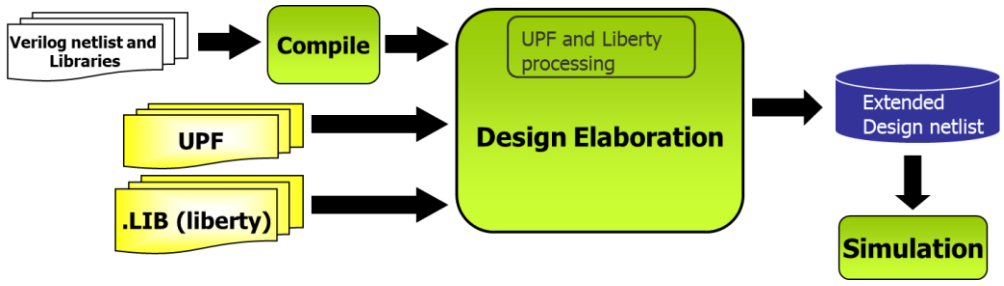

Figure 2: Typical simulation flow for gate level netlist of UPF based low power design

C. Supply connections expectations and challenges at the gate level

In a gate level netlist, implementation tools may choose to instantiate buffers as necessary to driven control signals of power management cells or to act as feedthrough buffers that will keep a signal alive even when it passes through a power domain that is shutdown. Such buffers do not have any UPF policies that they can be matched with and therefore need to be connected to appropriate supplies that would ensure that they operate correctly. The implementation tool that instantiates such a cell ideally should update the UPF with explicit `connect_supply_net` to maintain consistency. Verification tools may fail prematurely during simulation if this explicit supply connection is missing from the UPF policy. Debugging this issue can be daunting especially as designs get bigger, and due to the fact that implementation may flatten out hierarchy and other artefacts from RTL that provide context for debug.

Another challenge at the gate level is the inability for a verification tool to correctly match a power management cell to a UPF strategy. This can occur at different levels e.g an appropriate strategy is missing in the UPF or a strategy such as level shifter strategy is present however the supplies are not specified in the strategy.

Consider a gate level netlist with a cell identified as an isolation cell in it however the UPF is missing an appropriate isolation strategy. In the absence of any clear directives, a verification tool may choose to fail to make any supply connections for this cell which in turn will lead to premature failure during simulation, alternatively a verification tool may choose to keep the supply of this cell always-on which may mask a potential issue in silicon.

Complex power management cells that combine level shifting and isolation require that the cell be matched to appropriate UPF level-shifter and UPF isolation strategy. If the UPF level shifter strategy does not have the specification for input and output supplies, then the connections has to be managed by the tool. The UPF standard does have a very simple algorithm for supply connections for cells with 2 power supplies. When such cells have 3 power supplies or when such cells are optimized for placement at the sink side or source side, then more complete supply connection algorithm is required. Consider the UPF statements below.

```
create_supply_set VDDH
create_supply_set VDDL
create_supply_set VDDL_sw
create_power_domain PD1 –supply {primary VDDL_sw}
create_power_domain PD2 –supply {primary VDDH}

set_level_shifter uls –domain PD1 –applies_to outputs \
–rule low_to_high –location parent
set_isolation uiso –domain PD1 –applies_to outputs \
-isolation_supply_set VDDH –isolation_signal iso_en \
-isolation_sense low
```

Implementation tools can use the statements above to implement both isolation and level shifter strategy using 2 PG supply ELS cells, assuming the gate level library has such cells. The expectation is that the verification tools would connect the input supply of the ELS cell to the source power supply of the output ports of PD1 i.e. PD1.primary while the output supply of the ELS cell is connected to the sink power supply namely PD2.primary. The isolation strategy specifies the isolation supply which in this example matches the sink power supply. The input supply has to be identified by the tool through source sink analysis. Typically this type of cell is implemented such that the level shifting function is before the isolation function and this type of cell can be placed at the sink side. However tools cannot depend on the isolation supply always matching the sink power supply for supply connections purposes. The cell may be implemented such that isolation function is before the level shifting function which would imply that the specified isolation supply is some other supply (which is more relatively-on than the source but at the same voltage as the source domain) than sink domain. Of course such a cell has to be placed at the source side. The supply connection issues get compounded if the implementation chooses to use an ELS cell with 3 PG supplies

In the next section we will propose a set of rules for automatic supply connections in the absence of explicit connections in the UPF or missing supply connections in the UPF policies which takes advantage of Liberty attributes.

In section IV we will explore the simulation semantics for such connections and using waveforms we will present results of application of this proposal in section V. We will conclude with further work in this area in section VI.

III AUTOMATIC CONNECTIONS PROPOSAL

In a gate-level netlist, power management cells can be of different types based on their function such as level-shifter, isolation, retention, always_on buffers. Power management cells can have different flavors based on the number of supply pins they have.

A. TYPE OF CELLS

A1. Always-on cell

Generally these are simple combinational cells like buffer and inverter, etc that remain always powered irrespective of where they are placed. These cells remain powered on by a backup power supply in the region where they are placed even when the main power supply is switched off. The cells typically have a primary power pin and also a secondary backup power pin that supplies the current that is necessary when the main supply is not available. Liberty cell level attribute ‘always_on’ is required to identify a cells as

an always-on cell. The primary power of an always-on cell is usually connected to the supply of the power domain in which the cells is placed. The backup supply is expected to be always powered on.

A2. Retention cells

Retention cells are sequential cells that hold their state when the power supply is shut down and restore this state when the power is brought up again. The retention cell or register consists of a main register and a shadow register that has a different power supply. The backup power supply to the shadow register is always powered on to maintain the memory of the state. The primary supply is usually connected to the supply of the power domain in which the cell is placed.

A3. Level-shifter, Isolation and Enable-level-shifter cells

Level-shifters are special cells used for translating signals from one voltage domain to another. Such cells are inserted at a domain boundary to translate from a lower to a higher voltage range, and sometimes from a higher to a lower voltage range as well. The translation ensures the logic value sent by the driving logic in one domain is correctly received by the receiving logic in the other domain.

Isolation cells are also special cells which are used to isolate floating inputs from a powered-down domain to a powered-on domain. Such cells are typically used at the output of a powered-down domain to prevent floating (unpowered signals) from propagating to powered-on domains. They clamp the output node to a known value before the source domain is powered-off and keep it clamped until the source domain is fully powered-on.

Enable-level-shifter (ELS) cells are power management cells which implement the functionality of level-shifters and isolation in a single cell. Such cells are used at the interfaces where power switching is combined with multi-voltage operations.

One such type of cell is the single-rail level-shifter, and ELS cells which have only one supply. This cell have only one primary power pin and one primary ground pin defined in liberty and are usually powered with the supply of the power domain in which the cell is placed.

Then there are dual-rail Level-shifters, and ELS cells with 2 supplies. These cells have two power pins with one primary power pin having attribute ‘std_cell_main_rail : true’ in liberty. This attribute defines the power pin which is the main rail in the cell and is used to determine at which side of the power domain boundary the cell is placed. Such cells are usually placed in either the source or the sink power domain.

Dual-rail cells that combine Level-shifting and Isolation in the single cell can be categorized into two types. The first type has the isolation followed by the level-shifter (ISO-LS) and is more commonly referred to as a Combo cell. The second type has the level-shifter followed by isolation (LS-ISO) and is commonly referred to as an Enable Level Shifter (ELS) cell. Cells which have the main rail as the ‘related_power_pin’ of the enable pin and the output pin of the cell are usually LS-ISO and cells which have main rail as ‘related_power_pin’ of the enable pin and the input pin are usually ISO-LS type. The main rail of the cell is expected to be connected to the supply of the power domain in which the cell is placed. The secondary power pin of the cell is also dependent on the placement of the cell and if the cell is placed in the sink power domain then it is expected to be connected to the primary supply of the source power domain and vice-versa.

The third kind of cells are the ELS cells with 3 supply pins namely primary power pin, input power pin and output power pin. Attribute ‘std_cell_main_rail : true’ identify the primary power pin which is usually not

the ‘related_power_pin’ of any signal pin in the cell. The input power pin is the pin which is the ‘related_power_pin’ of the input data pin and the output power pin is the pin which is ‘related_power_pin’ of the output pin of the cell. The relation of the bias pin with the power pins determine the placement of these types of cells.

Table 1: Bias supply connections and impact on cell placement

#	Bias pin connectivity	3 PG-pin ELS cell placement
1	If bias pin is the ‘related_bias_pin’ of both primary power pin and the input power pin	Cell is placed in a parent/sibling of source side domain with voltage level same as source domain
2	If bias pin is the ‘related_bias_pin’ of both primary power pin and the output power pin	Cell is placed in a parent/sibling domain of sink side domain with voltage level same as the sink domain
3	If bias pin is the ‘related_bias_pin’ of only primary power pin	Cell can be place in any voltage domain which can be different then source and sink domain

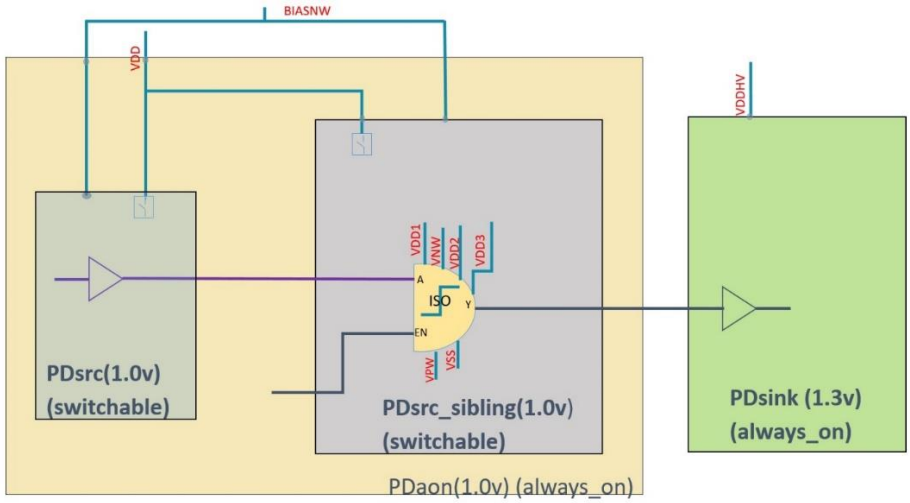

Figure 3 : Placement of 3 PG pin ELS cell

The above figure shows a 3 PG-pin ELS cell placed in a switchable source-side sibling domain (PDsrc_sibling) which is working at voltage level 1.0v. The output of the cell is received in an always_on sink domain (PDaon) working at 1.3v. The figure also shows the related power and related ground pins for input, output and enable pins of the cell.

The table below lists the pertinent Liberty attributes that help in automatic connections of power management cells

Table 2: Liberty attributes relevant for supply connections

<table>
<tr><th>#</th><th>Liberty Attribute</th><th>Description</th></tr>
<tr><td>1</td><td>pg_type</td><td>Specifies the type of power, ground and substrate-bias pin modeling. Some of the relevant values of <code>pg_type</code> attribute can be:
<table>
<tr><td>primary_power</td><td>Specifies that <code>pg_pin</code> is a primary power source</td></tr>
<tr><td>primary_ground</td><td>Specifies that <code>pg_pin</code> is a primary ground source</td></tr>
<tr><td>backup_power</td><td>Specifies that <code>pg_pin</code> is a backup (secondary) power source</td></tr>
<tr><td>backup_ground</td><td>Specifies that <code>pg_pin</code> is a backup (secondary) ground source</td></tr>
<tr><td>pwell</td><td>Specifies regular p-wells for substrate-bias modeling</td></tr>
<tr><td>nwell</td><td>Specifies regular n-wells for substrate-bias modeling</td></tr>
</table></td></tr>
<tr><td>2</td><td>physical_connection</td><td>This attribute defines type of connection – device_layer or routing_pin</td></tr>
<tr><td>2</td><td>related_power_pin</td><td>This attribute associate a predefined power pin with the signal pin, in which it is defined.</td></tr>
<tr><td>3</td><td>related_ground_pin</td><td>This attribute associate a predefined ground pin with the signal pin, in which it is defined.</td></tr>
<tr><td>4</td><td>related_bias_pin</td><td>Defines all bias pins associated with a power, ground or signal pin within a cell</td></tr>
<tr><td>5</td><td>std_cell_main_rail</td><td>This attribute is defined in a <code>primary_power</code> power pin. When the attribute is set to <code>true</code>, the <code>pg_pin</code> is used to determine which power pin is the main rail in the cell</td></tr>
<tr><td>6</td><td>is_isolation_cell</td><td>This attribute identifies a cell as an isolation cell</td></tr>
<tr><td>7</td><td>is_level_shifter</td><td>This simple attribute identifies a cell as a level shifter</td></tr>
<tr><td>8</td><td>always_on</td><td>This simple attribute identifies a cell as an always on cell</td></tr>
<tr><td>9</td><td>power_down_function</td><td>This simple attribute defines function when corresponding pin should be corrupted</td></tr>
<tr><td>10</td><td>retention_cell</td><td>This simple attribute define type of retention cell</td></tr>
</table>

IEEE1801 LRM provides guidance for power supply connectivity of Isolation, Retention and level-shifter cells, other power management cells such as always_on buffers are not typically covered by a strategy. So for such cells simulation tool would expect explicit `connect_supply_net` specification in UPF and if these explicit connection are missing in UPF then the onus of implicitly connecting these cells falls upon the tool.

B. Connection proposal for ELS and Combo cells with 3 supplies

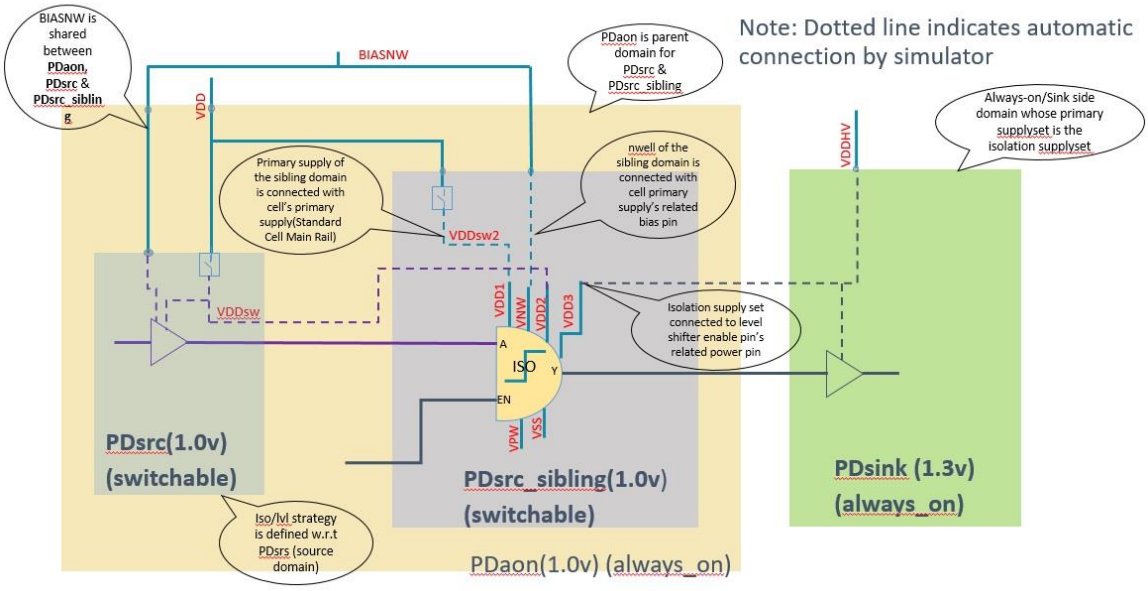

Figure 4: Automatic connection proposal result for ELS cell with 3 supplies

The figure above shows the tool created connection for the type-1 (bias pin is the related bias pin of both primary power and input pg-pin) 3 PG-pin ELS cell.

B1. Identifying 3 PG-pin ELS or Combo cells

In section II, we presented main components of UPF processing at gate level which includes power management cell identification and matching of identified cells to UPF strategies. A 3 PG-pin ELS or Combo cells can be identified in the design based on the following liberty attributes

1- is_level_shifter : true, and is_level_shifter_enable_pin : true
2- is_level_shifter : true and is_isolation_cell : true
3- related_power_pin attribute of level-shifter enable pin is -
    a. Same supply specified as related_power_pin of output pin for ELS cells.
    b. Same supply specified as related_power_pin of input pin for Combo cells

Tools should identify the input data pin by presence of either of the following attributes

1- level_shifter_data_pin
2- isolation_cell_data_pin

Input PG pin is to be identified as the 'related_power_pin' of the input data pin

Output PG pin is to be identified as the 'related_power_pin' of the logic output pin of the cell.

Tools should identify the internal PG pin by the presence of attribute 'std_cell_main_rail : true'

B1.1 Connection based on Level-shifter strategy supplies

When a cell is identified as a 3 PG-pin or 3 supply ELS or Combo cell and matched with the appropriate level-shifter strategy which has the supplies specified in the strategy, following connection rules should be followed

Table 3: Supply Connection rules for ELS or Combo cell with 3 supplies when supplies are specified in UPF strategy

#	PG Pin	Connected to
1	Input PG pin	input_supply of the level-shifter strategy
2	Output PG pin	output_supply of the level-shifter strategy
3	Internal PG pin	internal_supply of the level-shifter strategy
4	Bias PG pins	Input supply set's bias pins, if bias PG pin is 'related_bias_pin' of only input PG pin
		Output supply set's bias pins, if bias PG pin is 'related_bias_pin' of only output PG pin
		Internal supply set's bias-pins, if bias PG pins is 'related_bias_pin' of internal PG pin or shared between internal PG pin and source side PG pin or shared between internal PG pin and sink side PG pin.

B1.2 Connection when supply is not specified in Level-shifter strategy

When supply information is not specified in the level-shifter strategy then tool should do source/sink analysis and identify the following three supplies:

1- Primary supply of source power domain
2- Primary supply of sink power domain
3- Primary supply of the domain in which the cell is placed.

Tool should follow the following connection rules for combo cell:

Table 4: Supply connection rules for Combo cell (ISO followed by LS) with 3 supplies when supplies are not present in UPF strategy

#	PG Pin	Connected to
1	Input PG pin	isolation_supply_set specification of isolation strategy
2	Output PG pin	primary supply of sink power domain identified in source/sink analysis
3	Internal PG pin	primary supply of the power domain in which the cell is present
4	Bias PG pins	bias pins of source side supply's bias pins, if bias PG pin is 'related_bias_pin' of only input PG pin
		bias pins of sink side supply's bias pins, if bias PG pin is 'related_bias_pin' of only output PG pin
		Bias pins of primary supply of the domain in which the cell is placed, if bias PG pin is 'related_bias_pin' of internal PG pin or shared between internal PG pin and source side PG pin or shared between internal PG pin and sink side PG pin.

Tool should follow the following connection rules for ELS cells

Table 5: Supply connection rules for ELS cell (LS followed by ISO) with 3 supplies when supplies are not present in UPF

#	PG Pin	Connected to
1	Input PG pin	Primary supply of the source power domain identified in source/sink analysis
2	Output PG pin	Isolation_supply_set specification of isolation strategy which shall also match with primary supply of sink power domain identified in source/sink analysis.
3	Internal PG pin	primary supply of the power domain in which the cell is present
4	Bias PG pins	bias pins of source side supply's bias pins, if bias PG pin is 'related_bias_pin' of only input PG pin
		bias pins of sink side supply's bias pins, if bias PG pin is 'related_bias_pin' of only output PG pin
		bias pins of primary supply of the domain in which the cell is placed, if bias PG pin is 'related_bias_pin' of internal PG pin or shared between internal PG pin and source side PG pin or shared between internal PG pin and sink side PG pin.

Priority of connection should be in the following order

1- Explicit UPF connections specified using connect_supply_net
2- Connection based on the supplies specified in the matched Level-shifter strategy
3- If supply information is not specified in strategy then connection based on the tool-identified source/sink domain supplies
4- If cell is matched with only isolation strategy and not with a level-shifter strategy then tools shall follow the isolation cell connection rules.
5- If not strategy is matched, then all PG connections should be done with domain's primary in which cell is placed.

B2. Connection proposal for ELS cells with 2 supplies

B2.1 Identifying 2 PG-pin ELS cells

Similar to 3 PG pin ELS cells, 2 PG-pin ELS cells can be identified in the design based on the following liberty attributes

1- is_level_shifter : true, and is_level_shifter_enable_pin : true
2- is_level_shifter : true and is_isolation_cell : true

Tools should identifies the input data pin by presence of either of the following attributes

1- level_shifter_data_pin
2- isolation_cell_data_pin

Tools should identify the primary PG pin by the presence of attribute 'std_cell_main_rail : true' and the other PG pin can be identified as the secondary PG pin.

B2.2 Connection based on Level-shifter strategy supplies

Once a cell is identified as a 2 PG-pin ELS cell and matched with the appropriate level-shifter strategy which has the supplies specified in the strategy, following connection rules should be followed

Table 6: Supply connection rules for ELS cells with 2 supplies when supplies are specified in UPF

#	PG Pin	Connected to
1	Primary PG pin	Primary supply of the power domain in which the cell is placed
2	Secondary PG pin	input_supply, if primary PG pin is the 'related_power_pin' of enable and output pin
		output_supply, if primary PG pin is the 'related_power_pin' of input data pin
3	Primary ground and Bias pins	Appropriate functions of the supply connected to the primary PG pin

B2.3 Connection when supply set is missing in Level-shifter strategy

When supply information is not specified in the level-shifter strategy then tool should do source/sink analysis and identify the following three supplies:

1- Primary supply of the domain in which the cell is placed.
2- Primary supply of source power domain
3- Primary supply of sink power domain

Tool should follow the following connection rules:

Table 7: Supply connection rules for ELS cell with 2 supplies when supplies are missing in UPF

#	PG Pin	Connected to
1	Primary PG pin	Primary supply of the power domain in which the cell is placed
2	Secondary PG pin	Primary supply of the source power domain if primary PG pin is the 'related_power_pin' of enable and output pin of the cell. In this case, primary PG pin in #1 above shall match with isolation_supply_set specified in isolation strategy
		Primary supply of the sink domain if primary PG pin is the 'related_power_pin' of input data pin of the cell
3	Primary ground and Bias pins	Appropriate functions of the supply connected to the primary PG pin

Priority of connection for 2 PG-pin ELS cells should be same as the Priority order of 3 PG-pin ELS cells. Below table lists the type of Power management cell and the proposal for their automatic connection by simulation tools when explicit connections are not specified and when associated strategy does not have supply specification for other types of Power management cells

#	Cell type	UPF strategy matched	Power supply connection proposal
1	Retention cell	Strategy matched. -retention_supply specified in strategy.	Connect primary power pins to primary supply of power domain in which the cell is placed. Backup power pin to retention supply. Strategies with -use_retention_as_primary shall connect both primary and backup power to retention power.
2	Always ON	No Strategy	Connect primary power to the primary supply of the domain in which the cell is placed. Backup supply to tool generated always_on supply source.
3	Power management cell with 1 PG pin pair	No strategy matched	Connect primary supply to the primary supply of power domain where the cell is located
4	Isolation cell	Strategy Matched. -isolation_supply_set specified in strategy. -location specified either as self or parent/fanout	For -location self : Primary supply is connected to domain's primary and backup is connected to the isolation_supply_set i.e. Dual rail For –location parent/fanout : Primary supply is connected to domain that cell is located in i.e. Single rail
5	Retention and Isolation Cells with always_on attribute present in liberty	No strategies matched.	Primary supply pin is connected to power domain supply where cell is located backup supply pin is connected to tool generated always on power source
6	Power management cell with multiple PG pins	No strategies matched.	Primary supply and backup supplies are connected to power domain supply where cell is located
7	Level-shifter with 2 PG pin	Strategy Matched.	For -input supply and –output supply specified in strategy: Connect supply pin with std_cell_main_rail (scmr) attribute with primary supply of domain in which cell is placed. Connect other un-connected supply pin with input_supply of level shifter strategy if it is the related supply associated with level_shifter_data_pin pin or with output_supply of level shifter strategy if the supply is the related supply is associated with the output pin. For supplies not specified in strategy: If input_supply or output_supply of level shifter strategy is not specified then use source/sink

			analysis to identify supplies to use for connection of un-connected pins.
8	Level-shifter with 3 PG pin	Strategy Matched.	<u>For -input_supply and –output supply specified in strategy:</u> Connect Primary pin with scmr attribute with primary supply of domain in which cell is placed. Connect supply pin of level_shifter_data_pin with input_supply. Connect supply pin of output pin with output_supply. <u>For supplies not specified in strategy:</u> If input/output_supply not specified do source/sink analysis for connection.

Table 8: Supply Connection rules proposal

IV CORRUPTION SEMANTIC CONSIDERATIONS

Power domain corruption semantics is the mechanism employed by simulation tools to indicate when one or more power supplies sources that provide voltage to cells in the design have been turned off.

Simulation corruption semantics is based largely on UPF defined simstate (NORMAL, CORRUPT, etc) semantic during RTL based simulation. When a supply set is in a power state with simstate CORRUPT, then if that supply set is the primary supply of a power domain, then all logic elements within that power domain will be corrupted during that power state. Normal operation will resume for that domain once the power state of the primary supply set of the power domain transitions to a state whose simstate is defined as NORMAL. If the supply set is specified in an isolation or retention strategy, then the output of the Isolation or retention inferred by the tool is corrupted to indicate that power to this cell has been turned off. For the case of level shifting if the supply set is connected to the output supply set specification, then the output of the level shifter is corrupted to indicate that the output driver of the level shifter is turned off.

At the gate level, the netlist will typically contain standard cells and power management cells. These cells, provided by the library vendor (in Verilog), may be power aware or non-power aware. The cell will typically have a corresponding Liberty cell view that captures the PG pins of the cell and various power related attributes for the all pins of the cell such as those we described earlier in the previous section. In this section we will explore the impact of simulation corruption semantics of such gate level cells paying particular attention to power management cells.

A Power aware library cell description will include normal functionality of the cell and the power behavior of the cell - i.e. managing power up and power down (CORRUPTION) of the cell - in the Verilog model for that cell. The power behavior for such a cell is based on the state of input supply ports modelled in the Verilog description with the input ports being of single bit HDL types such as bit, wire, supply1, supply0

or internal wires of these types that serve as power supply inputs. The simulation semantic is managed by the model itself.

Power aware library cells are usually encountered in gate level netlists generated by Physical implementation tools where supply network is also present in the Verilog netlist. In similar netlists where the supply network is managed in UPF, there may be explicit `connect_supply_net` commands in UPF or automatic connections as described in the previous section can be applied to connect such a model. The simulation tool would also need to be aware of such a power aware model so that it does not apply UPF based corruption semantics since the model itself will manage its own corruption semantic.

Functional model of a Cell (Sample)

```
module ELSCELL (Y, A, EN);

 output Y;
 input A, EN;

 and u0(Y, A, EN);

endmodule
```

Power Aware model of a Cell (Sample)

```
module ELSCELL (Y, A, EN);
 output Y;
 input A, EN;
 supply1 VDDO, VDD, VNW;
 supply0 VSS, VPW;
 and u0(out_temp, A, EN);

 // Corrupt output when supplies are turned off
 assign Y = ((VDDO===1'b1)&&(VNW===1'b1)&&
 (VPW===1'b0)&&(VSS===1'b0)&&(!EN|VDD===1'b1))?
 out_temp : 1'bx;

endmodule
```

Figure 5: Non Power Aware (Functional) and Power Aware cell model sample in Verilog

A non-power aware library cell also referred to as functional model, typically contains only the functionality of the cell in the Verilog description. This type of cell does not have any supply ports in the Verilog description and is usually encountered in netlist generated by implementation tools before physical placement and routing such as post synthesis netlist. Usually the power supply network is managed largely in UPF rather than the netlist. The simulation semantics is managed by the simulation tool in this case. The tool may be instructed to use Liberty attributes such as "`power_down_function`" present for each output logic port to determine when to CORRUPT the particular output port, and for input ports "related`_power/ground`" attributes specified for each input port to determine when to CORRUPT the particular input. Let us refer to this semantic as liberty attribute based corruption.

Sample Liberty Model

```
cell(ELSCELL) {
 is_level_shifter : true ;
 level_shifter_type : HL_LH;

 pg_pin(VNW) {pg_type: nwell;
 pg_pin(VPW) {pg_type: pwell;
 pg_pin(VDDO) {pg_type: primary_power;
 pg_pin(VSS) {pg_type: primary_ground;
 pg_pin (VDD) {pg_type: primary_power;
                 std_cell_main_rail : true;
```

```
pin(A) { related_power/ground_pin : VDD/VSS;
        related_bias_pin : "VNW VPW";
        level_shifter_data_pin : true;

pin(EN) {related_power/ground_pin: VDDO/VSS;
    related_bias_pin: "VPW";
    level_shifter_enable_pin: true;

pin(Y){related_power/ground_pin: VDDO/VSS;
  related_bias_pin: "VPW";
  power_down_function:
"!VDDO+(!VDD&EN)+VSS+VPW+!VNW"
```

Figure 6: Sample Liberty Model contents

Regardless of whether the corruption semantic is managed by the cell library model itself in the case of a power aware cell or whether liberty attributes are leveraged by the verification tool when it manages the simulation semantic of functional cell library model, the supply network connections need to be handled correctly by the simulation tool since the corruption semantics of the cells depends heavily on states of the supply network as can be seen in the samples shown in figures 4 and 5 above.

V RESULTS PRESENTATION VIA CASE STUDY

To validate our supply connections proposal, we created a test netlist which had some 3PG Pin source side ELS cells with sparse UPF strategy information about how the supply for the cells were connected. The UPF used had strategies of the form shown below.

```
set_level_shifter ulshift -domain Plv \
-applies_to outputs -rule low_to_high -location parent

set_isolation   uiso -domain Plv\
 -isolation_supply_set VDDGSupply -applies_to outputs\
 -isolation_signal EN -isolation_sense low -location parent
```

We simulated this netlist without application of the connection proposal given in section III and got following results.
At elaboration time, tool gave warnings indicating that it had incomplete supply connection information

Instances :
1. /TEST/ u1_l3/i_any/i_cell
   Corruption mode : Liberty semantics corruption

Ports :

1. VDD
   Connection : /TEST/u1_l3/VDDGon , VCT : UPF2SV_LOGIC
2. VSS
   Connection : /TEST/u1_l3/VSSGon , VCT : UPF_GNDZERO2SV_LOGIC
3. BIASNW
   Connection : /TEST/u1_l3/BIASNWon , VCT : UPF2SV_LOGIC
4. VPW
   Connection : /TEST/u1_l3/VPWon , VCT : UPF_GNDZERO2SV_LOGIC
5. VDDI
   Connection : /TEST/u1_l3/VDDIsw , VCT : UPF2SV_LOGIC
6. VDDG
   Connection : /TEST/u1_l3/VDDsw , VCT : UPF2SV_LOGIC
7. VSSG
   Connection : /TEST/u1_l3/VSSsw , VCT : UPF_GNDZERO2SV_LOGIC

We proceeded to simulation and got the following results.

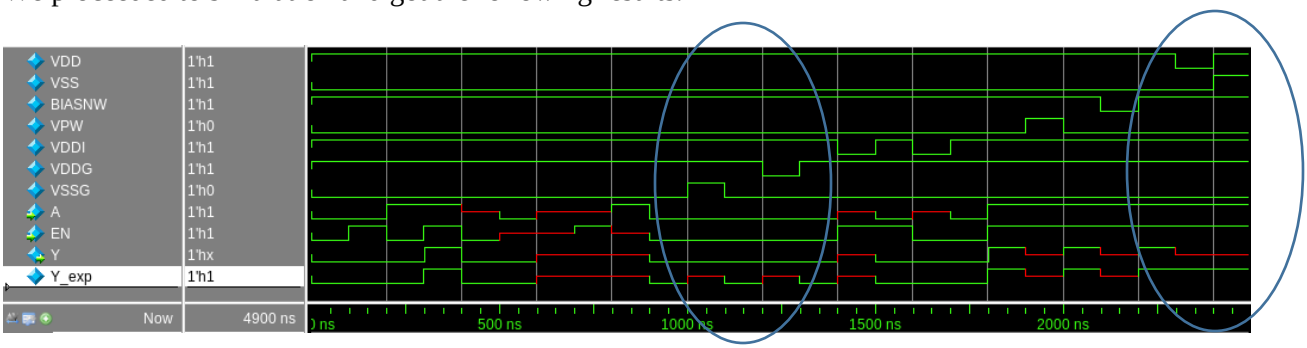

Figure 7: Waveforms before application of connection proposal

The waveforms showed effect of the assumptions that the particular verification tool we used had made. In this particular case, this tool did few wrong connections for ELS cell because it was not able to derive complete connectivity information from the sparse UPF policy and as a result you can see that from the waveforms that the output port Y of this cell was driven to unknown “X” when VDD and VSS are powered down resulting in false failures. Also, Y is expected to get corrupted when VDDG and VSSG are powered down which didn’t happen, resulting in false pass. The difference in expectations can be observed by looking at the waveforms for Y and Y_exp in figure 6 above.
In absence of clear / common semantic simulation tools may make other assumptions such as keeping all unconnected supplies always on. The problem with keeping unspecified supplies always on is that simulation results may not necessarily match with actual silicon behavior.

Next we simulated the same netlist enabling the supply connections proposal we have outline in section III and in the simulation results (logfiles and waveforms) we saw the following. The log file showed appropriate supply connections as indicated below

Instances :

1. /TEST/ u1_l3/i_any/i_cell

Corruption mode : Liberty semantics corruption

Ports :

1. VDD
   Connection : /TEST/u1_l3/VDDsw , VCT : UPF2SV_LOGIC
2. VSS
   Connection : /TEST/u1_l3/VSSsw , VCT : UPF_GNDZERO2SV_LOGIC
3. BIASNW
   Connection : /TEST/u1_l3/BIASNWon , VCT : UPF2SV_LOGIC
4. VPW
   Connection : /TEST/u1_l3/VPWon , VCT : UPF_GNDZERO2SV_LOGIC
5. VDDI
   Connection : /TEST/u1_l3/VDDIsw , VCT : UPF2SV_LOGIC
6. VDDG
   Connection : /TEST/u1_l3/VDDGon , VCT : UPF2SV_LOGIC
7. VSSG
   Connection : /TEST/u1_l3/VSSGon , VCT : UPF_GNDZERO2SV_LOGIC

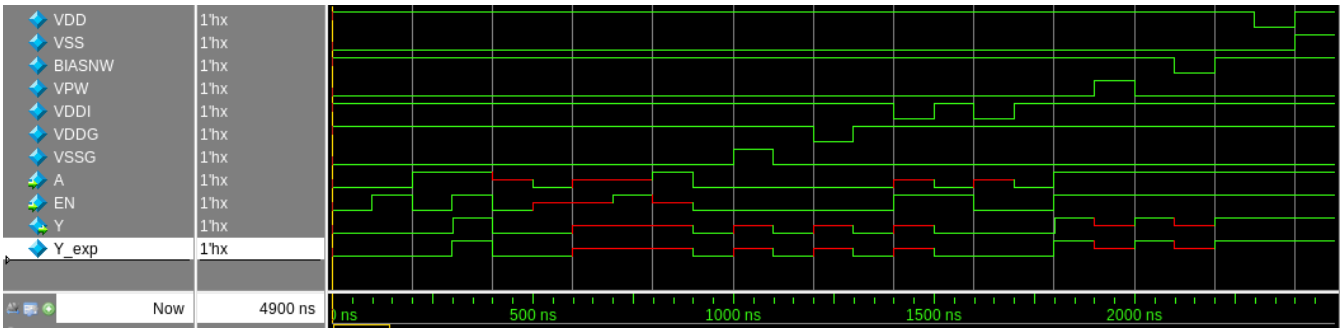

Figure 8: Waveform showing correct behavior with our connections proposal

- The output of our ELS cell was no longer “X” when VDD and VSS are powered down
- The output of our ELS cell was “X” when VDDG and VSSG are powered down
- The state of the supplies connected to the ELS cells correlated well with the behavior observed at the output port of the ELS.

This gives the confidence that simulation results will expose bugs such as incorrect supply switching transitions or incorrect supply connection due to wrong power management cell type being used in a netlist of a power managed design. In addition, the proposed supply rule connections will also help in catching issues such as wrong cell placement by synthesis tool and issues related to transient behavior like operation in forbidden/illegal power supply modes.

VI FUTURE WORK AND CONCLUDING REMARKS

In this paper we have highlighted some of the challenges that can be encountered while verifying UPF based gate level designs when the supply connectivity information is sparse. We have discussed the role of Liberty in gate level UPF based designs for supply connections and following from that we have proposed supply connection rules that when followed results in simulation results that closely matches real silicon behavior for power management cells. We have demonstrated how the connections proposal impacts the simulation semantics through the results presented in our case study.

We have shown that getting the power supply connectivity right is key in successfully verification of gate level representations of UPF based power managed design in order to avoid mismatches between simulation and implementation and to expose real supply connection issues in the design.

Our supply connection proposal leverages physical information contained in Liberty and addition analysis on UPF specified to derive any missing supply specification in UPF and may form the basis of proposals to the IEEE 1801 WG for further alignment between Liberty and UPF.

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