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Supply network connectivity: An imperative part in low power gate-level verification

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Introduction

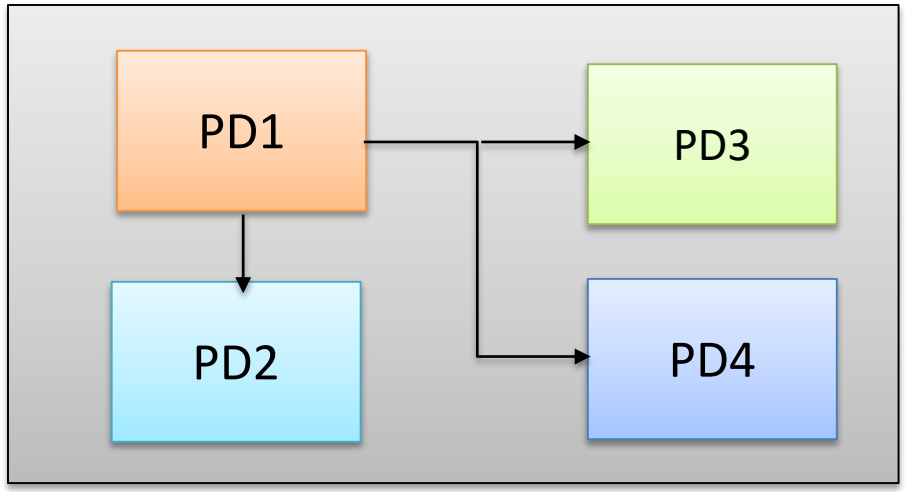
- Low power designs employing power gating is prevalent across electronics industry
  - Enabled by advances in UPF
- Verification of Low-power design at the gate level (GLS) is on the rise
  - Helps uncover any power integrity issues early
  - Helps raise confidence in the implementation
- Simulation semantics employed for such gate level designs depend on several factors
  - Liberty attributes of gate level cells : related_power/ground_pin, power_down_function etc
  - Supply network specified in UPF
  - Power supplies specified in UPF strategies

Power supply connections in GLS PA Sim

- At RTL power supply network, power up and power down behavior of RTL logic and UPF strategies are entirely specified in UPF
  - With exceptions such as memory macro cells which may need explicit connections in the UPF
- Implementation process transforms RTL + UPF to generate
  - GLS netlist with standard cells, macro cells and special power management cells
  - Each of these cells will have a Verilog model (.v) and a Liberty view(.lib)
- Verification environment needs to ensure that ports of these cells are connected appropriately to the power supply network depending on
  - Cell type
  - Explicit supply connection in UPF
  - UPF domain and/or UPF strategy specification
- Unexpected Simulation results may occur if supply connections are incomplete

Verification challenges

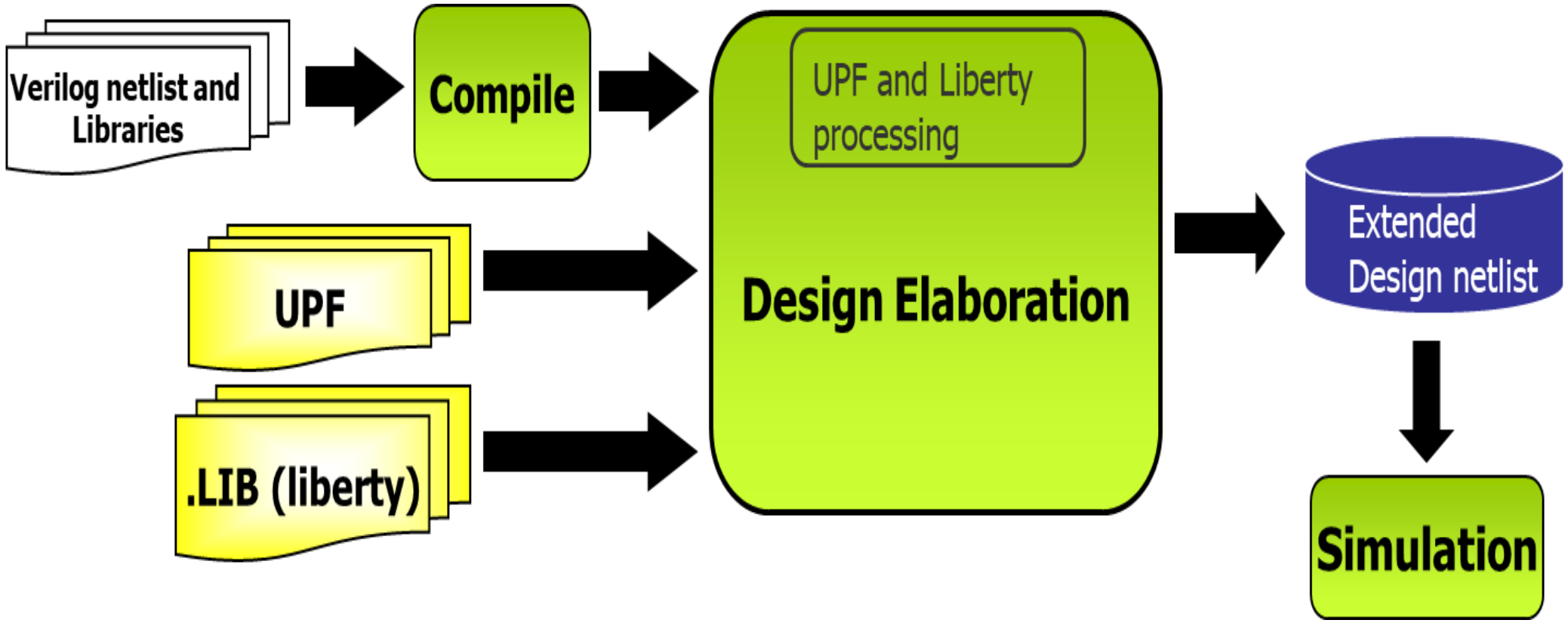
- So what are the sources of gaps?
- The abstract nature of UPF specifications
  - It may be more convenient to specify abstract supply connection policy in UPF with tool inferring the detailed connection for a given cell



Challenges continued

- UPF may be incomplete
  - E.g. UPF policy specify level shifter with some information such as input/output supply missing
  - Always-on buffers and repeater cells may be added by implementation tools with explicit supply connections missing from the UPF
- Designers mitigate some of these challenges by
  - Adding explicit connections in UPF : Tedious, time consuming and error prone in large gls designs
  - Force all unconnected supply ports to be always on : May mask real issues
- We propose a power supply connection solution in the presence of missing information
  - leveraging information in Liberty
  - And application of some design analysis to determine source domain and sink domain for any signal crossing through a power management cell

Typical Power aware GLS flow



Design Elaboration steps

- Typical gate level netlist
  - Some or all power management cells in the netlist
  - Supply network managed in UPF with some explicit connections
- UPF and Liberty are processed during Design elaboration
- Processing involves
  - Power management cell identification
  - Matching of cells to strategies and domain
  - Connections of appropriate supplies to ports of identified cells that match strategies/domains

Type of Power Management Cells

Logical

- Always-on cells
- Retention cells
- Level-shifter cells
- Isolation cells
- Isolation and Level-shifter cells
  - ELS - Level-shifter followed by isolation (LS-ISO)
  - Combo - Isolation followed by Level-shifter (ISO-LS)

Physical

- Placement domain
  - Source side
  - Sink side
  - Any
- Well Implementation
  - Shared N-Well
  - Isolated N-Well

Liberty Attributes for cell identification

Following are the pertinent Liberty attributes that help in cell identification and automatic supply connections of power management cells

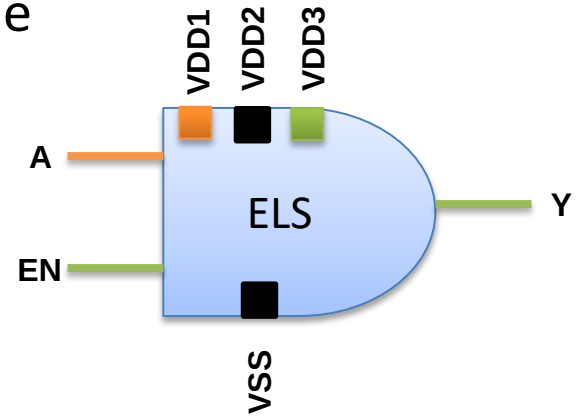
- pg_type
  - primary_power, primary_ground, backup_power, backup_ground, pwell, nwell
- related_power_pin
- related_ground_pin
- related_bias_pin
- std_cell_main_rail
- is_isolation_cell
- is_level_shifter
- always_on
- retention_cell
- power_down_function
- physical_connection
- level_shifter_data_pin
- isolation_cell_data_pin
- level_shifter_enable_pin
- isolation_cell_enable_pin

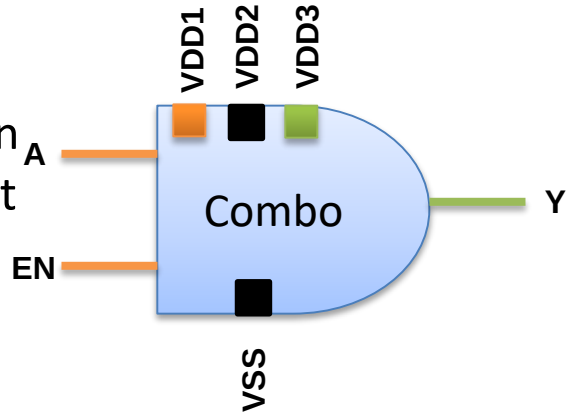
3 PG PIN ELS/Combo cell

- Motivations for focusing on 3 PG PIN ELS/Combo cell
  - Shared n-well 3 PG Pin ELS : Can be placed in third domain which can be either a parent domain of source/sink domain
  - Isolated n-well 3 PG Pin ELS : Can be placed in any unrelated domain
- Advantages over 2 PG PIN ELS
  - 3 PG Pin ELS cell is required for net driving AON logic within switchable domain
  - When there is no provision of placing ELS cell in either sink or source domain. Example in path between macro to macro.
  - It provides more flexibility for timing and routing resource optimization
- Typical Usage scenarios
  - With growing design complexity we see need for 3 PG pin ELS due to functional requirement increasing.

Case Study: Identifying 3 PG pin ELS/Combo

- 3 PG-pin ELS or Combo cells can be identified in the design based on the following liberty attributes
  - is_level_shifter : true, and is_level_shifter_enable_pin : true
  - is_level_shifter : true and is_isolation_cell : true
  - related_power_pin attribute of level-shifter enable pin is -
    - Same supply specified as related_power_pin of output pin for ELS cells.
    - Same supply specified as related_power_pin of input pin for Combo cells
  - Tools should identify the input data pin by presence of either of the following attributes
    - level_shifter_data_pin
    - isolation_cell_data_pin
  - Input PG pin is to be identified as the 'related_power_pin' of the input data pin
  - Output PG pin is to be identified as the 'related_power_pin' of the logic output pin of the cell.
  - Tools should identify the internal PG pin by the presence of attribute 'std_cell_main_rail : true'





Power supply connection proposal

- When Level-shifter strategy has supplies specified for 3 PG PIN ELS, then
  - Input_supply, output_supply and internal_supply specified in strategy are used directly
  - See paper for details

- 3 PG pin ELS cell connection when supply is not specified in Level-shifter strategy
  - When supply information is not specified in the level-shifter strategy then tool should do source/sink analysis and identify the following three supplies:
    - Primary supply of source power domain
    - Primary supply of sink power domain
    - Primary supply of the domain in which the cell is placed

Power supply connection proposal

- Simulation tool should follow the following connection rules for combo cell:

#	PG Pin	Connected to
1	Input PG pin	isolation_supply_set specification of isolation strategy
2	Output PG pin	primary supply of sink power domain identified in source/sink analysis
3	Internal PG pin	primary supply of the power domain in which the cell is present
4	Bias PG pins	bias pins of source side supply's bias pins, if bias PG pin is ‘related_bias_pin’ of only input PG pin
		bias pins of sink side supply's bias pins, if bias PG pin is ‘related_bias_pin’ of only output PG pin
		Bias pins of primary supply of the domain in which the cell is placed, if bias PG pin is ‘related_bias_pin’ of internal PG pin or shared between internal PG pin and source side PG pin or shared between internal PG pin and sink side PG pin.

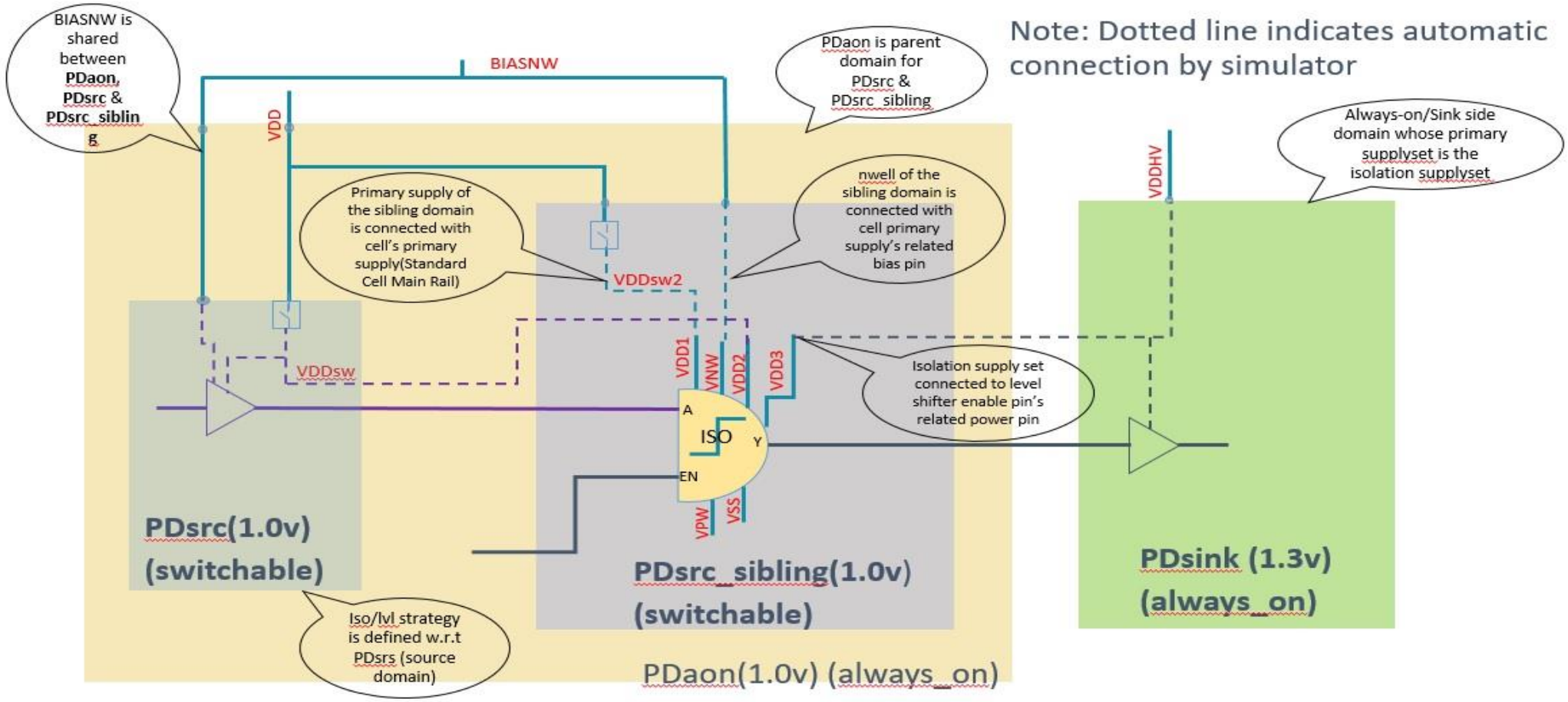
Power supply connection proposal

- Simulation tool should follow the following connection rules for ELS cell:

#	PG Pin	Connected to
1	Input PG pin	Primary supply of the source power domain identified in source/sink analysis
2	Output PG pin	Isolation_supply_set specification of isolation strategy which shall also match with primary supply of sink power domain identified in source/sink analysis.
3	Internal PG pin	primary supply of the power domain in which the cell is present
4	Bias PG pins	bias pins of source side supply's bias pins, if bias PG pin is ‘related_bias_pin’ of only input PG pin
		bias pins of sink side supply's bias pins, if bias PG pin is ‘related_bias_pin’ of only output PG pin
		bias pins of primary supply of the domain in which the cell is placed, if bias PG pin is ‘related_bias_pin’ of internal PG pin or shared between internal PG pin and source side PG pin or shared between internal PG pin and sink side PG pin.

Power supply connection proposal

- Tool created connection for the type-1 (bias pin is the related bias pin of both primary power and input pg-pin) 3 PG-pin ELS cell:



Case study : 2 PG Pin ELS/Combo

- 2 PG Pin ELS / Combo is identified as follows
  - Using attributes is_level_shifter:true, is_isolation_ cell:true, is_level_shifter_enable_pin : true
  - related_power_pin attribute of level-shifter enable pin is -
    - Same supply specified as related_power_pin of output pin for ELS cells.
    - Same supply specified as related_power_pin of input pin for Combo cells
  - Tools should identify the input data pin by presence of either of the following attributes
    - level_shifter_data_pin
    - isolation_cell_data_pin
  - Input PG pin is to be identified as the ‘related_power_pin’ of the input data pin
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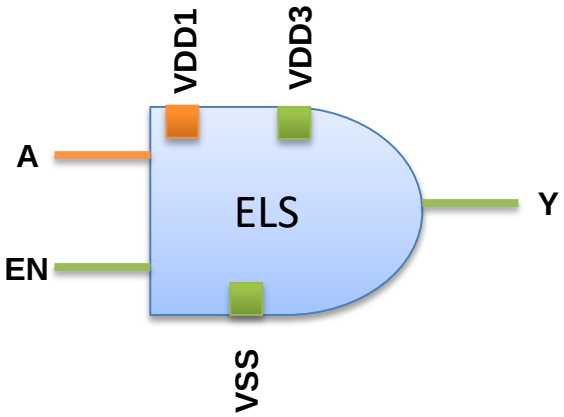
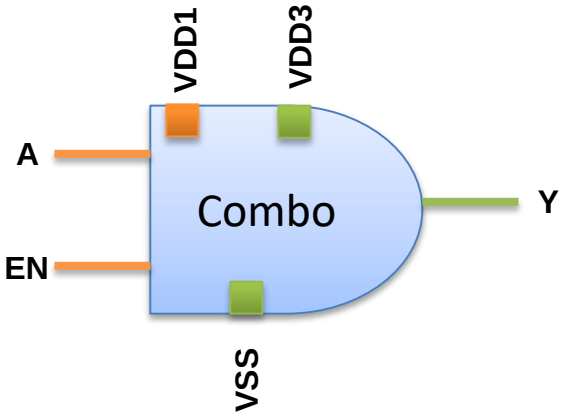




Power supply connection proposal : 2 PG pin ELS/Combo

- Connect supply pin with std_cell_main_rail (scmr) attribute to primary supply of domain in which cell is placed.
- Connect 2nd PG pin as follows
  - For source side ELS connect to primary supply of sink domain and for sink side ELS connect to primary supply of source domain
  - For sink side Combo cells connect to isolation supply specified in isolation strategy. 2-PG pin source side Combo cell not possible.
  - When supply specification are missing from the level shifter strategy use Source / sink analysis to identify the supply to use for 2nd PG pin
- Priority of connection remains same as in the 3 PG pin case

Power supply connection proposal

- Priority of connection should be in the following order
  - Explicit UPF connections specified using connect_supply_net
  - Connection based on the supplies specified in the matched Level-shifter strategy
  - If supply information is not specified in strategy then connection based on the tool-identified source/sink domain supplies
  - If cell is matched with only isolation strategy and not with a level-shifter strategy then tools shall follow the isolation cell connection rules.
  - If no strategy is matched, then all pg connections should be done with domain's primary in which cell is placed
- Paper has details of full proposal for connecting supplies of all different power management cell types

Corruption Semantics

Liberty Based

- PG pin information within liberty used for PG connections
- Low power attribute within liberty used for inferring power aware behaviour
- Verilog includes normal functionality only
- Simulation semantics is managed by the simulation tool in this case

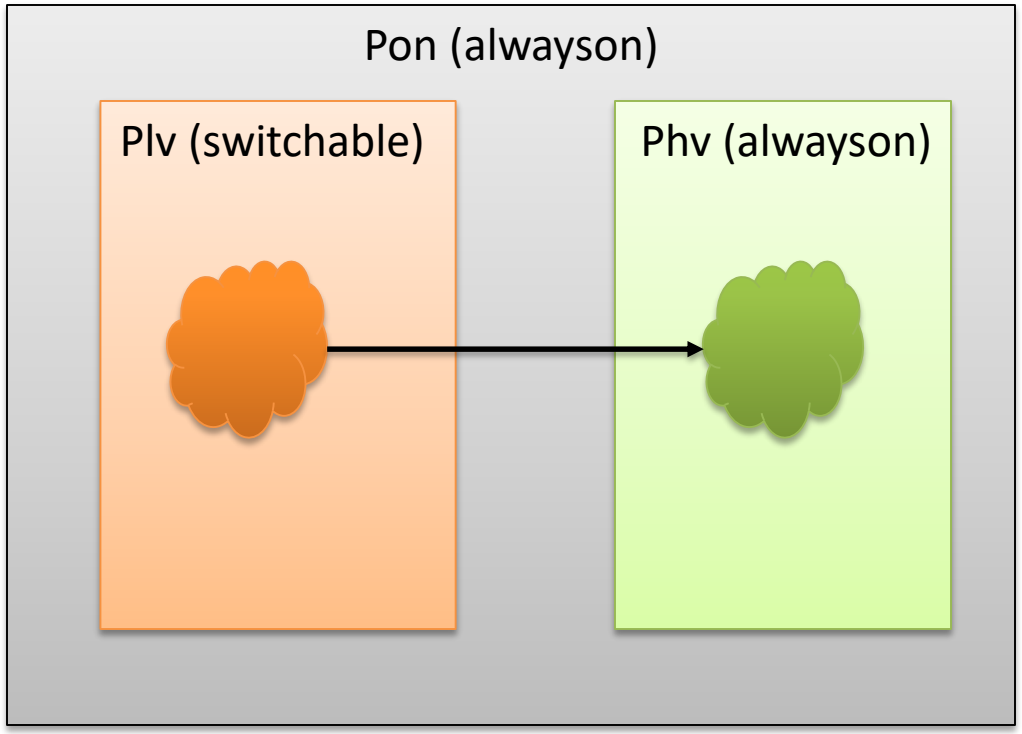
Verilog Based

- PG pin information within liberty used for PG connections
- Verilog includes normal functionality of the cell and the power behavior modeled using supply1/supply0.
- The simulation semantic is managed by the model itself in this case

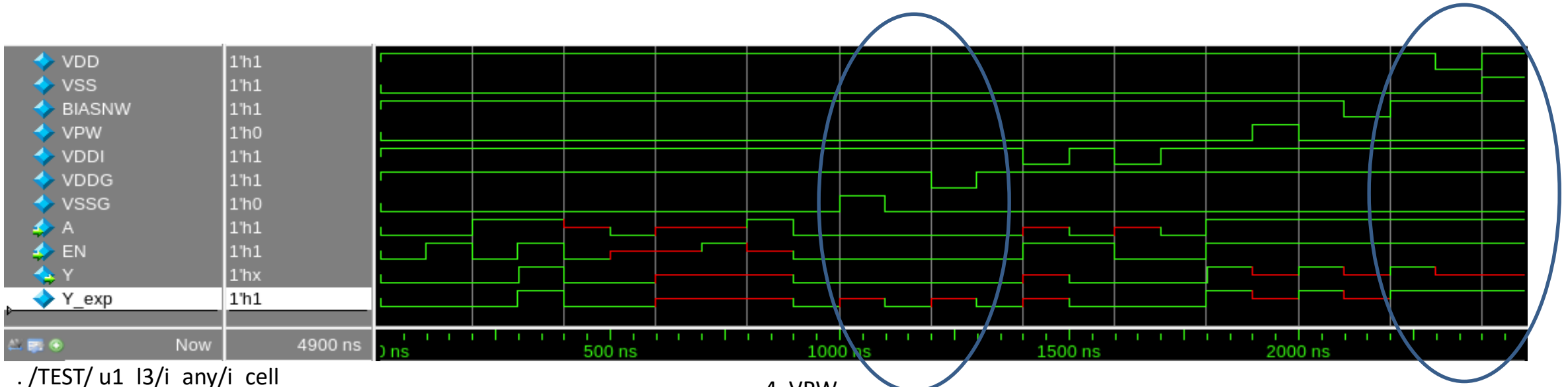
Case Study: ELS cell

- set_level_shifter ulshift \
  -domain Plv \
  -applies_to outputs \
  -rule low_to_high \
  -location parent

- set_isolation uiso \
  -domain Plv \
  -isolation_supply_set VDDGSupply\
  -applies_to outputs \
  -isolation_signal EN \
  -isolation_sense low \
  -location parent



Simulation Results: Wrong Connections



. /TEST/ u1_l3/i_any/i_cell

Corruption mode : Liberty semantics corruption

Ports :

1. VDD

   Connection : /TEST/u1_l3/**VDDGon** , VCT : UPF2SV_LOGIC

2. VSS

   Connection : /TEST/u1_l3/**VSSGon** , VCT : UPF_GNDZERO2SV_LOGIC

3. BIASNW

   Connection : /TEST/u1_l3/BIASNWon , VCT : UPF2SV_LOGIC

4. VPW

   Connection : /TEST/u1_l3/VPWon , VCT : UPF_GNDZERO2SV_LOGIC

5. VDDI

   Connection : /TEST/u1_l3/VDDIsw , VCT : UPF2SV_LOGIC

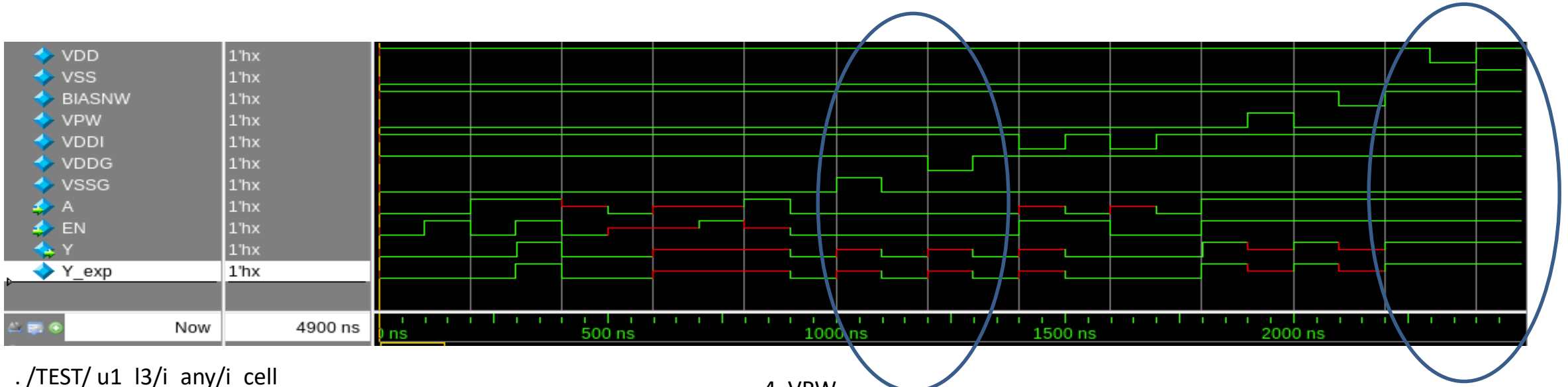
6. VDDG

   Connection : /TEST/u1_l3/**VDDsw** , VCT : UPF2SV_LOGIC

7. VSSG

   Connection : /TEST/u1_l3/**VSSsw** , VCT : UPF_GNDZERO2SV_LOGIC

Simulation Results: Wrong Connections



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Conclusion and future work

- Gate level low power simulation is on the rise
- Proper supply connections are critical for accurate gate level simulations
- The automatic supply connections proposal leverages existing information from Liberty and UPF
- UPF standard may want to formalize and align with the additional Liberty attributes leveraged by this paper.