Properly Introducing Python To Your UVM Testbench

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Abstract

There are many attractive aspects of using Python in a simulation testbench, including a large ecosystem of libraries and tools. Among the obstacles are the integration effort and limitations in the ability to reuse existing UVM content. This paper presents a UVM-centric integration approach, implemented by an open source library, that practically eliminates per-testbench integration work while preserving the ability to reuse existing UVM assets in a highly-performant manner. Examples highlight key usecases enabled by such an integration approach.

I. Introduction

Much of the testbench code we write is effectively object-oriented software. Scoreboards, random stimulus generators, and test sequences all heavily leverage software techniques. According to the 2024 Siemens and Wilson Research Group verification trend report [1], these software-centric activities comprise at least 36% of verification activities. It's natural to speculate whether using a pure-software language for these aspects would increase productivity. After all, popular languages, by definition, have larger communities of proficient engineers, and larger ecosystems of tools and supporting libraries.

AI-friendliness – how proficient large language models (LLMs) are with a language – is also a relevant concern, given the proliferation of AI coding assistants. Here, again, LLMs tend to excel with popular languages.

Python has been a highly-popular language for many years, holding the top spot in the TIOBE rankings for the last five years [2]. Despite all these seeming advantages, Python has a relatively modest 5% market share in the verification space according to the Wilson survey.

II. Integration Approaches and Trade-Offs

There are two current approaches to integrating Python into a simulation testbench, each of which have benefits and drawbacks.

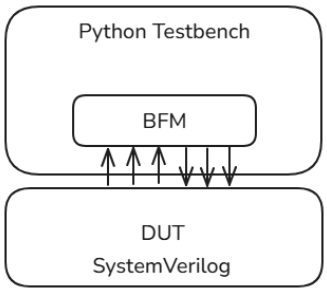

Figure 1: cocotb Signal-Level Interface.

cocotb [3], first released in 2013, integrates via the simulator's signal-level API (VPI and VHPI) and interacts with the design at the signal level. This makes integration with a design dynamic and simple. However, reuse of existing SystemVerilog UVM components is difficult at best due to the difference in abstraction levels: UVM components are activated via task and function calls, while cocotb can only interact with signals in the design. Consequently, cocotb testbench environments tend to be pure Python, aside from the design in Verilog or VHDL. This presents a significant obstacle to adoption in existing UVM testbench environments, where many thousands of hours have been invested in building UVM infrastructure for interacting with standard protocols.

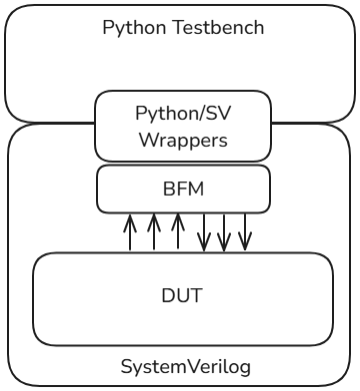

Figure 2: Wrapper-Based Task/Function Interface.

Wrapper-based integrations between Python and SystemVerilog use interface code, typically generated, to implement cross-calling between the two languages using a simulator extension API such as the direct programming interface (DPI). These integrations offer improved reuse of existing testbench components because they allow Python and SystemVerilog to interact at same task and function abstraction level as the verification components are typically implemented. However, the effort of designing, implementing, and maintaining the integration infrastructure can be significant. This slows adoption of Python in existing testbench environments because time must be taken to properly wrap and expose the API of each distinct testbench component to Python.

There are other Python-based libraries focused on design and verification, but these address different problems than connecting Python verification content to existing testbench environments. For example, Pymtl3 [6] focuses on capturing self-contained design and verification collateral, and lacks features for connecting Python to existing SystemVerilog testbench environments. pysv [7] focuses on creating C wrappers for Python methods that allow SystemVerilog to invoke the wrapped Python methods via DPI, but does not provide support for Python calling SystemVerilog tasks.

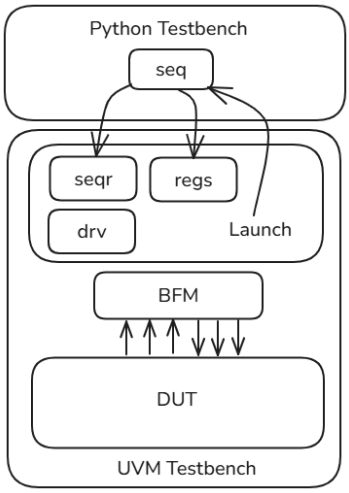

Figure 3: PyHDL UVM Interface.

The ideal Python integration with SystemVerilog is one that incorporates the benefits of the two approaches above. In short requires little integration effort while enabling reuse of existing UVM verification components with Python at the task and function call level. Fortunately, the UVM API provides all the necessary capabilities to enable this integration.

The PyHDL-IF[4] Python library implements a general purpose task and function based interface between SystemVerilog and Python. This library can be used by a SystemVerilog environment to call arbitrary Python libraries, and implements a wrapper-based mechanism to support Python calls to SystemVerilog tasks and functions. PyHDL-IF also provides a UVM-specific library that is the topic of this paper. The UVM-specific portion of the library provides three key areas of functionality:

- Support for running Python-implemented behavior from a SystemVerilog/UVM environment
- Pre-defined classes for interacting with UVM APIs and user-defined UVM types in SystemVerilog
- Support for generating a Python projection of user-defined UVM types to support Python development tools

III. Running Python behavior from UVM

UVM provides two key mechanisms for initiating behavior: components and sequences. Both can be leveraged as a way to initiate behavior implemented in Python as well as behavior implemented in SystemVerilog.

The PyHDL-IF library provides a family of SystemVerilog *proxy* objects that are constructed in the SystemVerilog portion of a UVM environment and hold a reference to a Python object. The SystemVerilog proxy manages invoking key methods on the Python implementation when the UVM library invokes the corresponding methods of the SystemVerilog proxy.

A simple sequence-based example is shown in *Listing 1*. The behavior of a UVM sequence is implemented in its *body* method. UVM ensures that this method is invoked as part of the process of running the sequence.

```
class base_test extends uvm_test;
    // ...
    task run_phase(uvm_phase phase);
        // Python-driven sequence proxy
        typedef pyhdl_uvm_sequence_proxy #(
            .REQ(seq_item)) seq_t;
        seq_t seq;

        phase.raise_objection(this);
        seq = seq_t::type_id::create("seq");
        seq.pyclass = "pyseq::PyRandSeq";
        seq.start(m_env.m_seqr);
        phase.drop_objection(this);
    endtask
endclass
```

Listing 1: Starting a Python-implemented Sequence.

The *pyhdl_uvm_sequence_proxy* class is used to implement a sequence in Python by linking a Python class instance to a UVM sequence instance.

The *pyhdl_uvm_sequence_proxy* class inherits from *uvm_sequence*, can run on any sequencer, and can be parameterized with the appropriate sequence-item type when running on a sequencer that drives sequence items. See *Listing 9* for a definition of the *seq_item* type.

The proxy class has a string-type field that specifies the name of the Python class that will implement the sequence. While this example specifies a hard-coded Python classname, dynamic mechanisms for determining the sequence to run, such as plus-args, can be used as well.

```
class PyRandSeq(uvm_sequence_impl):

    async def body(self):
        for i in range(8):
            req = self.proxy.create_req()

            await self.proxy.start_item(req)
            req.randomize()
            await self.proxy.finish_item(req)
```

Listing 2: Python Sequence Implementation.

The Python implementation of the sequence is a class that inherits from the *uvm_sequence_impl* class declared by the PyHDL-IF library. The sequence implementation overrides the *body* method, and could override other UVM-defined methods as well. The sequence implementation accesses the UVM sequence proxy via the *proxy* handle. The proxy

provides standard sequence APIs defined by UVM, as well as some special services. For example, the proxy provides *create_req* and *create_rsp* functions that construct a request and response sequence item of the proper type.

The PyHDL-IF library provides proxy classes for UVM sequences and UVM components, enabling Python to be easily integrated with very little change to the existing environment.

IV. Interacting with UVM APIs

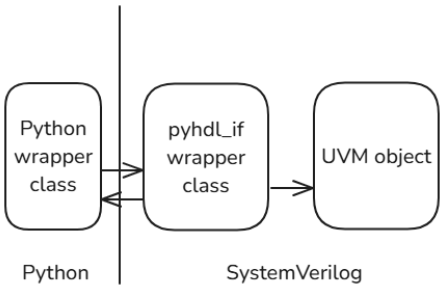

Figure 4: PyHDL-IF Wrapper Structure.

The PyHDL-IF library provides a set of wrappers for UVM classes. Figure 4 illustrates the wrapper scheme that the library uses to access objects in a UVM testbench. Each *uvm_object*-based object that the Python environment is currently accessing has a pair of accessor classes. In the SystemVerilog environment, a wrapper class holds a reference to the UVM object and implements accessor methods that convert Python method calls into SystemVerilog method calls. When a method returns a *uvm_object*-based reference, the wrapper class constructs a new Python/SV pair of wrapper objects and returns the Python object.

UVM-defined APIs are exposed mostly as is, unless significantly at odds with what is natural in Python.

```
function bit get_config_object (
    string field_name,
    inout uvm_object value,
    input bit clone=1);
```

Listing 3: UVM get_config_object Signature.

One example of this change category are the UVM config-db methods in the *uvm_component* class. SystemVerilog uses *inout* parameters to return more than one data element. It's common in Python to return a *tuple* in cases like this.

```
def get_config_object(self,
  name : str,
  clone : bool=True) -> Tuple[bool, UvmObject]:
```

Listing 4: Python get_config_object Signature.

Consequently, the Python implementation of get_config_object returns a tuple with the status (whether the named config entry exists) and the value of the config entry.

```
function void my_c::build_phase(uvm_phase phase);
  uvm_object obj;
  bit has;

  // ...

  has = comp.get_config_object("cfg", obj);

endfunction
```

Listing 5: Calling get_config_object in SystemVerilog.

```
def build_phase(self, phase):
  has, obj = comp.get_config_object("cfg")
```

Listing 6: Calling get_config_object in Python.

This difference in API signature slightly changes how a test written in Python interacts with this API compared to how SystemVerilog does. The difference is minor, and aligns the API With Python best practices. In *Listing 6*, note how Python unpacks the two-variable return of *get_config_object* into the individual variables *has* and *obj*.

The PyHDL-IF library also provides convenience APIs to make the UVM testbench structure more easily-accessible. One example of such a convenience API exposes registers in a register block as Python class fields. In this and similar cases, named objects are registered with the UVM library. These objects could be located by searching through the objects registered with UVM, but exposing them as Python class fields simplifies the Python code.

```
  class spi_reg_block extends uvm_reg_block;
    `uvm_object_utils(spi_reg_block)

    rand reg_CTRL   CTRL;
    rand reg_STATUS STATUS;
    rand reg_CLKDIV CLKDIV;
    rand reg_SS     SS;
    rand reg_TXDATA TXDATA;
    rand reg_RXDATA RXDATA;

    // ...
    virtual function void build();
      CTRL =
        reg_CTRL::type_id::create("CTRL");
      STATUS =
        reg_STATUS::type_id::create("STATUS");
      CLKDIV =
        reg_CLKDIV::type_id::create("CLKDIV");
      SS     =
        reg_SS::type_id::create("SS");
      TXDATA =
        reg_TXDATA::type_id::create("TXDATA");
      RXDATA =
        reg_RXDATA::type_id::create("RXDATA");

      // ...
      CTRL  .configure(this, null, "");
      STATUS.configure(this, null, "");
      CLKDIV.configure(this, null, "");
      SS    .configure(this, null, "");
      TXDATA.configure(this, null, "");
      RXDATA.configure(this, null, "");
    endfunction

  endclass
```

Listing 7: UVM Register Block.

The SystemVerilog UVM example in *Listing 7* creates several fields in a register block. Note that the objects are given a name, and that they are registered with the register block via the *configure* function. UVM provides functions to iterate over the registers in a block and access them by name. User-created testbench code can also access them directly as SystemVerilog class fields.

```
class PyRegSeq(uvm_sequence_impl):
```

```
  async def body(self):
      seqr = self.proxy.m_sequencer
      spi_regs : uvm_reg_block
      _,spi_regs = seqr.get_config_object(
          "spi_regs")

      spi_regs.CTRL.enable.set(1)
      spi_regs.CTRL.master.set(1)
      await spi_regs.CTRL.update()

      await spi_regs.CLKDIV.div.write(0x4)
      await spi_regs.SS.ss_mask.write(0x1)

      await spi_regs.TXDATA.write(0xA5)

      # Wait for
      for _ in range(100):
          await spi_regs.STATUS.read()

          if spi_regs.STATUS.tx_empty.get():
              break
```

Listing 8: Python Register-Programming Sequence.

As shown in *Listing 8*, PyHDL-IF provides convenience methods in Python that expose named UVM child objects as Python class fields, allowing Python code to interact with registers and register fields using the same pattern that would be used in SystemVerilog.

V. Introspecting User-Defined Types

UVM objects that are named, and are registered with a container type, such as a *component* or *reg_block* can be accessed from Python using existing UVM access APIs. Fields that are not registered in this way pose a different challenge.

```
class seq_item extends uvm_sequence_item;
  rand bit [7:0]   addr;
  rand bit         write; // 1=write, 0=read
  rand bit [31:0]  data;
  rand bit [3:0]   tid;

  // Simple constraints
  constraint addr_c {
    addr inside {[8'h00:8'hFF]};
  }

  constraint data_c {
    if (write) data != 32'h0;
  }

  `uvm_object_utils_begin(seq_item)
    `uvm_field_int(addr , UVM_ALL_ON)
    `uvm_field_int(write, UVM_ALL_ON)
    `uvm_field_int(data , UVM_ALL_ON)
    `uvm_field_int(tid  , UVM_ALL_ON)
  `uvm_object_utils_end

  function new(string name = "seq_item");
```

```
    super.new(name);
  endfunction
endclass
```

Listing 9: UVM Sequence Item.

The *seq_item* class in *Listing 9* declares several random fields. These fields are named in SystemVerilog, but they are not registered with the UVM library as named UVM objects. Classes similar to this are used extensively in UVM testbench environments to capture transactions observed by monitors, and to control initiator bus functional models (BFMs). Consequently, having the ability to read and write field values in these transaction-like classes is critical.

Two things must be possible to enable accessing these field values:

- It must be possible to obtain the names and types of the fields
- It must be possible to read and write the values of the fields

Fortunately, UVM provides both capabilities directly or indirectly. Both are enabled by the *uvm_field* macros shown in *Listing 9*.

Displaying transactions, along with their field names and values, is very helpful from a debug perspective. Consequently, UVM provides several APIs (e.g. print, sprint) to produce a textual representation of a transaction. The class creator can provide the core implementation of this functionality as SystemVerilog code, but the *uvm_field* macros provide automation and a much more concise and declarative method for doing so.

```
-----------------------------------
Name      Type      Size  Value
-----------------------------------
seq_item  seq_item  -     @550
  addr    integral  8     'h43
  write   integral  1     'h0
  data    integral  32    'ha8136875
  tid     integral  4     'hc
-----------------------------------
```

Listing 10: UVM Object Print Example Output.

The built-in UVM formatting produces the output above when the *print* method is called on the *seq_item* class. This information provides everything required to obtain the name, type, and size of fields in the object. While it would be possible to read the value of class fields by parsing this output, the performance would be low due to the amount of required string parsing.

UVM provides the *pack* and *unpack* APIs to get and set class fields. The *pack* API converts the values of registered class fields into an array of integers, while the *unpack* API does the reverse. The packed data does not preserve any meta-data about the layout of class from which it was produced. Consequently, the consumer of packed data must know the layout of the class in order to properly interpret the data.

Together, these two UVM-provided capabilities enable the PyHDL-IF library to get and set the value of fields in user-defined classes that inherit from UVM classes.

The PyHDL-IF library analyzes the transaction text output once for each unique UVM class type to create type information that is used to access class fields. *pack* and *unpack* methods implemented by the library return and accept Python classes whose layout mirrors the field layout.

A. Getting Field Values

```
class PyRandSeq(uvm_sequence_impl):

    async def body(self):
        # Send a small burst of randomized items
        for i in range(8):
            req = self.proxy.create_req()
```

```
            await self.proxy.start_item(req)

            req.randomize()

            vals = req.pack()
            print("Addr: 0x%08x" % vals.addr)

            await self.proxy.finish_item(req)
```

Listing 11: Starting a Python-Implemented Sequence.

While it's interesting to see the mechanics that make it possible to find the available class fields and access their values without altering the SystemVerilog source, the resulting user experience is most important. The code snippet in *Listing 11* calls the *pack* method on the sequence item after it is randomized. The object that is returned defines fields corresponding to the fields registered with *uvm_field* macros. The returned object contains the value of fields, but is otherwise independent of the UVM object. Python code can access the values, iterate through fields defined by the class, and otherwise use the *value* object as any other Python class. But, setting the value of fields in the *value* object will not change the value of fields in the UVM object.

B. Setting Field Values

The UVM *unpack* method provides a mechanism that enables the value of UVM class fields to be set. Setting UVM field values can be used to fully specify field values of sequence items. It can also be used to work cooperatively with the constraint solver. The PyHDL-IF library enables Python code to call *randomize* on UVM objects to randomize the contents, but it doesn't enable Python code to add new constraints. Setting field values allows Python code to use another common design pattern: randomization control knobs.

```
class seq_item extends uvm_sequence_item;
  bit              ctrl_addr_page;
  bit[1:0]         addr_page;

  rand bit [7:0]   addr;
  rand bit         write;
  rand bit [31:0]  data;
  rand bit [3:0]   tid;

  // Support full control of the page
  constraint addr_page_c {
    if (ctrl_addr_page) {
        addr[7:6] == addr_page;
    }
  }

  constraint data_c {
    if (write) data != 32'h0;
  }
endclass
```

Listing 12: SystemVerilog Sequence Item with Control Knobs.

The sequence item in *Listing 12* allows the address "page" (the upper two bits) to be controlled using a pair of control-knob fields. When *ctrl_addr_page* is set to 1, the upper bits of *addr* will be equal to the *addr_page* control-knob field. When it is 0 (the default), *addr* will be fully random.

```
class PyRandSeq(uvm_sequence_impl):
    async def body(self):
        # Exercise each page in turn
        for i in range(4):
            req = self.proxy.create_req()
```

```
            # Get the current values
            val = req.pack()

            # Configure the knobs
            val.ctrl_addr_page = 1
            val.addr_page = i

            # Set the field values
            req.unpack(val)

            # Randomize with control knobs
            req.randomize()

            await self.proxy.start_item(req)
            await self.proxy.finish_item(req)
```

Listing 13: Controlling Randomization from Python.

The *unpack* method provides a method to control randomization from Python by setting the value of control knobs. Note the sequence above:

- Call *pack* to get a Python object with the current values
- Configure desired values
- Call *unpack* to set new values

VI. Supporting Python Development Tools

The previously-described functionality is sufficient to enable Python to dynamically interact with a UVM testbench. But, it's important to consider the developer experience. Python provides a wealth of tools, and most of these operate on Python source code. Static checking tools such as MyPy[5] can catch errors before the Python code is executed. Integrated development environments provide code-navigation, content assistance, and in-line access to documentation that improve developer productivity. AI assistants leverage source code, along with static checkers, to take on larger "spec to code" style tasks, allowing the AI assistant to both suggest and validate content.

A common aspect of all of these tools is that they operate on Python source code. The PyHDL-IF library allows Python code to find UVM elements of interest at runtime. This is great for integration efficiency, but doesn't support the operation of these critical development tools. Fortunately, the same runtime-integration features can be used to automatically extract a Python representation of the UVM testbench. These *mirror* Python classes are not required for Python to interact with the UVM testbench, but provide two critical capabilities. First, they provide tools insight into how to properly interact with the UVM testbench via Python. And, secondly, they enable unit testing Python testbench components independent of the simulation environment.

PyHDL-IF provides a special-purpose UVM test named *pyhdl_uvm2py* whose purpose is to read UVM-based classes and create corresponding *mirror* Python classes.

```
tasks:
- name: extract-py-mirrors
  uses: "hdlsim.${{ sim }}.SimImage"
  needs: [sim-img, pyhdl-if.DpiLib]
  with:
    plusargs:
    - UVM_TESTNAME=pyhdl_uvm2py
    - pyhdl_outdir=${{ rootdir }}/python
```

Listing 14: Mirror-Class Extraction Simulation Run.

As shown above generating python mirror classes is initiated by running the *pyhdl_uvm2py* on the simulation image that contains the target UVM testbench environment. Additional *plusargs* specify where to output the Python classes and support control over which UVM classes are converted.

```
import dataclasses as dc

@dc.dataclass
class spi_reg_block(uvm_reg_block):

  CTRL : reg_CTRL = dc.field()
  STATUS : reg_STATUS = dc.field()
  CLKDIV : reg_CLKDIV = dc.field()
  SS : reg_SS = dc.field()
  TXDATA : reg_TXDATA = dc.field()
  RXDATA : reg_RXDATA = dc.field()
```

Listing 15: Python Mirror Register Block Class.

The result is a series of Python classes that reflect the SystemVerilog UVM elements that are accessible from Python. The Python mirror class above corresponds to the *spi_reg_block* SystemVerilog class shown earlier. Note that UVM named fields are presented as Python class attributes along with their types. This enables static checking and content assistance tools to validate the correctness of user code, and provide suggestions to the user during the development process.

VII. Unit Testing your Testbench Code

The goal of design verification is to ensure that the model (typically RTL) of a design matches the specification. But, all code we write is subject to bugs. While we want to focus our efforts on finding bugs in the hardware design, realistically we will spend a certain amount of time finding and fixing bugs in the testbench code as well. Doing so as quickly and efficiently as possible allows us to focus the bulk of our energy on design bugs.

Testing testbench components in their most-minimal form raises productivity by finding implementation issues as early as possible when they are easiest to correct. Applying unit testing, a core software discipline, helps to boost productivity when applied to testbench components as well.

Unit testing is also a critical tool when working with AI coding assistants. While AI coding assistants make mistakes, having them create and run tests acts as a self-correction mechanism and significantly improves results.

Unit testing in a SystemVerilog/UVM testbench can be a bit challenging. In Python, the *mirror* classes that are automatically generated from the UVM definition make the process much simpler.

Unit testing is also a critical capability when working with agentic AI coding assistants. While AI assistants make mistakes when generating code, they are also capable of resolving these errors using feedback unit tests.

```
@dc.dataclass
class MemTx(uvm_sequence_item):
    addr : int = dc.field(default=0)
    we : bool = dc.field(default=False)
    data : int = dc.field(default=0)
    size : int = dc.field(default=0)
```

Listing 16: Python Mirror Class for MemTx Transaction.

AI assistants rely on having proper *context* about the task. The Python *mirror* class shown in in *Listing 16* corresponds to an existing SystemVerilog sequence class in the testbench, and is provided to the AI assistant as context.

```
from .mem_tx import MemTx

class MemScoreboard(object):

    def write(self, t : MemTx):
        pass
```

Listing 17: Scoreboard Skeleton.

The scoreboard template shown in *Listing 17* references the mirror-class type, and provides more context on the desired scoreboard structure.

```
Implement the write method in mem_scoreboard:
- Must check that accesses are only to 0..0xFF,
  0x200..0x2FF, 0x400..0x4FF, 0x600..0x6FF
- Writes may only be to the ranges 0x600..0x6FF
- Track writes and compare reads against the
  expected value.
- Report an error on mismatch

Write some unit tests in mem_scoreboard/tests.
Exercise corner cases and ensure tests pass
before concluding the task
```

Listing 18: LLM Scoreboard Prompt.

The prompt in *Listing 18* is used, along with the context data, by the AI assistant to create a simple memory-checking scoreboard and unit tests. As per the instructions, the AI assistant uses the unit tests to identify errors in the code it generates.

```
def test_write_mask_size1_and_mismatch():
    sb = make_sb()
    # Only low byte should be stored/compared
    sb.write(MemTx(addr=0x600, we=True,
        data=0x1234, size=1))
    sb.write(MemTx(addr=0x600, we=False,
        data=0x34, size=1))
    assert sb.errors == 0
    # Mismatch on the next read
    sb.write(MemTx(addr=0x600, we=False,
        data=0x35, size=1))
    assert sb.errors == 1
```

Listing 19: Scoreboard Unit Test.

An example of an AI generated unit test for the scoreboard is shown in *Listing 19*.

The presence of the Python *mirror* objects simplifies the process of creating unit tests. Continuing to use and extend the unit tests as changes are made to the scoreboard helps to catch mistakes early without needing to run and debug a full simulation.

VIII. Future Work

While the PyHDL-IF library is ready to be deployed today, there are several areas of enhancement to explore in the future.

Currently, the UVM-specific aspect of the library focuses on pre-defined UVM class APIs. A future effort will extend the UVM portion of the library to support UVM-derived classes with custom APIs.

It's common to capture class and method meta-data in SystemVerilog as comments. Adding support for attaching meta-data to UVM class types enables documentation captured in SystemVerilog to be attached to classes and propaged to the Python *mirror* classes generated by PyHDL-IF. Propagating documentation to generated Python classes will enhance the utility of this *mirror* classes to Python code analysis and AI coding assistant tools.

Finally, expanding coverage of the UVM API will remain an ongoing task based on usecase requirements.

IX. Conclusion

Leveraging Python to implement the software-like aspects of our testbench environments is attractive due its popularity and sizable ecosystem. Making use of the UVM library's well-defined API enables Python to integrate with existing environments in a low-effort and high-performance manner. The same features enable automatic creation of a Python

class API that mirrors the testbench API and enhances the support provided by Python development tools. All of these features are implemented in PyHDL-IF, an Apache 2.0-licensed open source library, enabling engineers to quickly and productively add Python to existing UVM testbench environments.

A. References

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