2024 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

MUNICH, GERMANY
OCTOBER 15-16, 2024

Harnessing the Strength of Statistics and Visualization in Verification

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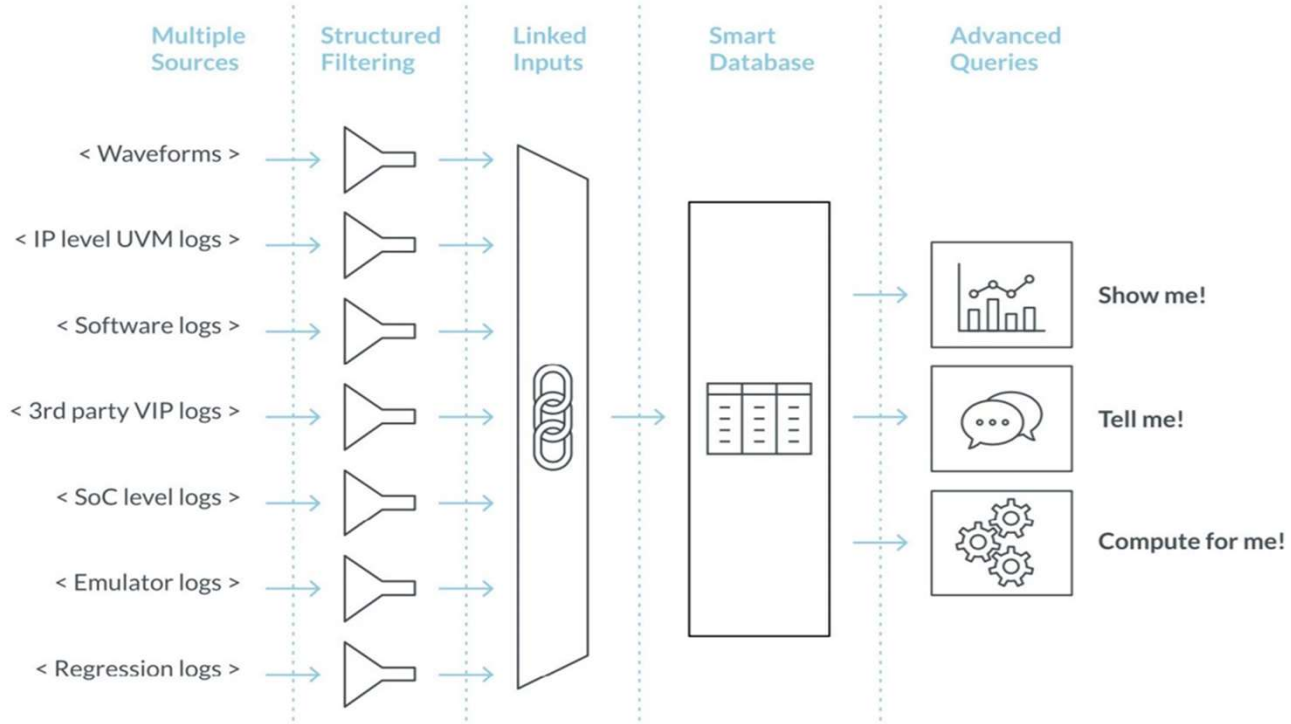
Objectives

- Improve verification techniques with statistics and visualization
- Highlight their untapped potential in simplifying processes
- Address challenges of managing large-scale data in verification
- Emphasize the need for high-quality Big-Data techniques
- Introduce new transaction paths and visualization methods
- Demonstrate the practical benefits in solving data challenges

Methodology



Typical verification challenges

1. Vast amounts of data from multiple sources make analysis and conclusions immensely time-consuming and error-prone
2. Repeated processes lack a consistent methodology, making them inefficient
3. Distribution of transaction, for qualifying test and verification environment
4. Utilization of outstanding transactions, for improved performance
5. Pre-existing code not written by the verification engineer
6. Detection of repetitive transaction patterns irregularity, for measuring throughput and detection of transfer timeouts
7. Stress and performance test quality assessment

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Data Field Correlation and Distribution

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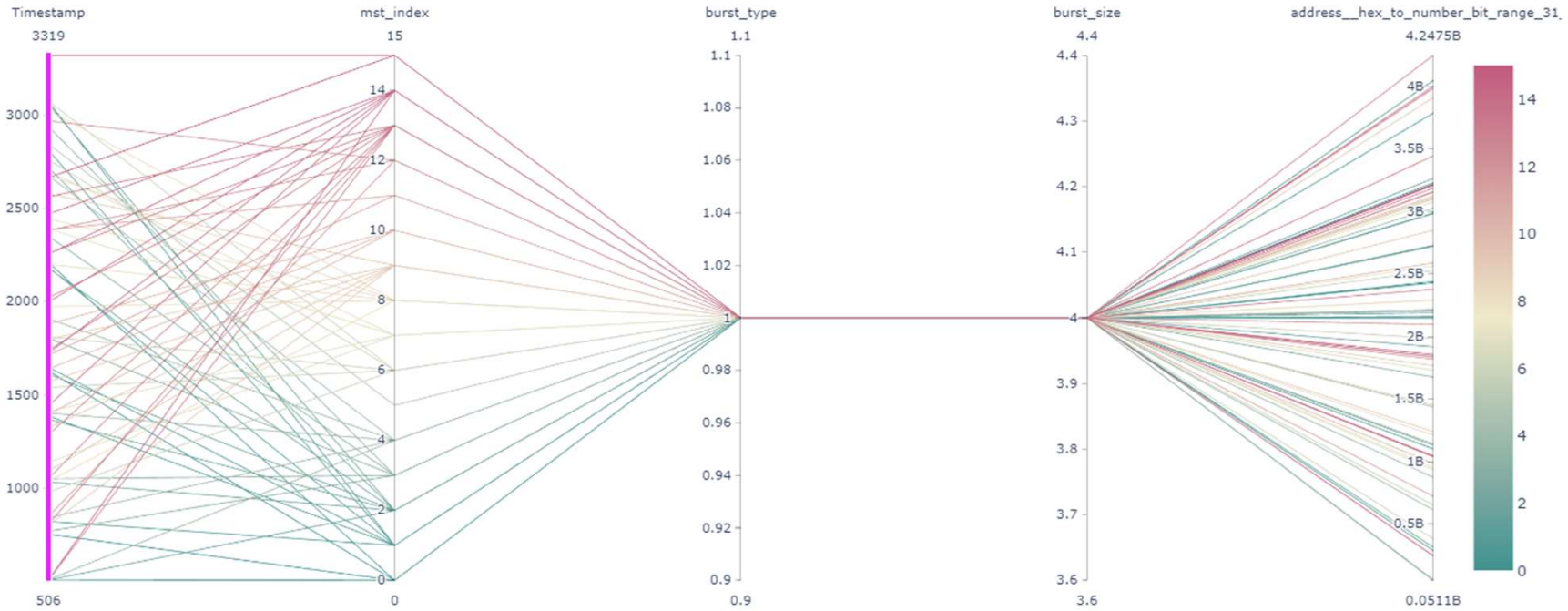
Transaction data field correlation



Transaction path data field correlation

This visualization reveals the density and trends of outstanding transactions, highlighting the link between errors and peak transaction levels.

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Exposed Constraints Issues

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Transition probability matrix

- Expected command life cycle:

command_desc → data_desc → data_pointers_fetch → multiple single_transfers → cycle complete or new data_desc

- Before fixing the bug constraint (left): The transition probability *data_desc → data_desc* was 0.26, indicating an illegal transition not aligned with the specification
- After fixing the bug constraint (right): Correct transitions were observed.

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Pre-Written Code from Other Developers

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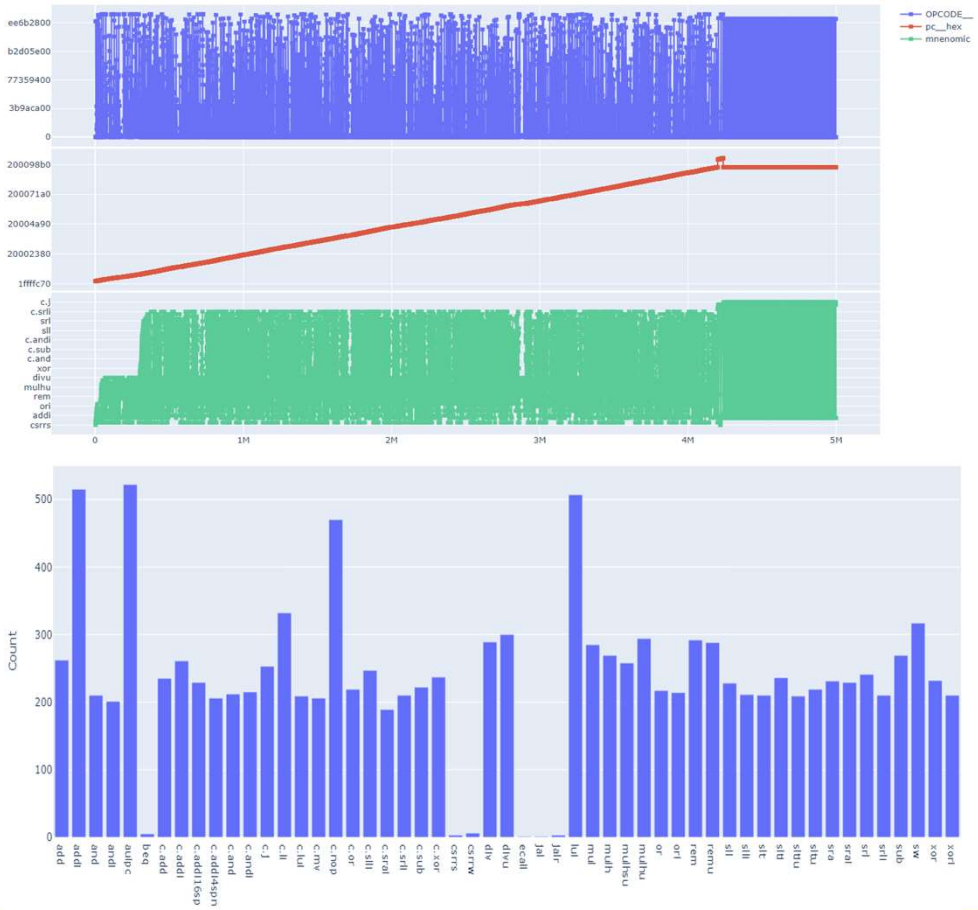
RISC-V Example

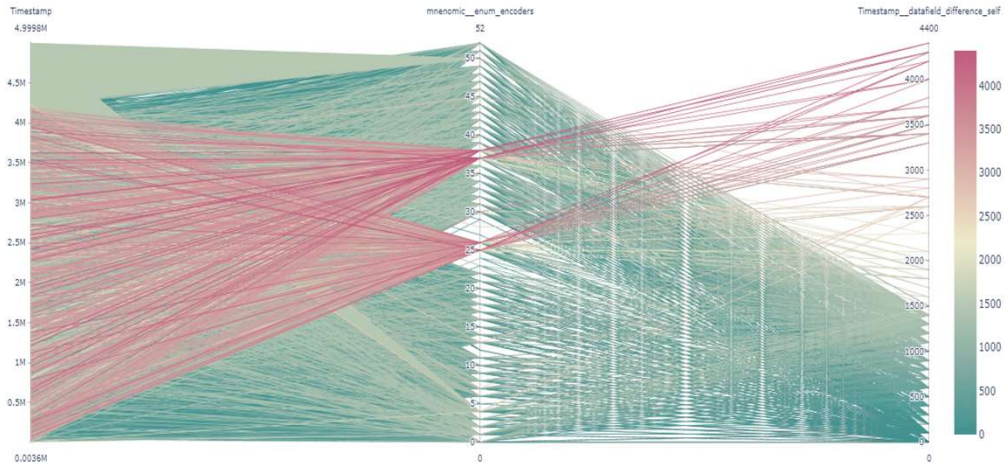
```
//Sim Time,      Cycle : #inst  hart   pc    opcode    reg=value   ; mnemonic
//-------------------------------------------------------------------
      3575,         30 :       #1 0 20000000 f14022f3  t0=00000000 ; csrrs    t0,csr_f14,zero
      3675,         31 :       #2 0 20000004 00004301  t1=00000000 ; c.li     t1,0
      3775,         32 :       #3 0 20000006 00628263              ; beq      t0,t1,0x2000000a
      6275,         57 :       #4 0 2000000a 00000e97  t4=2000000a ; auipc    t4,0x0
      7775,         72 :       #5 0 2000000e 00ce8e93  t4=20000016 ; addi     t4,t4,12
      7875,         73 :       #6 0 20000012 000e8067              ; jalr     zero,t4,0x20000014
     10475,         99 :       #7 0 20000016 400019b7  s3=40001000 ; lui      s3,0x40001000
     10575,        100 :       #8 0 2000001a 10498993  s3=40001104 ; addi     s3,s3,260
     11975,        114 :       #9 0 2000001e 30199073              ; csrrw    zero,csr_301,s3
     12075,        115 :      #10 0 20000022 00013c97  s9=20013022 ; auipc    s9,0x13000
     12175,        116 :      #11 0 20000026 192c8c93  s9=200131b4 ; addi     s9,s9,402
     12175,        116 :      #12 0 2000002a 0000a997  s3=2000a02a ; auipc    s3,0xa000
     13475,        129 :      #13 0 2000002e f2698993  s3=20009f50 ; addi     s3,s3,-218
     13575,        130 :      #14 0 20000032 0019e993  s3=20009f51 ; ori      s3,s3,1
     13675,        131 :      #15 0 20000036 30599073              ; csrrw    zero,csr_305,s3
```



Assessment of open-core RISC-V DV solution

Visualization and statistics simplified the quality evaluation of the open-source solution, particularly:

- Randomization level of SW for CPU verification
- Distribution of instruction
- Instructions with highest execution time



Correlation between instructions and their duration

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Stress Test Quality Assessment

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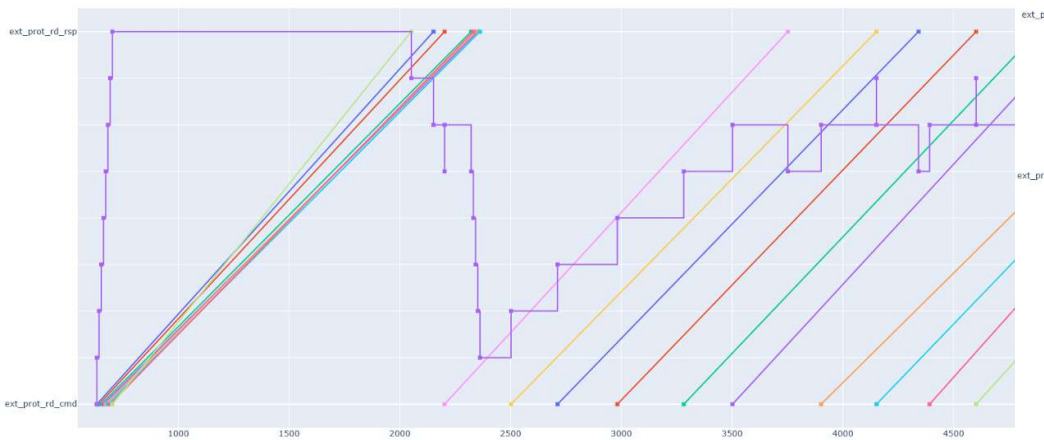
Transaction flow overlaid with outstanding transactions count



Statistical analysis allowed us to zoom in on the crucial performance bug, which prevented the module from working at its full capacity after reaching the maximum threshold.

Conclusion

Statistics helps with understanding random test scenarios, identifying constraint issues, and uneven data distribution.

Statistics and visualization improve the analysis and reliability of SoC behavior by processing Big-Data from simulation results

Visualization helps uncover correlations between errors, simulation data, and potential design issues

Viewing simulation as a **Big-Data set offers engineers macro-level insights,** making it easier to pinpoint specific problems

With the rise of **open-source and AI-generated code,** statistics and visualization are set to become **vital tools for verification and diagnostics.**

Questions


Statistics?
01
OPTION
02
OPTION
Visualization?
Distribution?
03
OPTION
04
OPTION
Verification dataset?