"Shift left" Hierarchical Low-Power Static Verification Using SAM

Bharani Ellore bharani.ellore@amd.com, Parag Mandrekar parag.mandrekar@amd.com, Himanshu Bhatt himanshu@synopsys.com, Susantha Wijesekara susantha@synopsys.com, Bhaskar Pal bpal@synopsys.com

Why is Signoff Abstract Model (SAM) Flow Critical?

- Increasing design sizes
- LP Signoff in flat SoC takes a long time
- For some designs more than 26 hours
- Next generation SoCs growing
- Expected to be 1x bigger and can’t rely on full-flat run
- Integration of large number of IPs with standalone UFM files validated at block level
- Existing hierarchical flows do not cover all aspects of Signoff

SAM vs Blackbox

SAM Hierarchical Flow Methodology

Creating and Reading a SAM Model

Reading SAM Model

Writing SAM Model

How is QoR Guaranteed?

- QoR guarantee is MUST for Signoff confidence
- Multiple QoR validation flows are developed
  - Subtractive QoR Flow:
    - TOP+SAM Violations => Full Flat Violations – Block Violations
  - Additive QoR Flow:
    - Block Violations + TOP+SAM Violations => Full Flat Violations

Subtractive QoR

Additive QoR

Compare Violation Utility Usage and Outputs

Results on Customer Designs

VC LP Hierarchical Verification Flows and Tradeoffs

Accuracy vs Performance

Bbox flow ETM flow Sam flow