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Reset and Initialization:
the Good, the Bad and the Ugly

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Agenda

- Initialization Challenge
- The Register Status
  - 5 scenarios of register corruption
  - Assertions for registers
- The Initialization Sequence
  - The 3 phases
- Verification Methodology
  - Results
  - 5 corruption cases
- Summary and Reference

Initialization Challenge

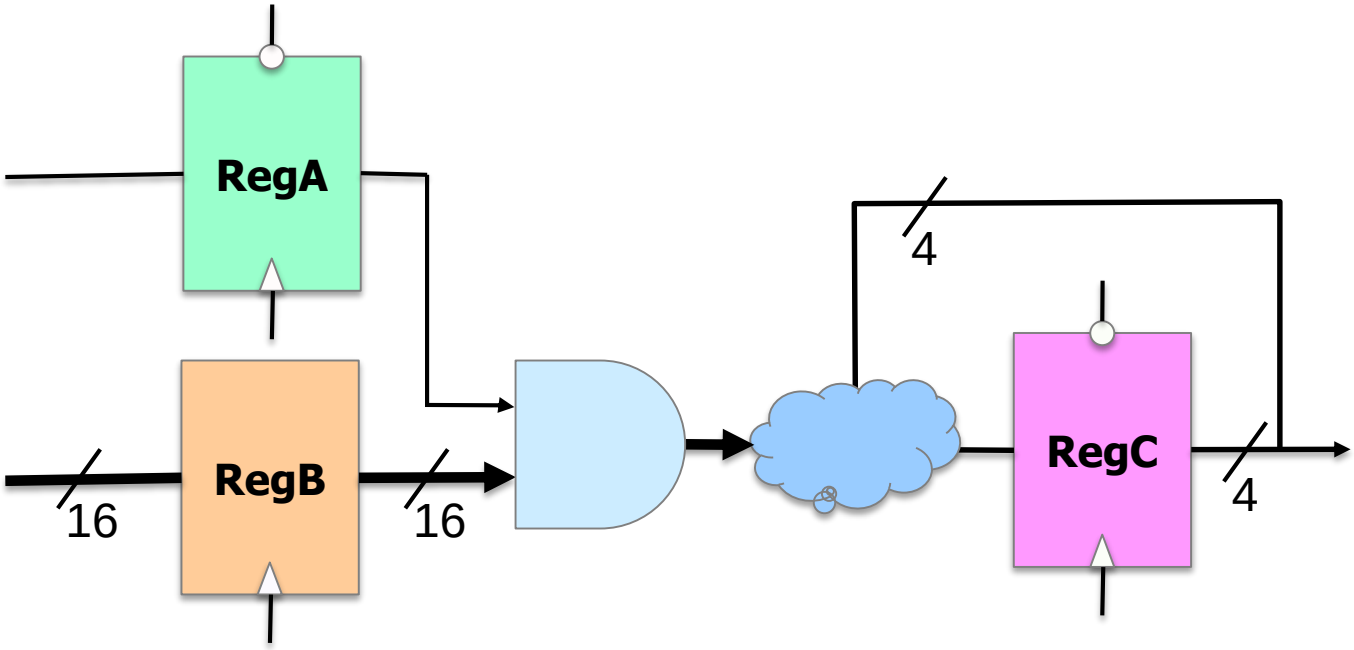
- One daunting challenge of developing a low-power SoC design is how to full verify its power-up, reset and initialization sequences.
- All of these possible reset sources are combined together to initialize the design
  - Power-on reset
  - Hardware reset
  - Software reset
  - Interrupt reset
  - Watchdog timer reset

The Register Status

- To understand the internal status of a design, our methodology classifies design registers into:
  - ***GOOD*** registers - are initialized properly,
  - ***BAD*** registers - are not initialized
  - ***UGLY*** registers - are initialized, but are subsequently corrupted

The Example

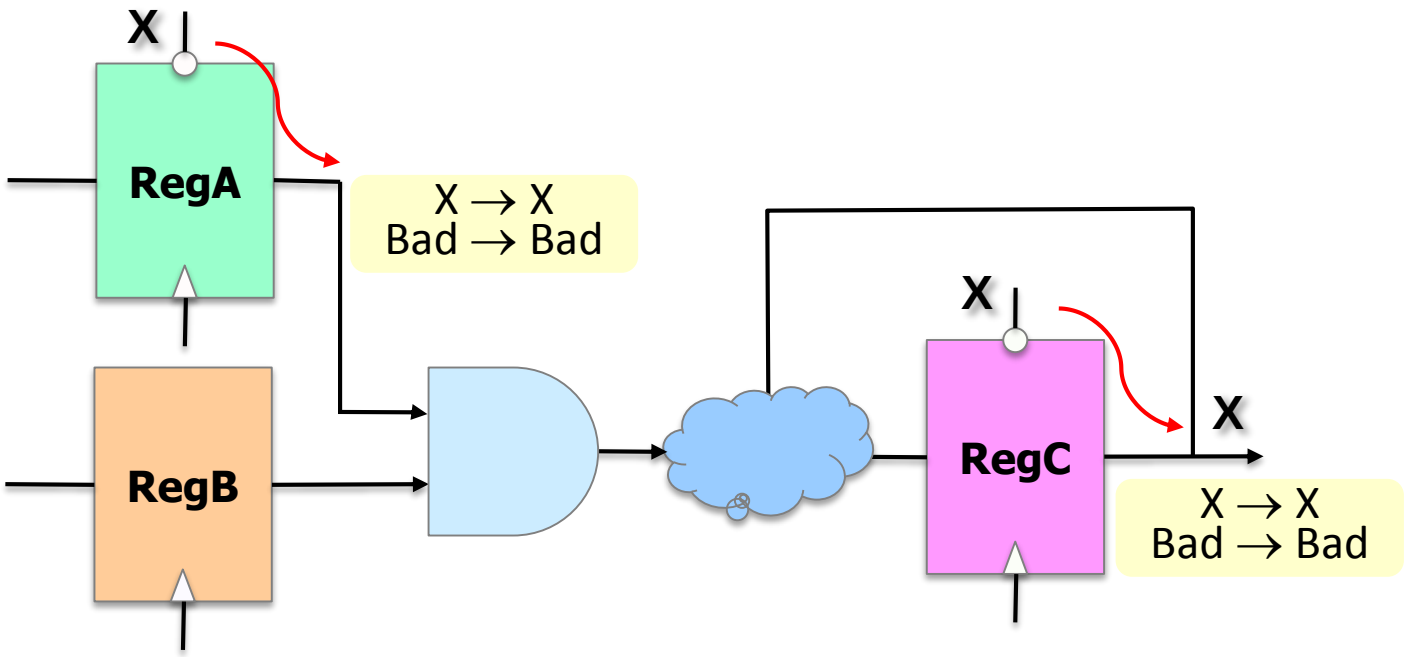
- RegC is a FSM state register whose input function logic contains the outputs of RegA and RegB



The FSM, RegC, should not be corrupted

The Scenario 1

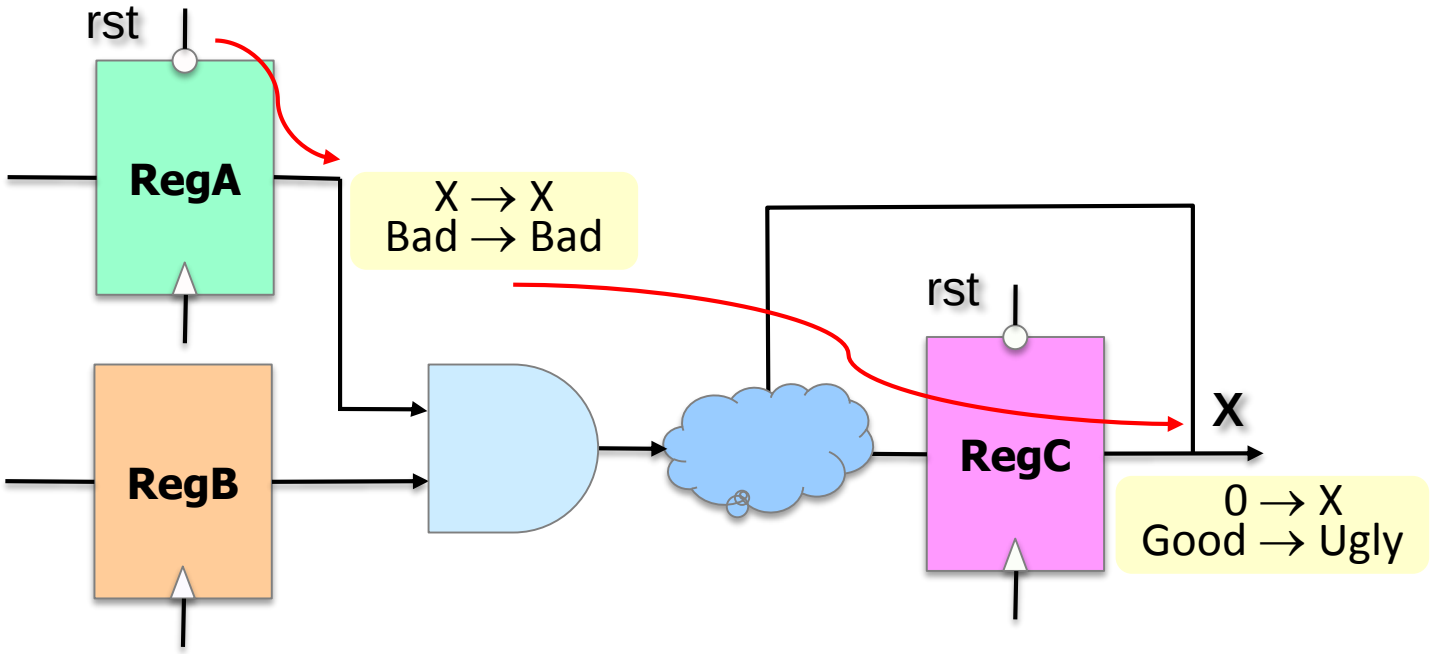
- Reset Propagation Problem
  - reset signals failed to reach RegA and RegC correctly



Same issue when clock signals are Xs

The Scenario 2

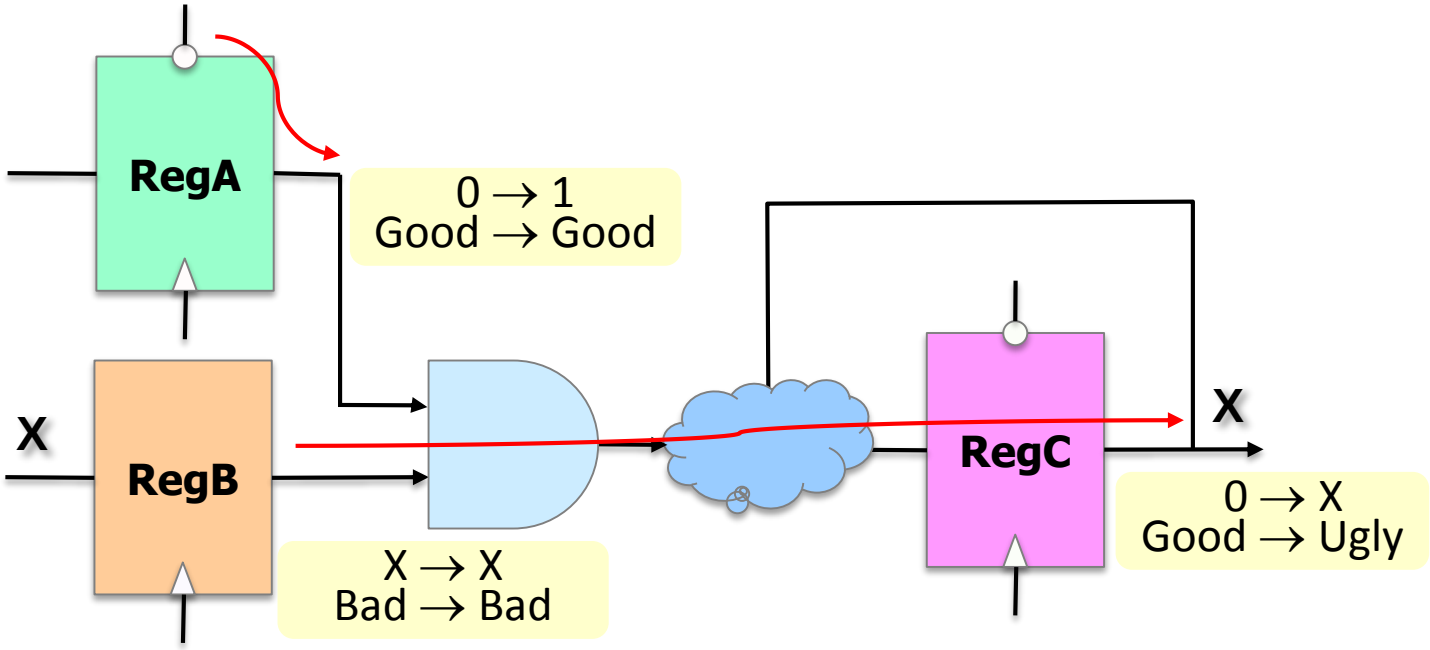
- Reset Timing Problem
  - reset signals to RegA and RegC did not meet protocol



RegA is not initialized correctly; RegC is corrupted by RegA.

The Scenario 3

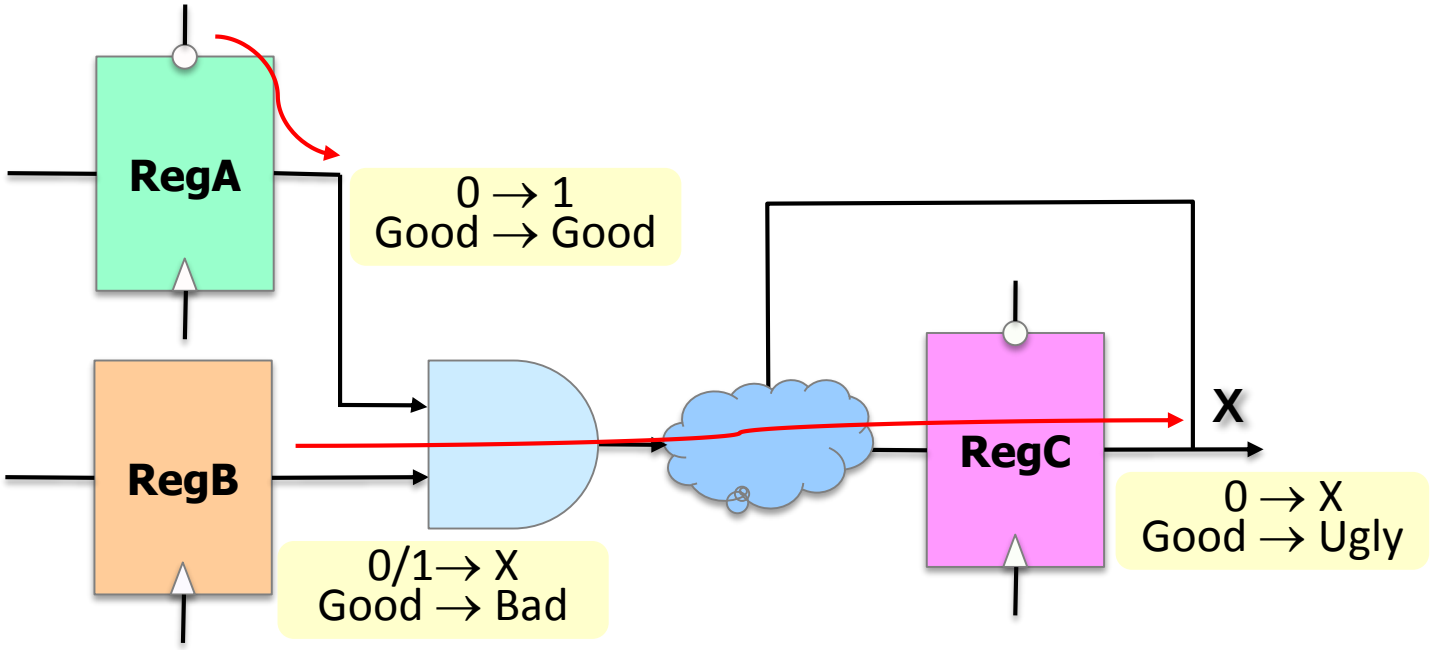
- X-propagation Problem:
  - reset signals assert correctly; RegB is not initialized



RegB is not initialized correctly; RegC is corrupted by RegB.

The Scenario 4

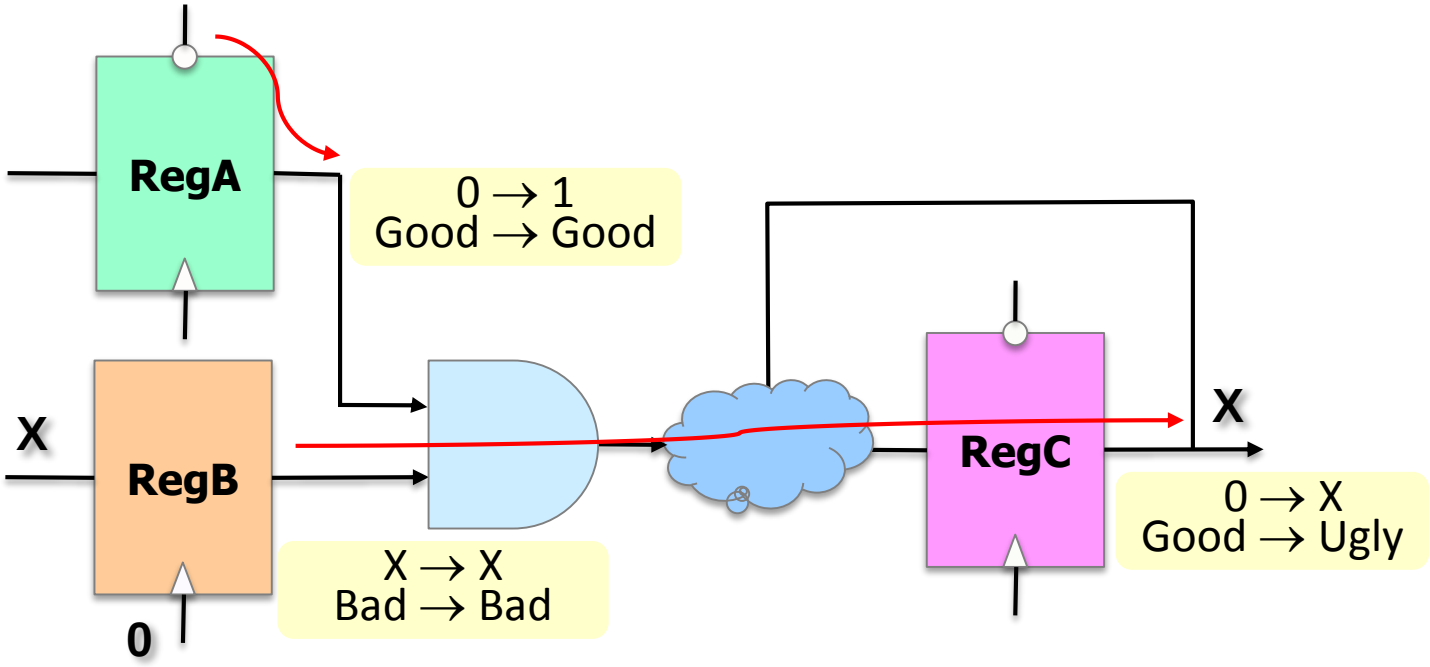
- Power Sequence and Isolation Problem:
  - RegB is powered down; driving X; and not isolated



RegB is powered down; RegC is corrupted by RegB.

The Scenario 5

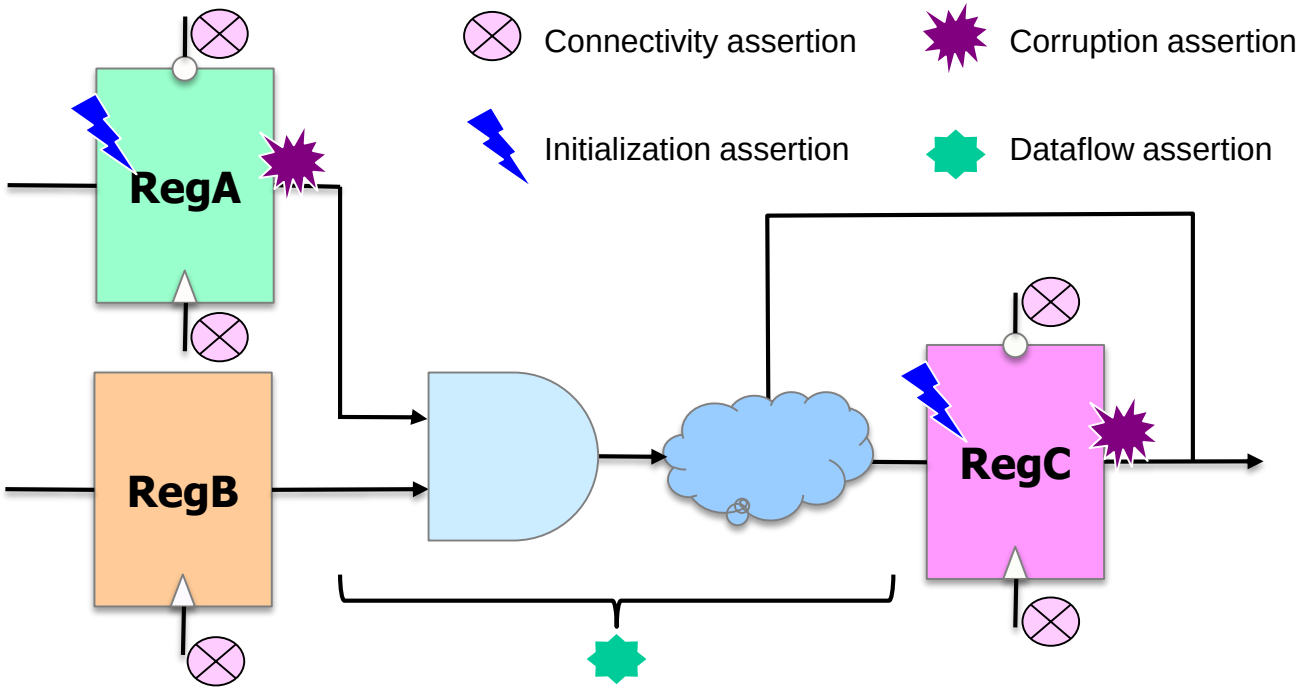
- Clock Gating Problem:
  - RegB is controlled by gated clock that is turned off



Clock to RegB is gated off; RegC is corrupted by RegB.

Assertions for Registers

- Ensure good clocks and resets
- Catch corruption with formal verification

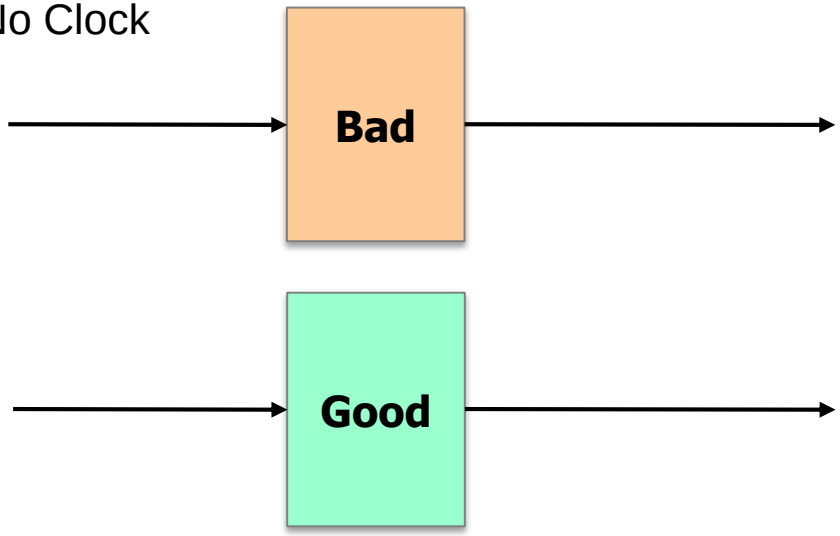


Some assertions are available implicitly with X-prop simulation

The Initialization Sequence

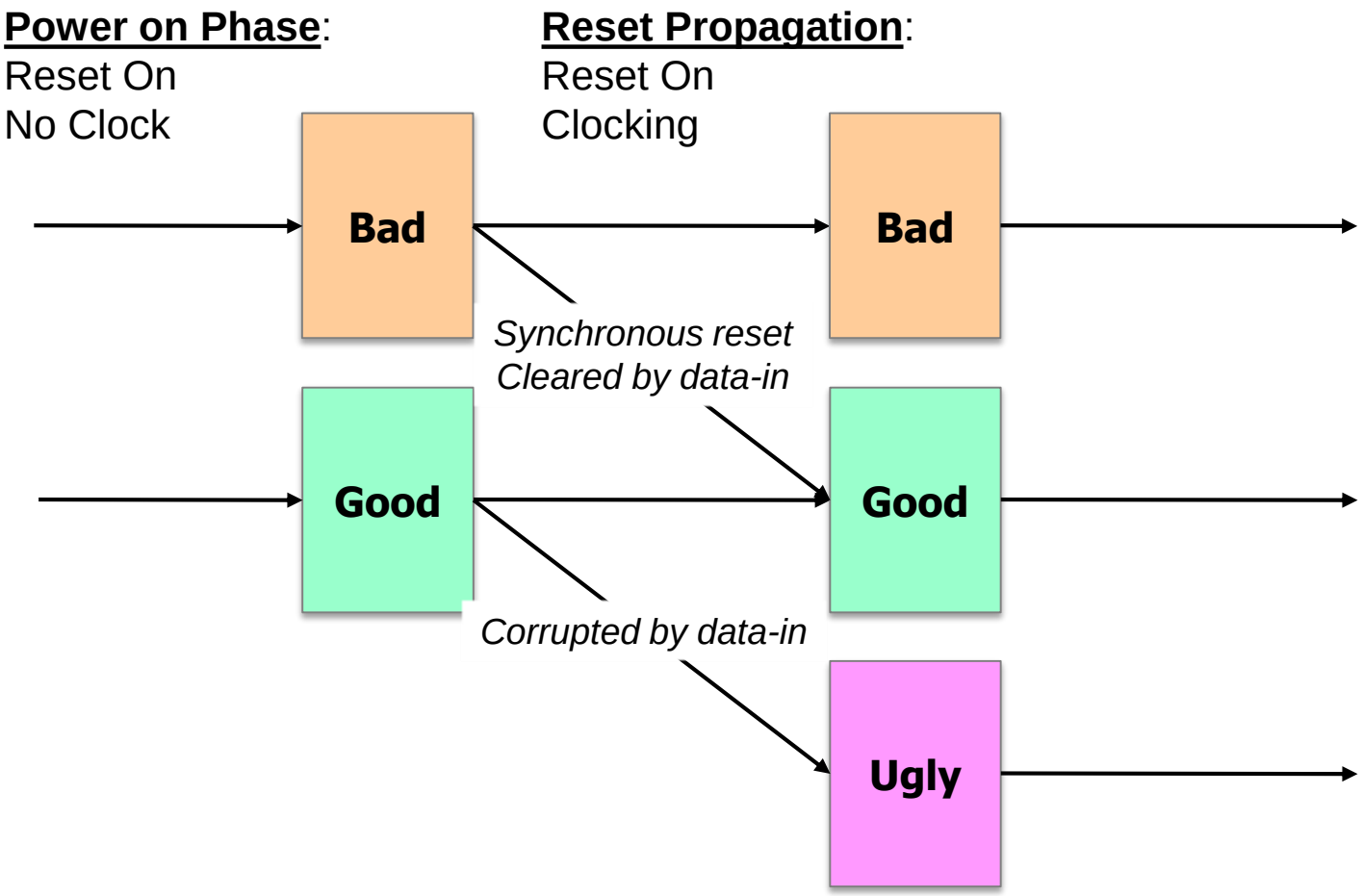
- 3 Phases in Initialization Sequence

Power on Phase:
Reset On
No Clock



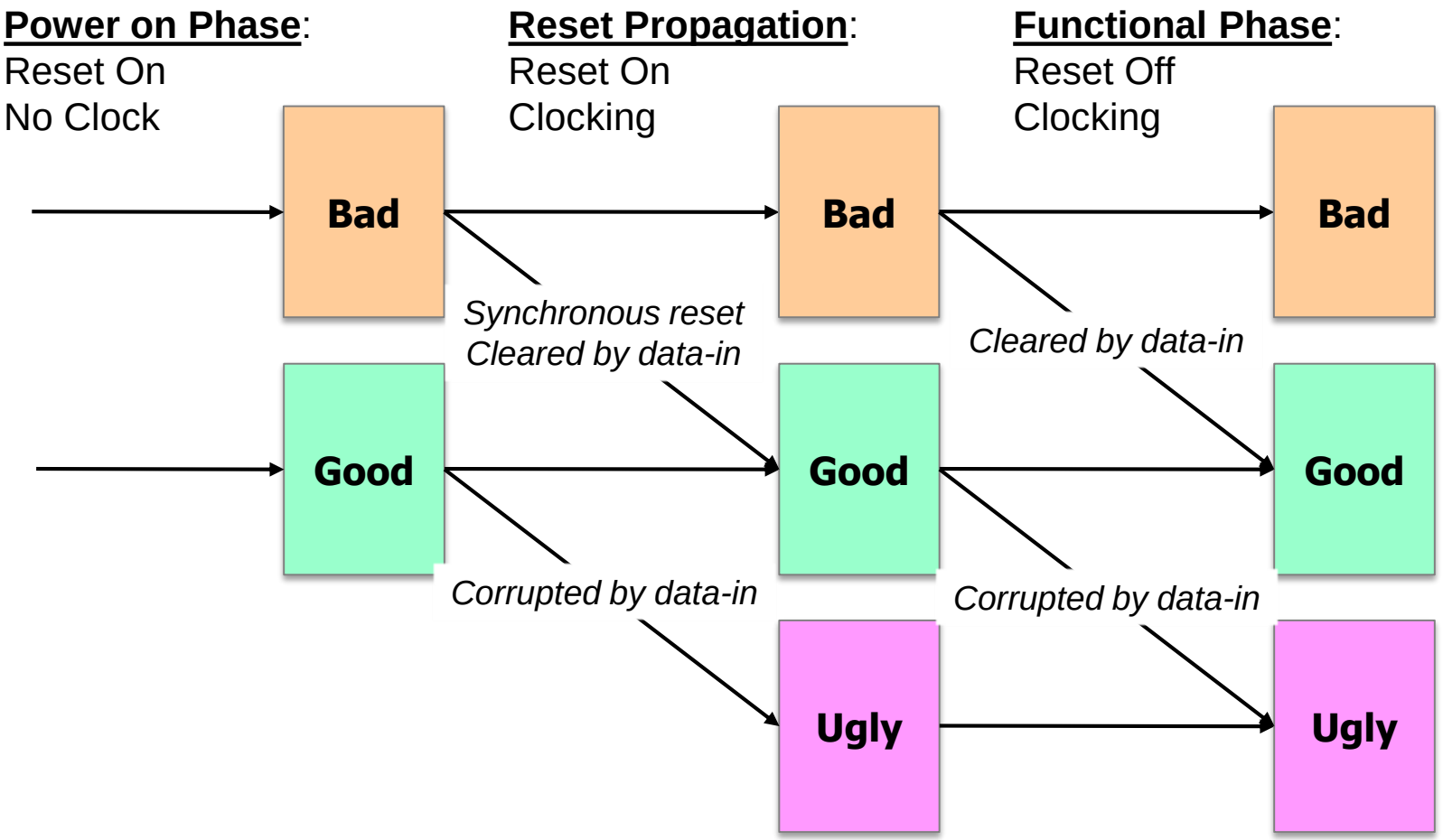
The Initialization Sequence

- 3 Phases in Initialization Sequence



The Initialization Sequence

- 3 Phases in Initialization Sequence



Verification Methodology

- Reset & Clock Trees
  - Static Checks on reset trees and clock trees
  - Formal connectivity check: verify control and distribution of reset and clock signals
- Initialization
  - X-prop simulation: monitor X propagation and usage
  - Formal initialization check: find true un-initialized registers; avoid X pessimism
- Initial Status
  - Formal modeling checking: ensure good registers are not corrupted; turned ugly

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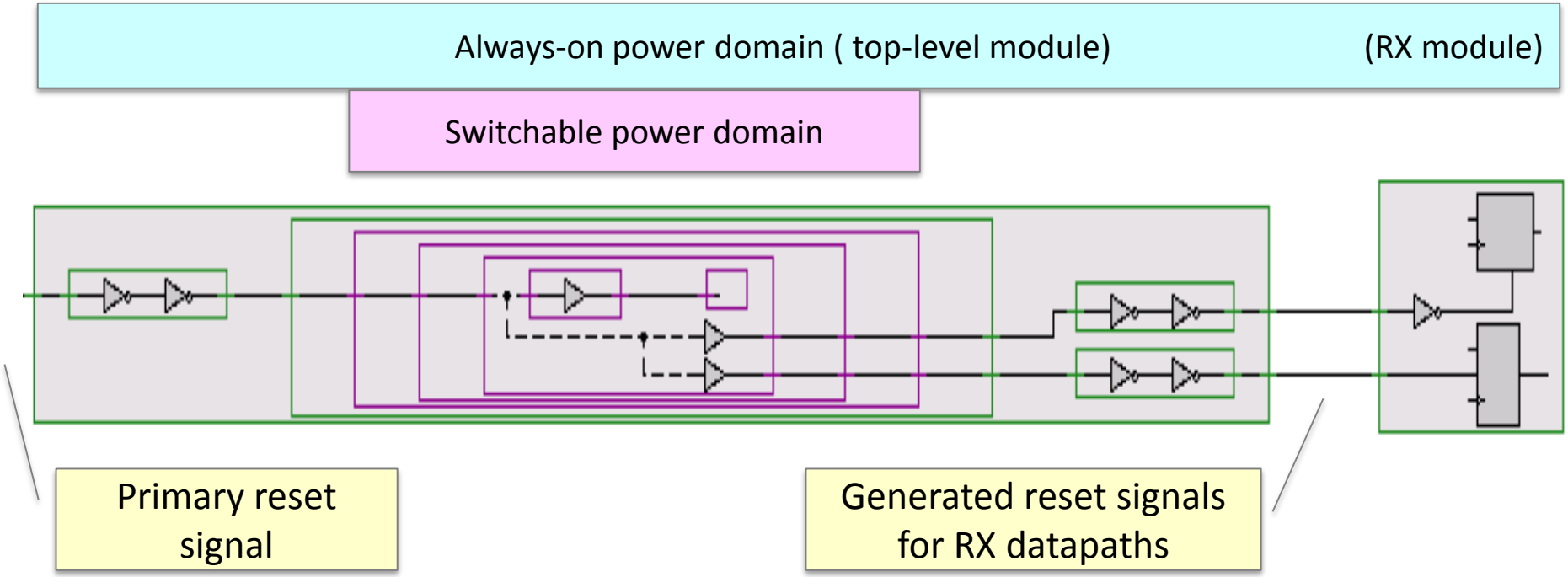
Results

Design Complexity	Design 1	Design 2	Design 3
Number of register bits	305	47016	43622
Number of latch bits	0	592	0
Number of RAMs	2	0	64
Number of asynchronous resets	3	13	16
Number of synchronous resets	2	33	35
Number of clocks	3	5	12

Register Status information	Design 1	Design 2	Design 3
Good registers	38%	50%	34%
Bad registers	58%	9%	66%
Ugly registers	4%	41%	<1%

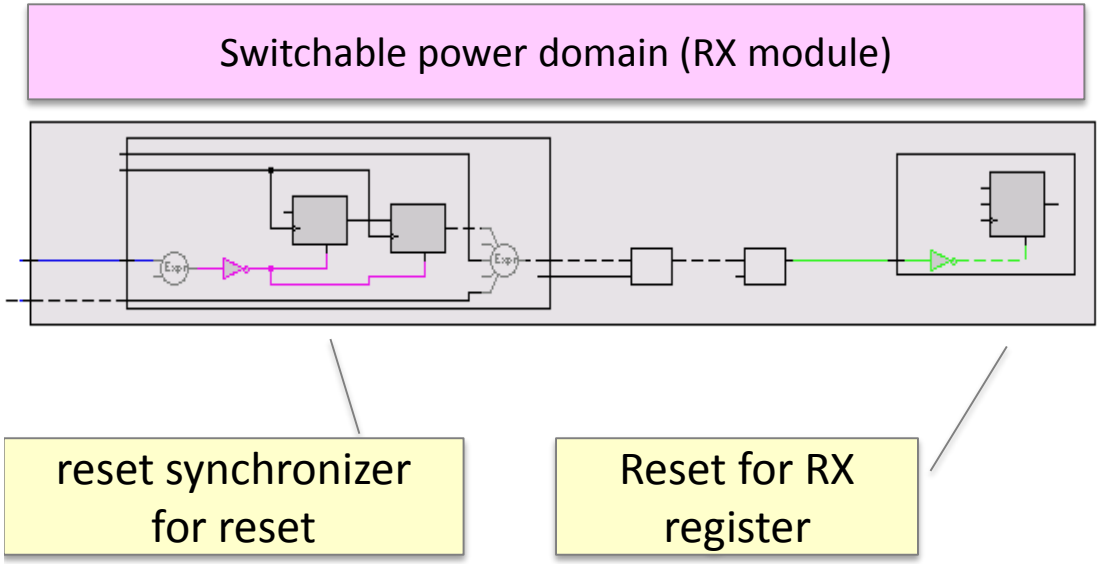
Corruption Case #1

- Reset signals passed from one module to another
  - Reset signals are unknown when via module is powered down

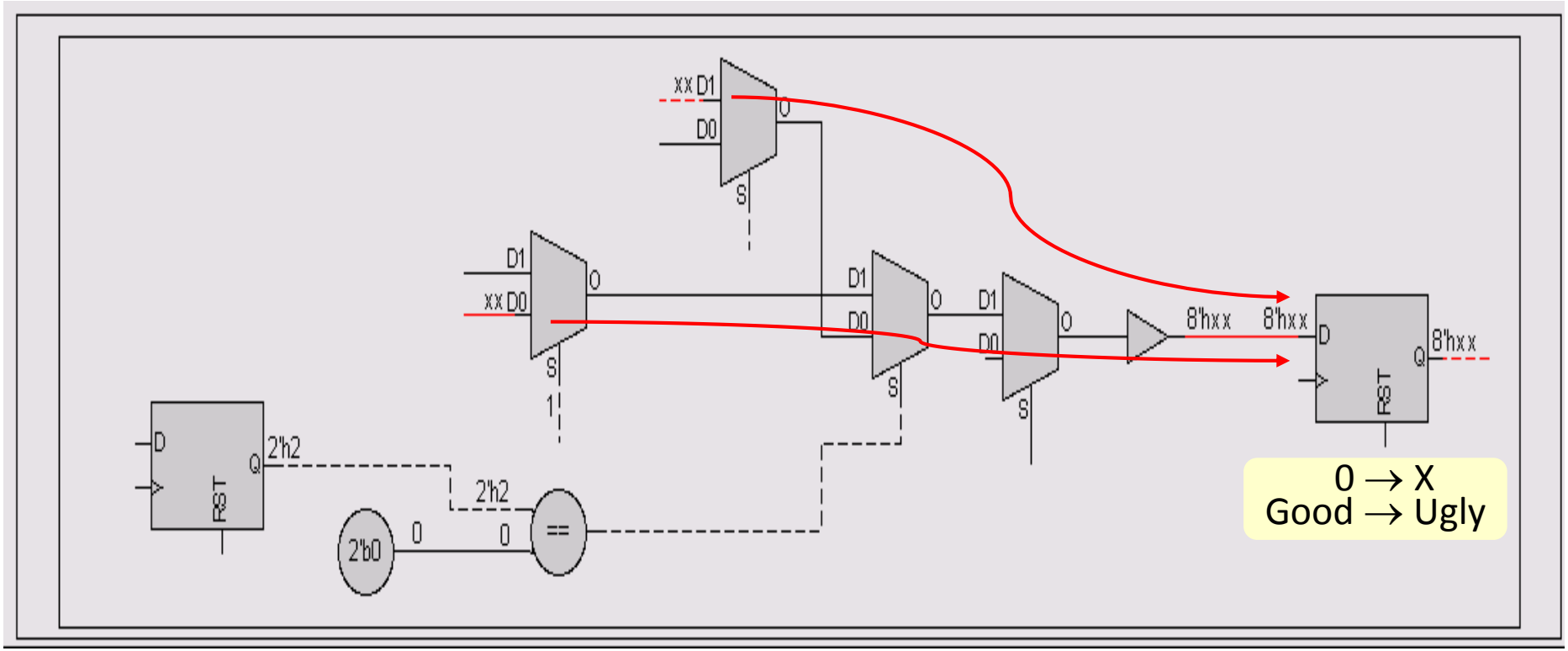


Corruption Case #2

- Reset control signals from another module
  - Foreign reset control signals may disable initialization after power cycle

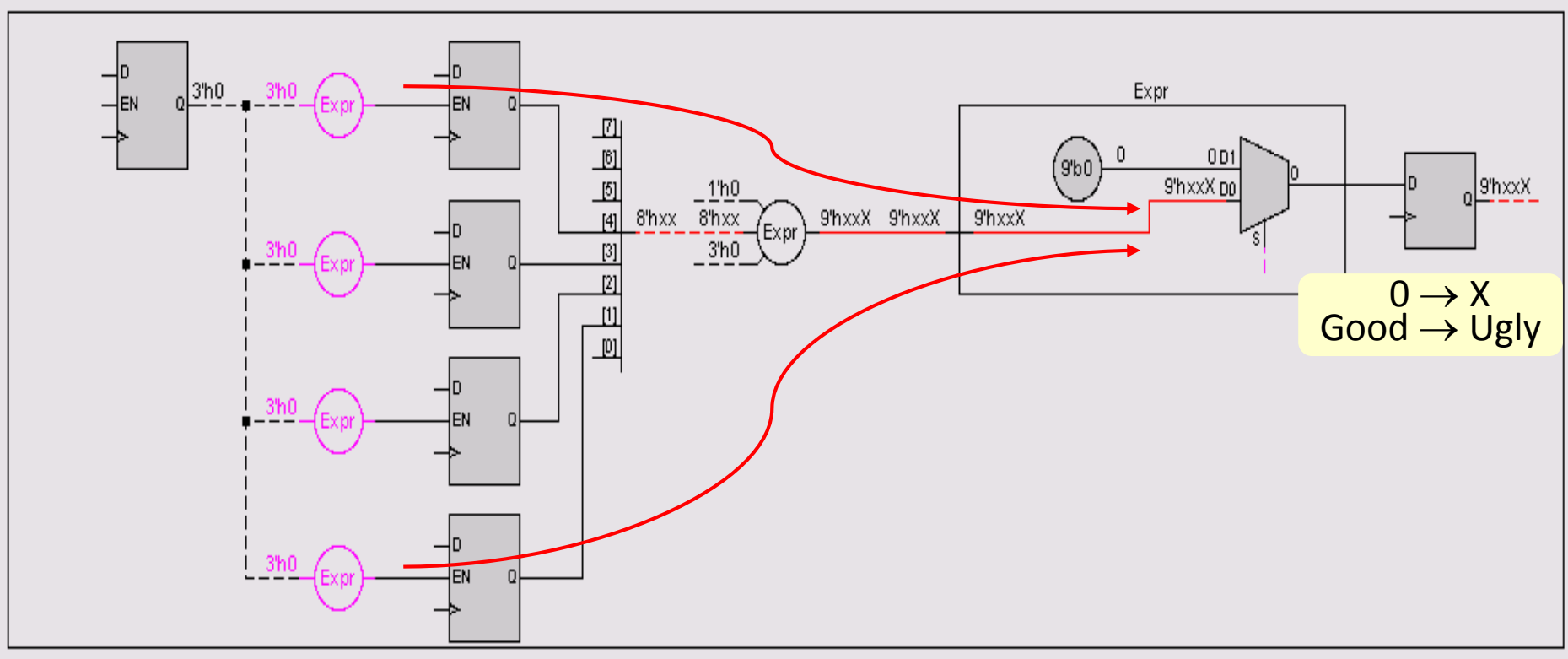


Corruption Case #3



- A good register was corrupted by an X source (an X assignment inside the default case branch).

Corruption Case #4



- A good (synchronous reset) register was corrupted by a group of uninitialized bad registers. The TX registers were not enabled and were holding their un-initialized values.

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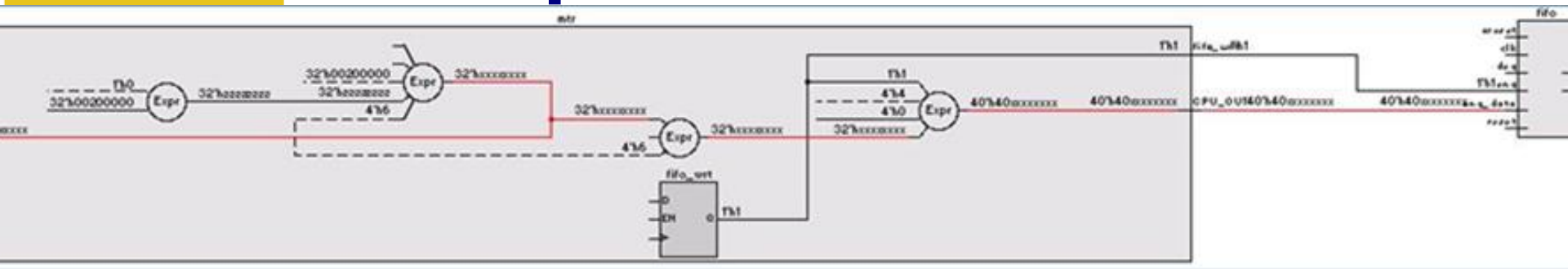
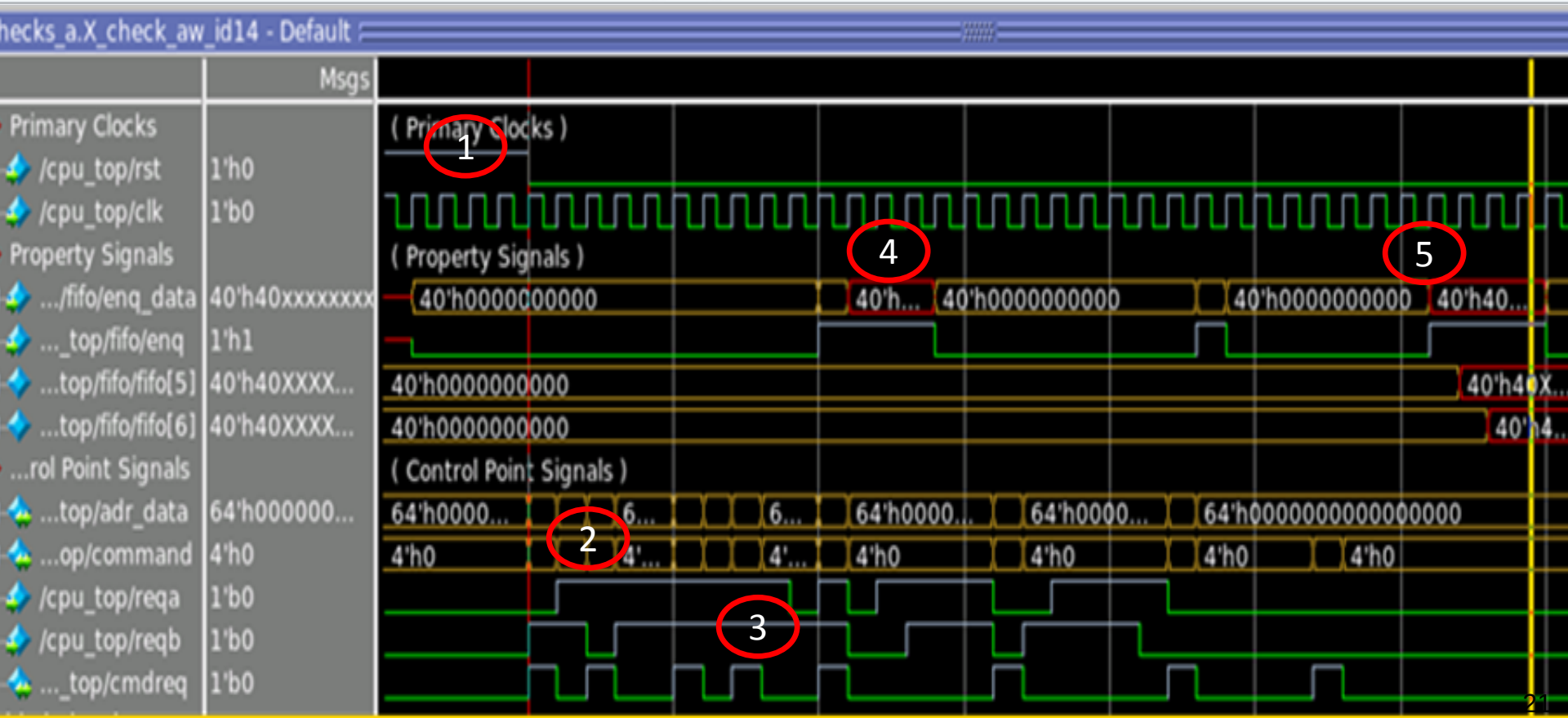
Corruption Case #5





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Summary

- As SoC designs get complex, reset and initialization become harder to verify

- We discussed:
  - The register status: Good, Bad and Ugly
  - Assertions for registers
  - The initialization sequence
  - Verification Methodology
  - Results

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Reference

DVCon 2015

- Multi-Domain Verification: When Clock, Power and Reset Domains Collide
  - Ping Yeung, Erich Marschner, Mentor Graphics
  - Kaowen Liu, MediaTek Inc.

- Addressing the Challenges of Reset Verification in SoC Designs
  - Chris Kwok, Priya Viswanathan, Ping Yeung, Mentor Graphics