

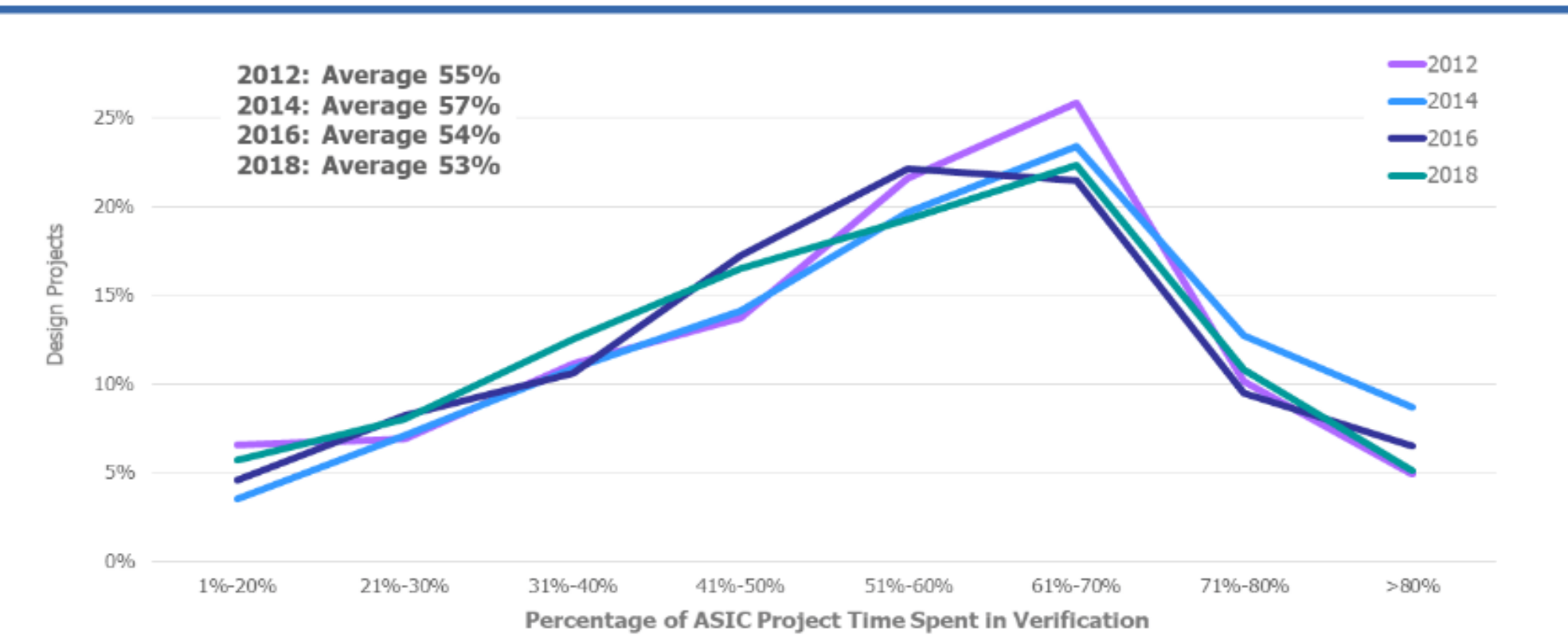
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## Abstract

As the technology node is shrinking, more and more IPs are getting integrated in single System-on-chip. In the System-on-chip, verification is getting more tedious, time consuming and challenging task. Based on case study on different internal and third-party IP's, realized that there are no mechanism nor internal / external tools available for doing the quick debug by understanding the test cases and its programming. Verification Engineers are putting manual effort to understand the IP programming in the test cases and there is no direct way to map the register programming to the Technical Reference Manual / Programmers model. This poster presents a tool RegAnalyzer which resolves this problem.

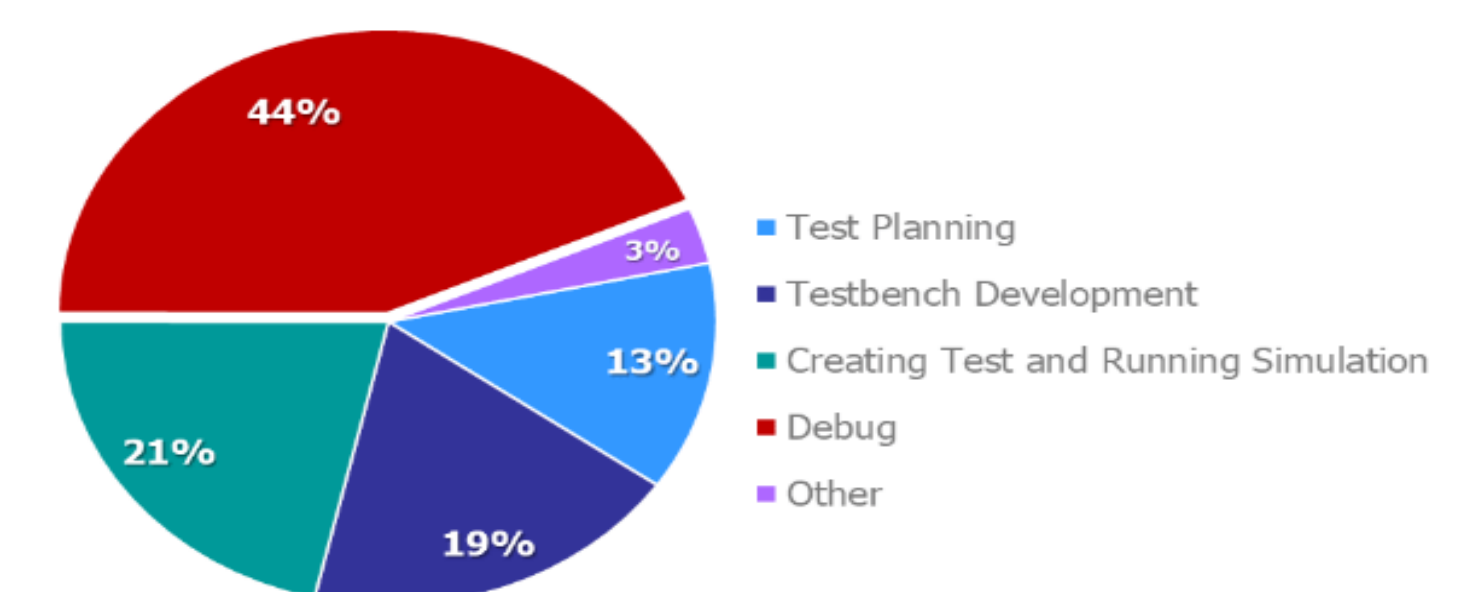
## Percentage of IC/ASIC Project Time Spent in verification

ASIC: Percentage of Project Time Spent in Verification

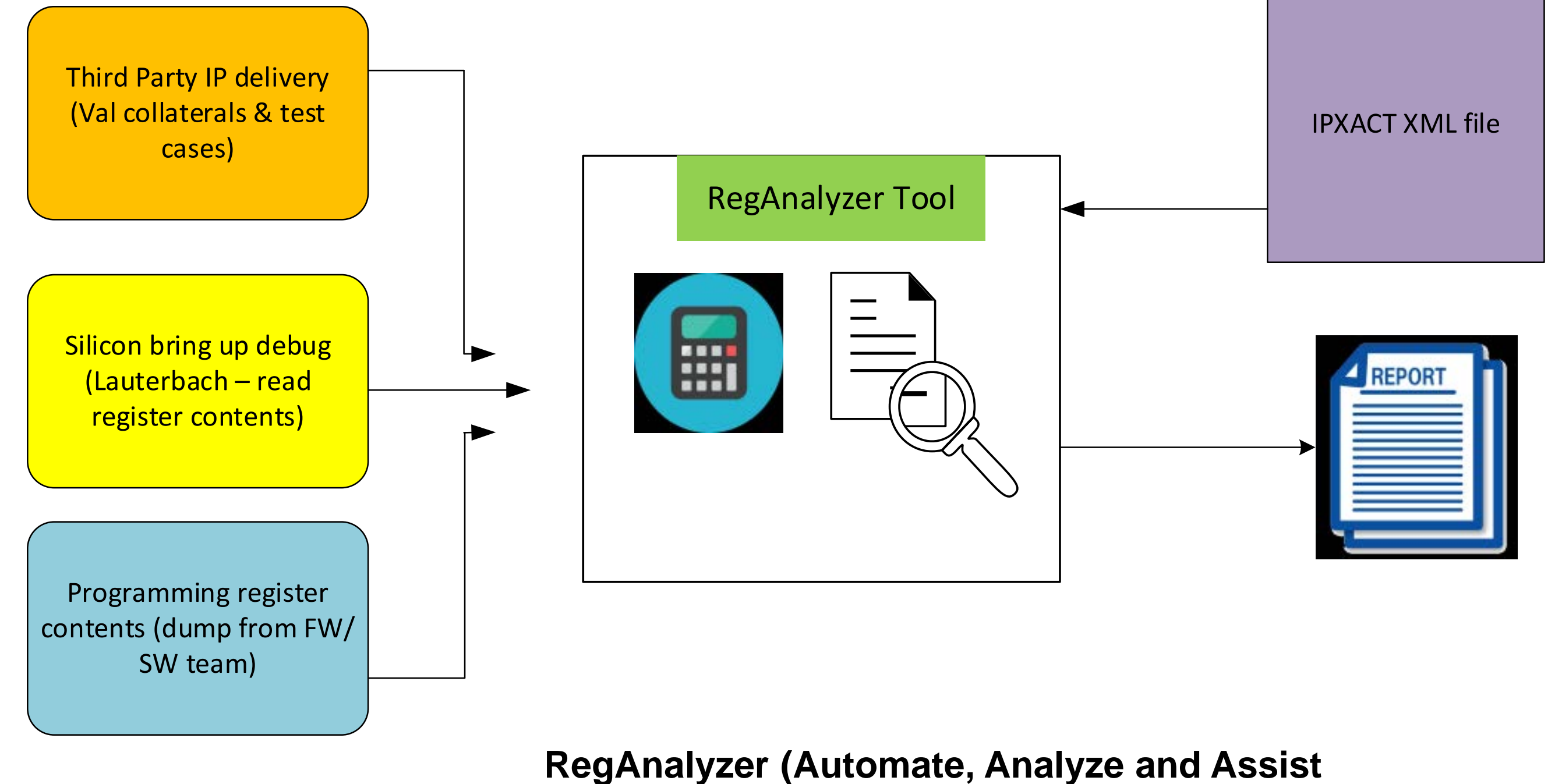
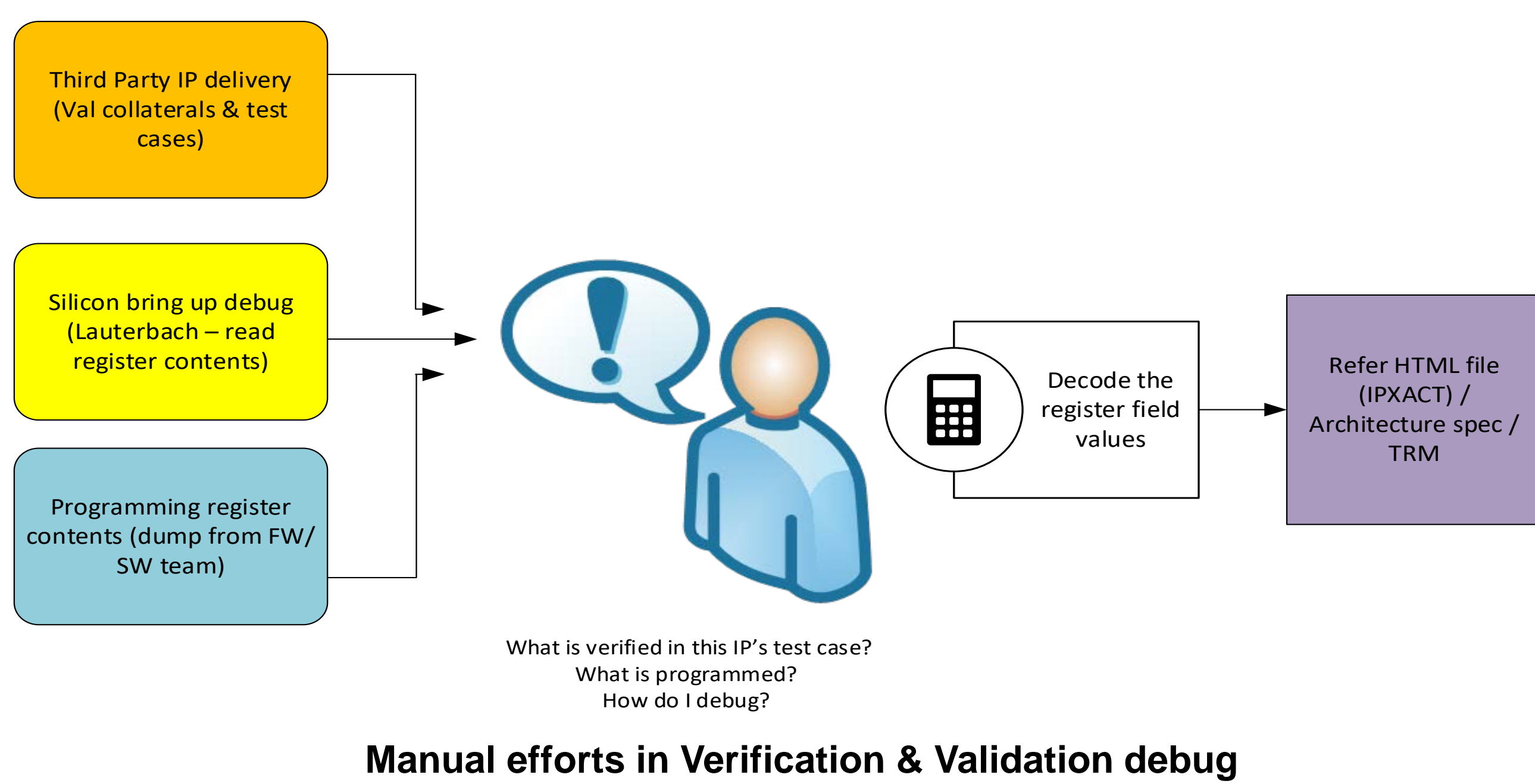


## Where IC/ASIC Verification Engineers Spend their Time

ASIC: Where Verification Engineers Spend Their Time



## Manual efforts -> Automation



## RegAnalyzer Tool

Register Name	Field Width	Reset Value	Actual Value	Register Field Description
DIP_ID	16	0x490008	0x713406	0x00000001. The identification register allows identify the module, the module version and the used configuration.
CONFID	16	0x713	0x0	bit 0 serial interface bit 1 parallel interface bit 2 RGB interface bit 3 MVI interface bit 4 MIPI DSI interface bit 5 TVout interface bit 6 reserved bit 7 Camera interface bit 8 Line/Rect command bit 9 Bitctrl/scroll/Move command bit 10 Bitctrl2 command bit 11 Triangle command bit 12 Rotate image command bit 13 Rotate image command bit 14 Update command bit 15 scheduling data/startup sequence: #703#
MOD_VERSION	16	0x4306	0x1	The first part (0x43) corresponds to module DCC. The second part is a version. 0x00 = XG213/618 HSI (1.4.0/2.0.0), 0x01 = XG213 HSI (2.5.0), 0x02 = XG618 HSI/Paracelus (2.9.0), 0x03 = XG223 (3.4.0), 0x04 = XG631, 0x5=XG632, 0x6=XG642
DIP_CON	0x4900020	0x00000000	0x35555555	The register is used for configuration of the display interfaces, especially the serial display interface. It contains a control field for all display interfaces with standard pads in case of tristate usage.
READ_CS2	1	0x0	0x1	If this bit is set and the corresponding bit in crossrefz is set then halfduplex reading will be performed during serial transmission.
READ_CS1	1	0x0	0x1	If this bit is set and the corresponding bit in crossrefz is set then halfduplex reading will be performed during serial transmission.
READ	5	0x0	0xa	
SM	5	0x0	0x15	
PO	1	0x0	0x1	
HS	1	0x0	0x1	
TSI	2	0x0	0x1	
DIP_VERSION	0x4900024	0x00000000	0x00002434	The register contains one hot coded bits to select the DIP module mode, i.e. serial.

## Test case / T32 output / Trace file which contains the register programming

```
WRITE_WORD(0x00000004, 0x00000000);
WRITE_WORD(0x00000008, 0x00000400);
WRITE_WORD(0x00000008, 0x00000400);
WRITE_WORD(0x00000008, 0x00000080);
WRITE_WORD(0x0000000c, 0x28004000);
```

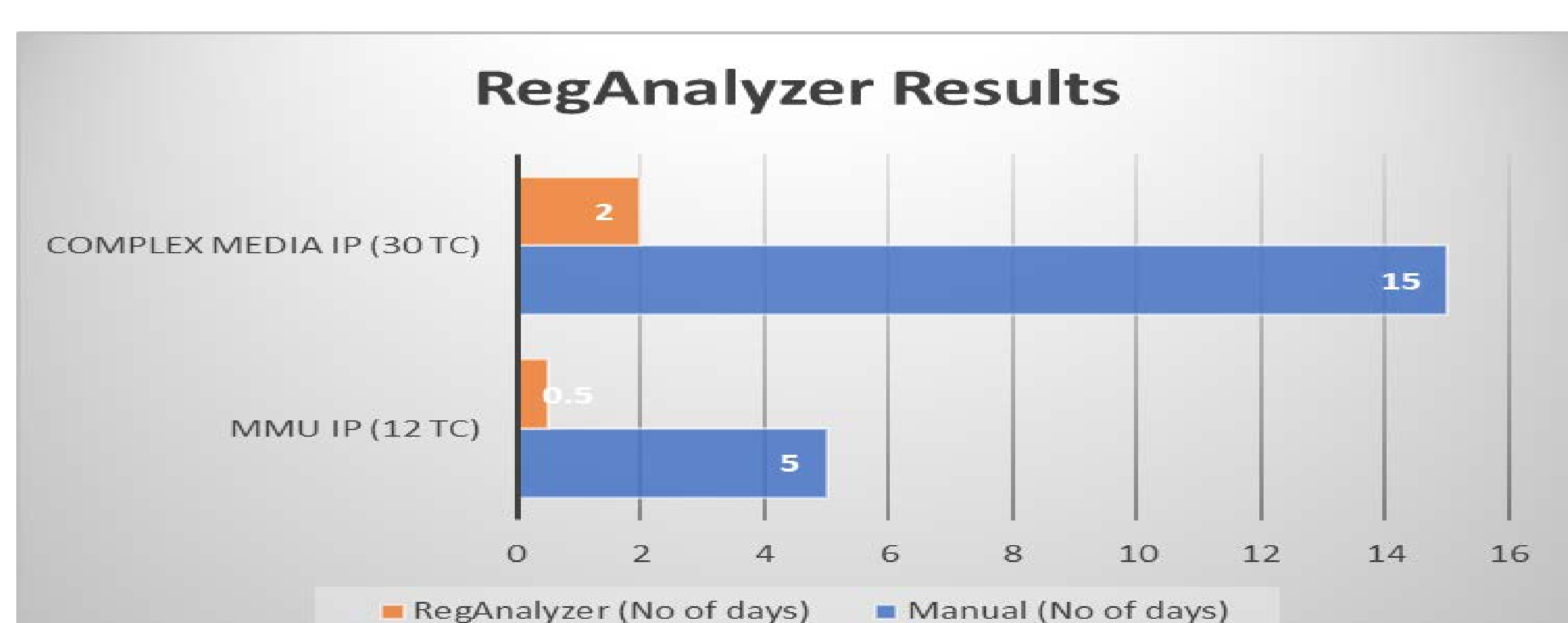
**B: Register view / SpotLight**

N	R0	08004E00	R8	0	S	Stack
2	R1	08004DF8	R9	0		
C	R2	08004DF0	R10	0		
V	R3	0	R11	0		
W	R4	08004E00	R12	0		
B	R5	0	R13	20002410		
0	R6	0	MEM	00000000		
0	R7	0	PC	0800472C		
2	CONTROL	0	XPSR	01000000		

**B: Data dump r(013) / DIALOG**

address	0	4	01234567
SD:20002410	08004DF8	FFFFFFFF	FFFFFFFF
SD:20002418	00000000	00000000	00000000
SD:20002420	20001400	08004DF0	00000000
SD:20002428	08004DF8	00000000	00000000
SD:20002430	00000000	08004E00	00000000
SD:20002438	00000000	00000000	00000000
SD:20002440	00000000	00000000	00000000

## Results



## Conclusion

RegAnalyzer is an effective GUI tool which will help in day-to-day verification activities, reduce the manual efforts drastically and save debug time. This tool will help during the design pre-silicon verification and post silicon validation to understand the register programming and its details. By using all the different features supported by this tool, verification and validation Engineers can make tremendous progress and reduce the overall debug time during Silicon-On-Chip development.