RegAnalyzer -A tool for programming analysis and debug for verification and validation

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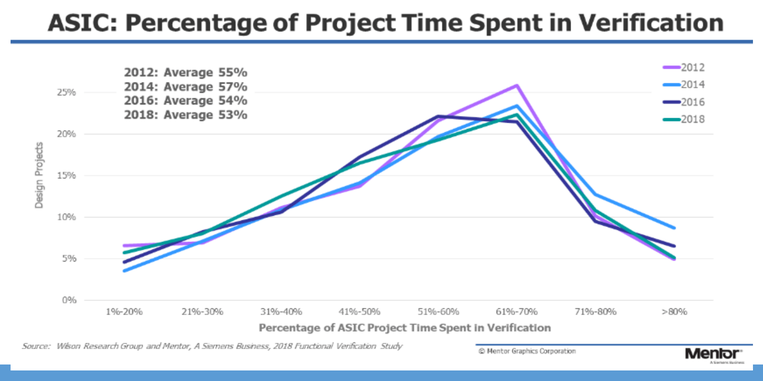
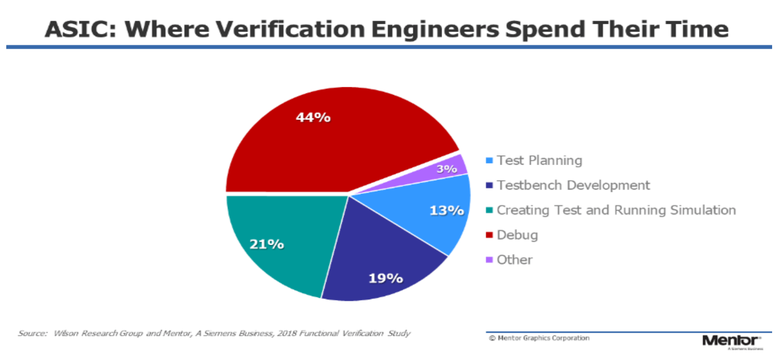
Abstract

As the technology node is shrinking, more and more IPs are getting integrated in single System-on-chip. In the System-on-chip, verification is getting more tedious, time consuming and challenging task. Based on case study on different internal and third-party IP's, realized that there are no mechanism nor internal / external tools available for doing the quick debug by understanding the test cases and its programming. Verification Engineers are putting manual effort to understand the IP programming in the test cases and there is no direct way to map the register programming to the Technical Reference Manual / Programmers model. This poster presents a tool RegAnalyzer which resolves this problem.

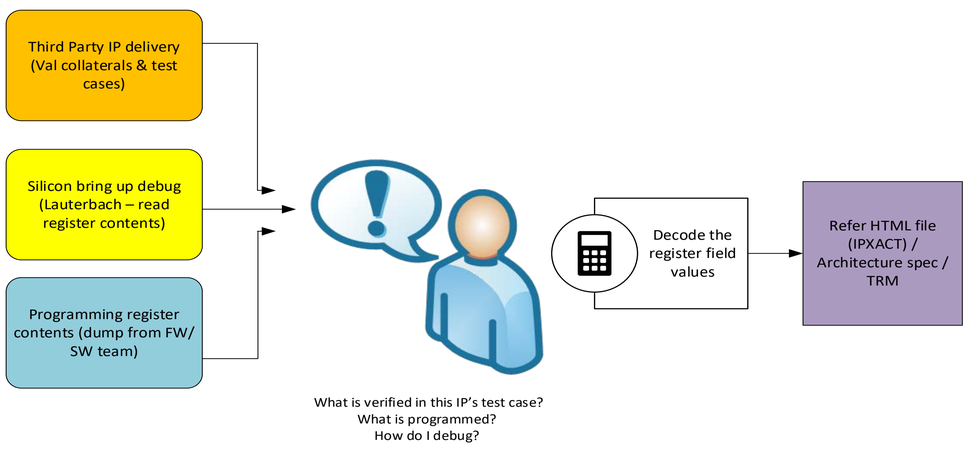
Percentage of IC/ASIC Project Time Spent in verification



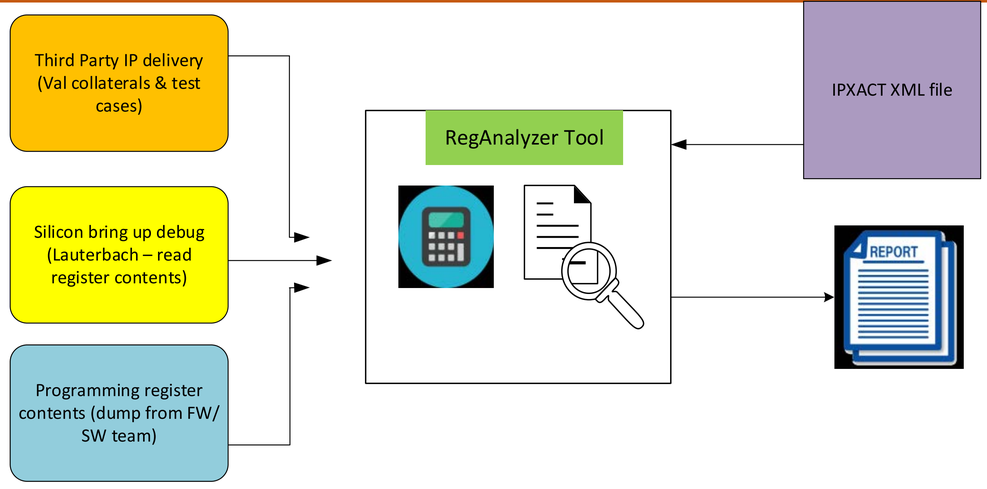
Where IC/ASIC Verification Engineers Spend their Time



Manual efforts -> Automation

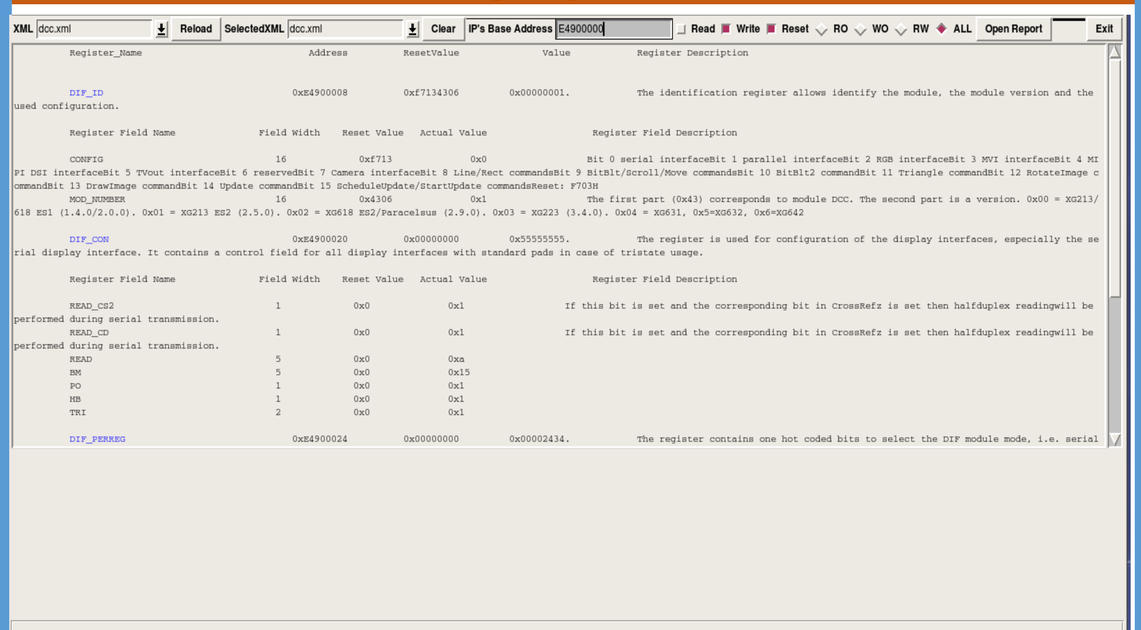


Manual efforts in Verification & Validation debug



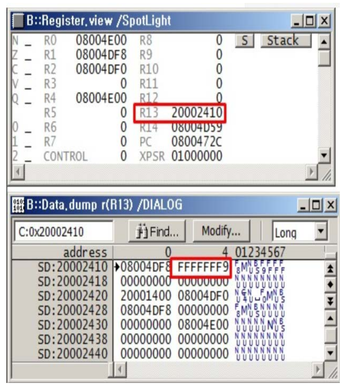
RegAnalyzer (Automate, Analyze and Assist

RegAnalyzer Tool



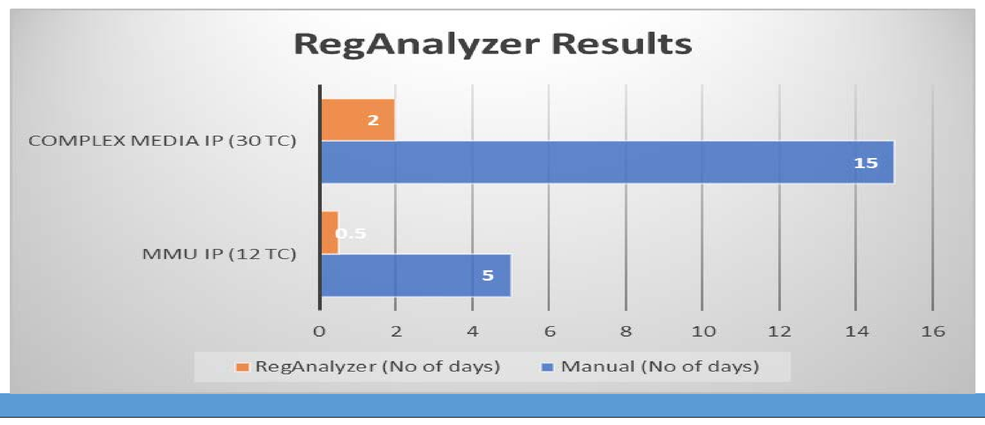
Test case / T32 output / Trace file which contains the register programming

```
WRITE_WORD(0x00000004 , 0x00000000);
WRITE_WORD(0x00000008 , 0x00000400);
WRITE_WORD(0x00000008 , 0x00000400 );
WRITE_WORD(0x00000008 , 0x00000080);
WRITE_WORD(0x0000000c , 0x28004000);
```




```
W 0000000c/1800C000
W 00000010/01600900
W 00000014/10001A7C
W 00000018/0001A141
W 0000001c/0000003F
W 00000020/00000000
W 00000024/00000000
W 00000028/00000000
W 0000002c/00000000
W 00000030/00000000
W 00000034/00000000
W 00000038/00000000
W 0000003c/00000000
W 00000040/02031890
W 00000044/05050304
W 00000048/00000404
W 0000004c/10907D01
W 00000050/04030404
W 00000054/04040507
W 00000058/77020100
W 0000005c/11111510
W 00000060/00000001
W 00000064/11111130
W 00000068/00000111
```

Results



Conclusion

RegAnalyzer is an effective GUI tool which will help in day-to-day verification activities, reduce the manual efforts drastically and save debug time. This tool will help during the design pre-silicon verification and post silicon validation to understand the register programming and its details. By using all the different features supported by this tool, verification and validation Engineers can make tremendous progress and reduce the overall debug time during Silicon-On-Chip development.