2017 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

Real Number Modeling for RF Circuits

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ANALOG DEVICES

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Outline

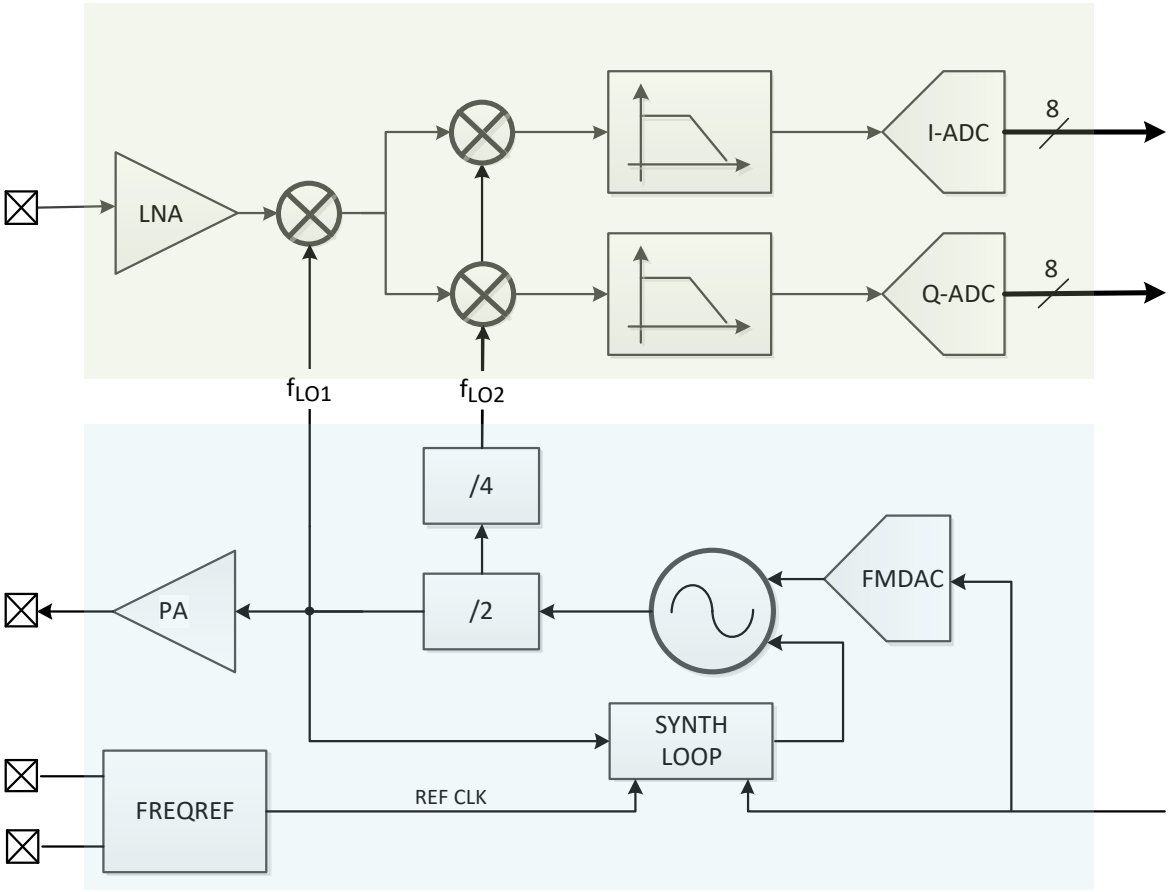
- Motivation
- TX Path Models
- RX Path Models
- Performance
- Validation
- Conclusion

Motivation

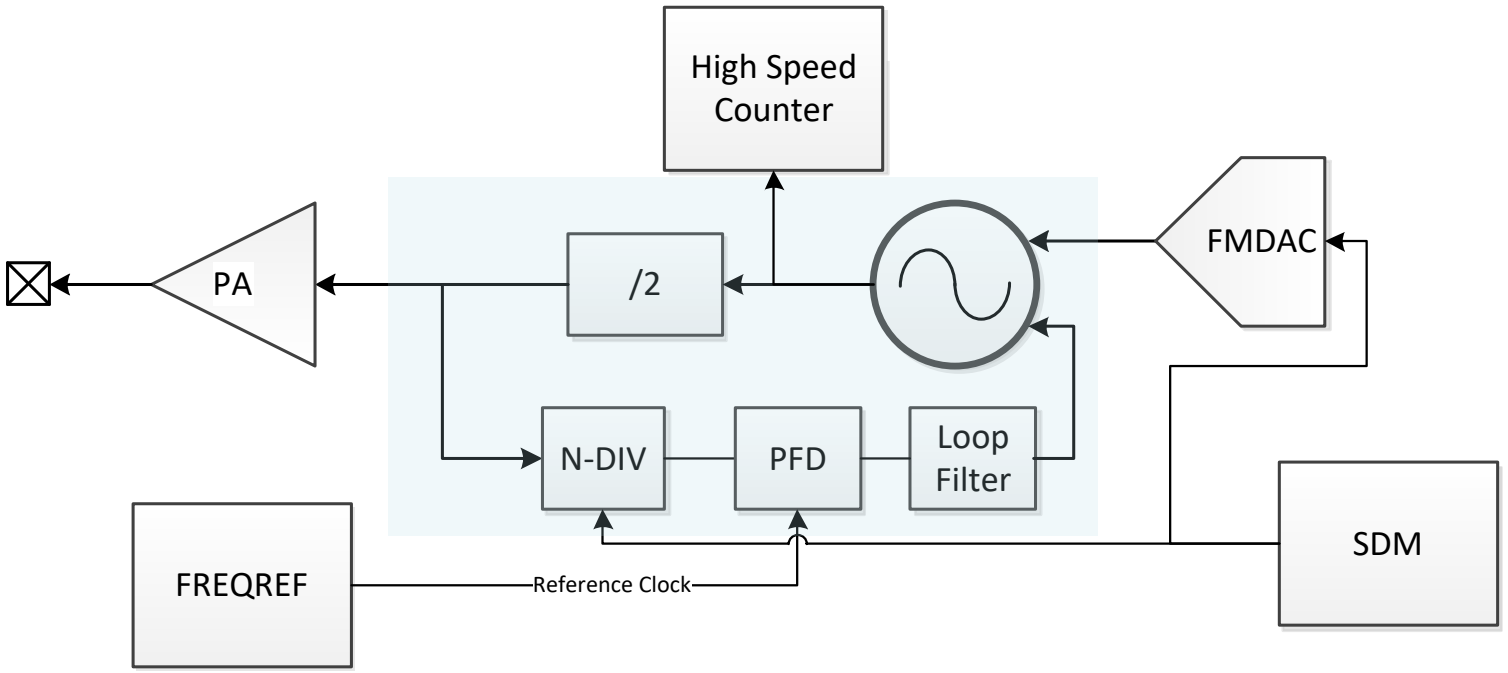
Full chip model of a RF SoC

- Test case development and debug
- Horizontal re-use: Eval (PSS!)
- Firmware development and debug
- Not suited for:
  - RF performance (noise, linearity, etc…)
  - Analog performance (current draw, brown outs, etc…)

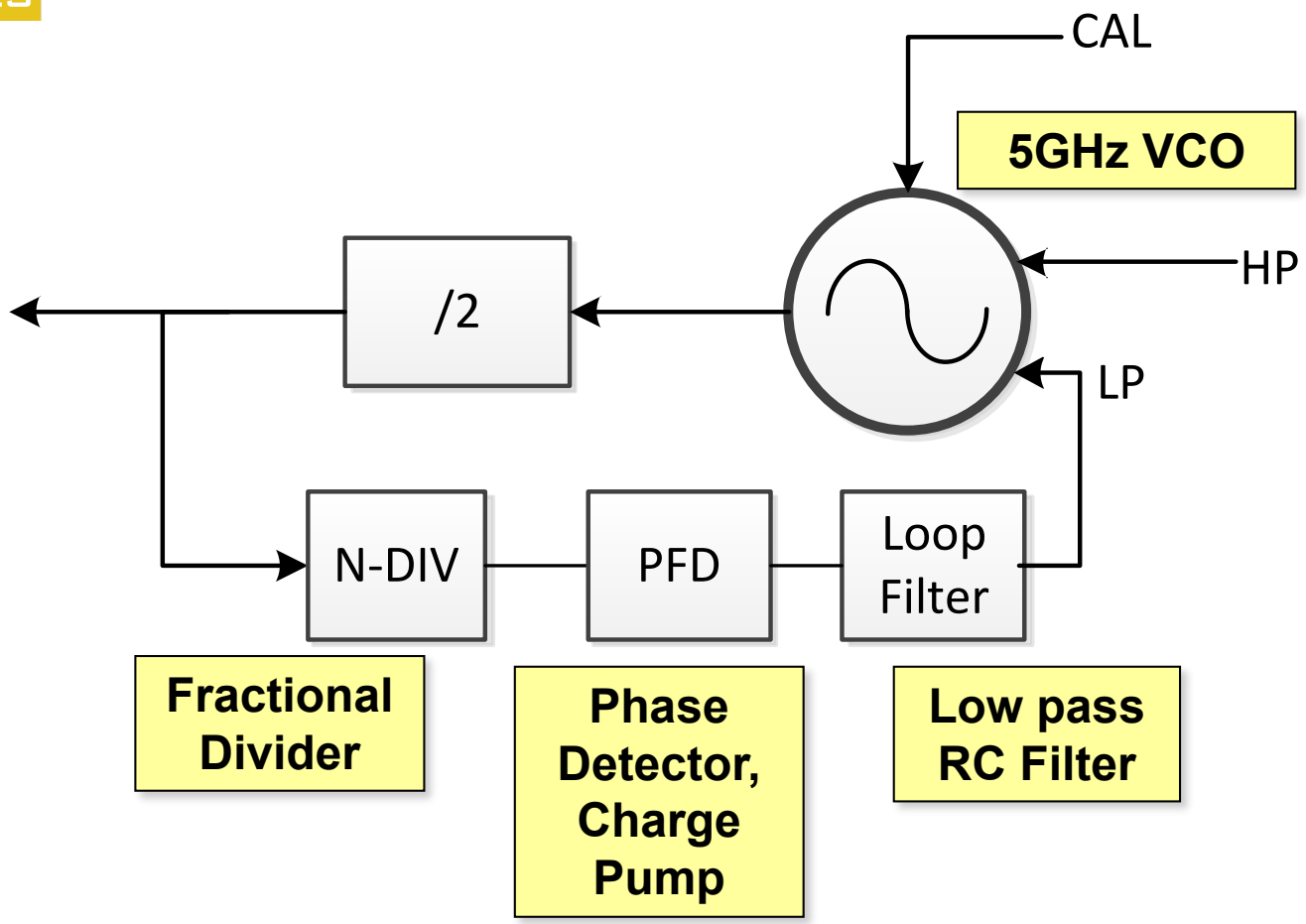
RF Front End


LNA
I-ADC
8
Q-ADC
8
f_{LO1}
f_{LO2}
/4
/2
PA
FMDAC
SYNTH
LOOP
FREQREF
REF CLK

TX Path

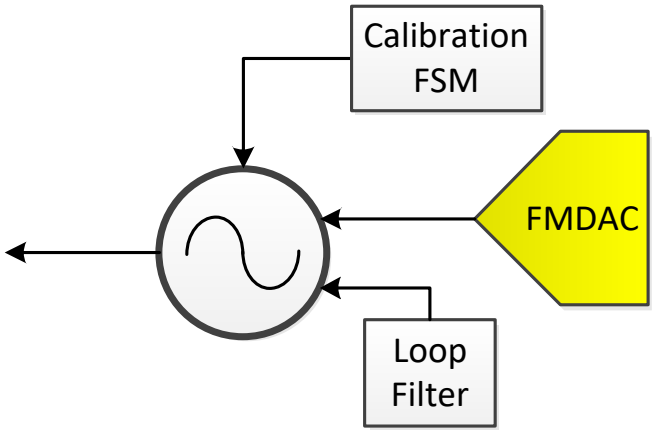

High Speed Counter
PA
/2
FMDAC
N-DIV
PFD
Loop Filter
SDM
FREQREF
Reference Clock

PLL


CAL
5GHz VCO
HP
LP
/2
N-DIV
PFD
Loop Filter
Fractional Divider
Phase Detector, Charge Pump
Low pass RC Filter

VCO

- VCO inputs:
  - loop filter port
  - modulation port
  - calibration codes

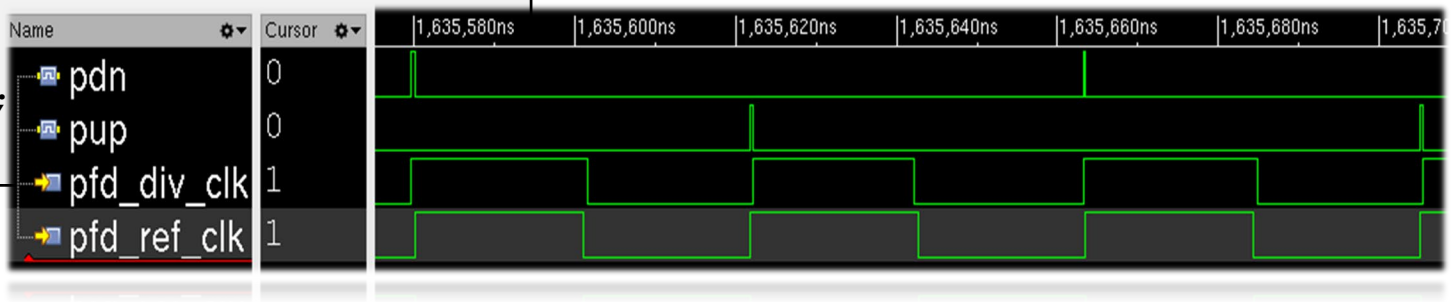



```
assign f_vco = fc + kv_lp * (vtune_lp-0.6) +
                    kv_hp * (vtune_hp_p-vtune_hp_m);
assign hperiod = (1s/f_vco)/2.0;

always begin
  wait(pwr_ok);
  #hperiod vco = !vco & pwr_ok;
end
```

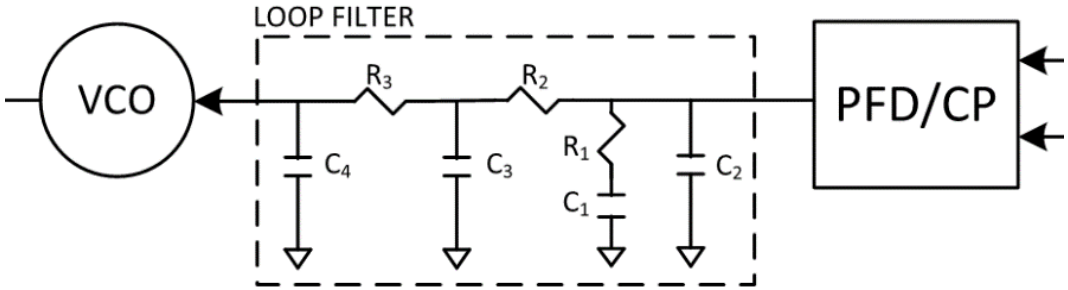
Phase Detector/Charge Pump

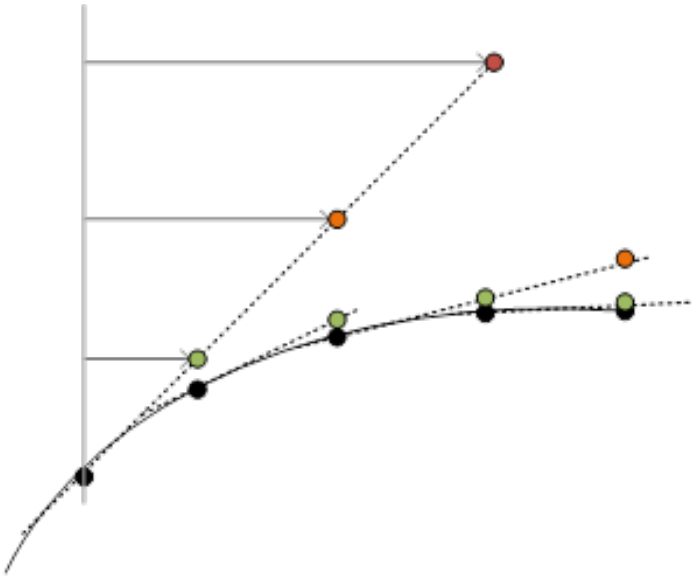
```
always @(posedge ref_clk or negedge rst)
begin
  if(!rst) begin
    pup = 1'b0;
  end else if(pdown) begin
    pdown <= 1'b0;
  end else begin
    pup <= 1'b1;
  end
end

always @(posedge div_clk or negedge rst)
begin
  if(!rst) begin
    pdown = 1'b0;
  end else if(pup) begin
    pup <= 1'b0;
  end else begin
    pdown <= 1'b1;
end
```

```
always @(posedge pup)
  pup_time = $realtime;

always @(posedge pdown)
  pdn_time = $realtime;

always @(negedge pup)
  filter(($realtime-pup_time)*Icp);

always @(negedge pdown)
  filter((pdn_time-$realtime)*Icp);
```



Loop Filter





```
t /= 1s;

// sanity check
t = min(t, +Txtal);
t = max(t, -Txtal);

// integrate charge pump
// current onto C2
Vc2 += Qin/C2;

// compute currents, I=V/R
Ir1 = (Vc2-Vc1)/R1;
Ir2 = (Vc2-Vc3)/R2;
Ir3 = (Vc3-Vc4)/R3;

// compute voltages: V=I*t/C
Vc1 += Ir1*Txtal/C1;
Vc2 -= (Ir1+Ir2)*Txtal/C2;
Vc3 += (Ir2-Ir3)*Txtal/C3;
Vc4 += Ir3*Txtal/C4;

Vc2 = min(Vc2, Vdd);
Vc2 = max(Vc2, 0);
```

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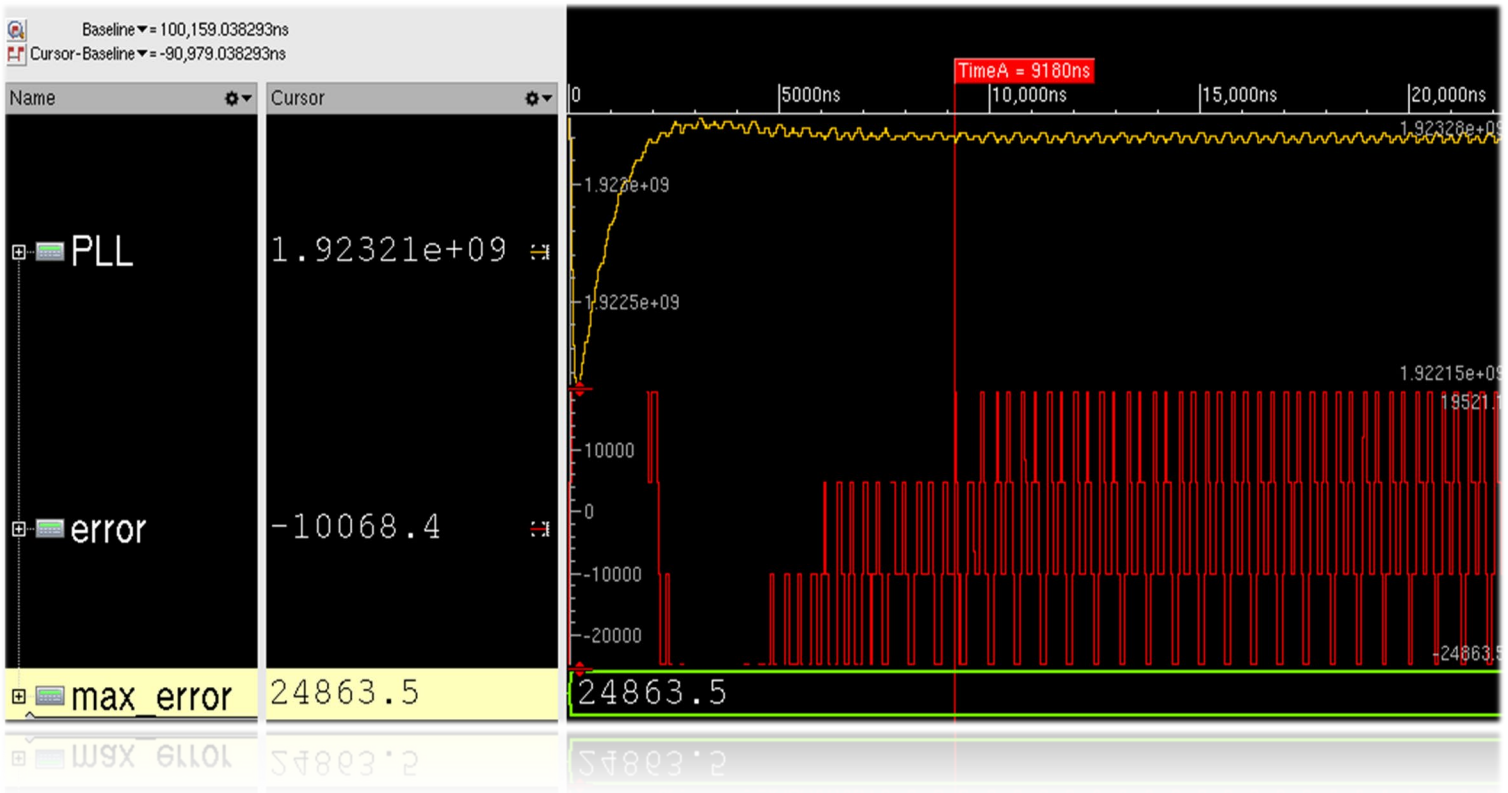
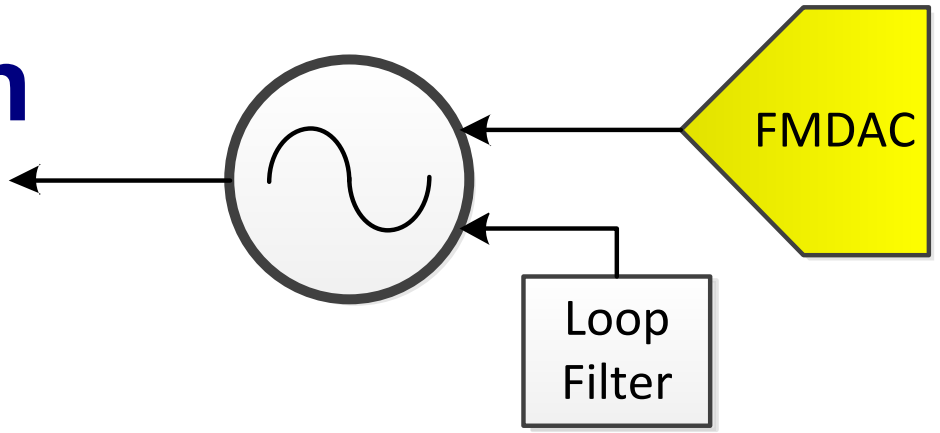
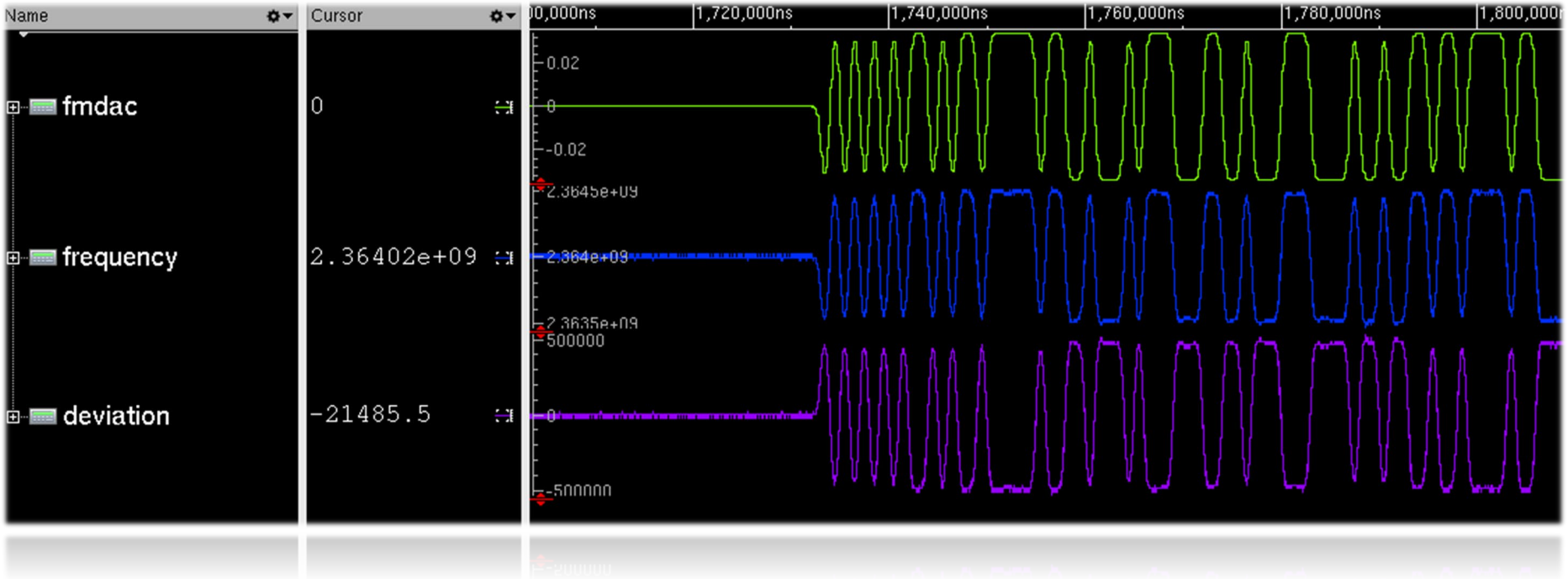
Lock example

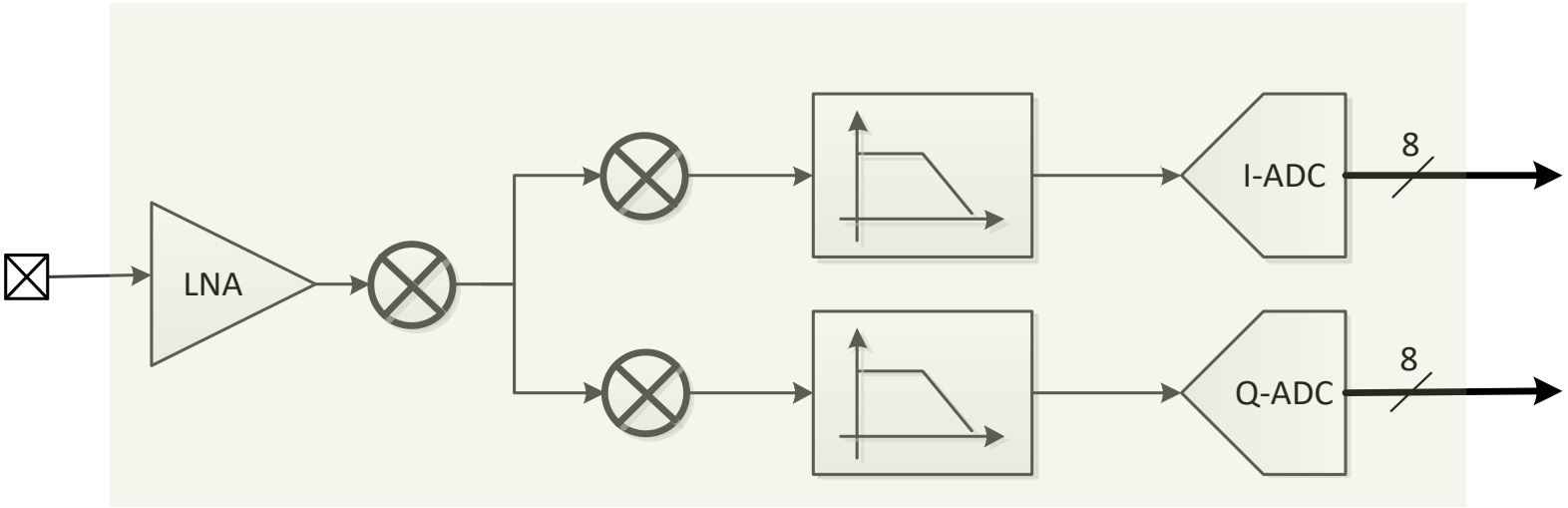


Modulation


FMDAC
Loop
Filter

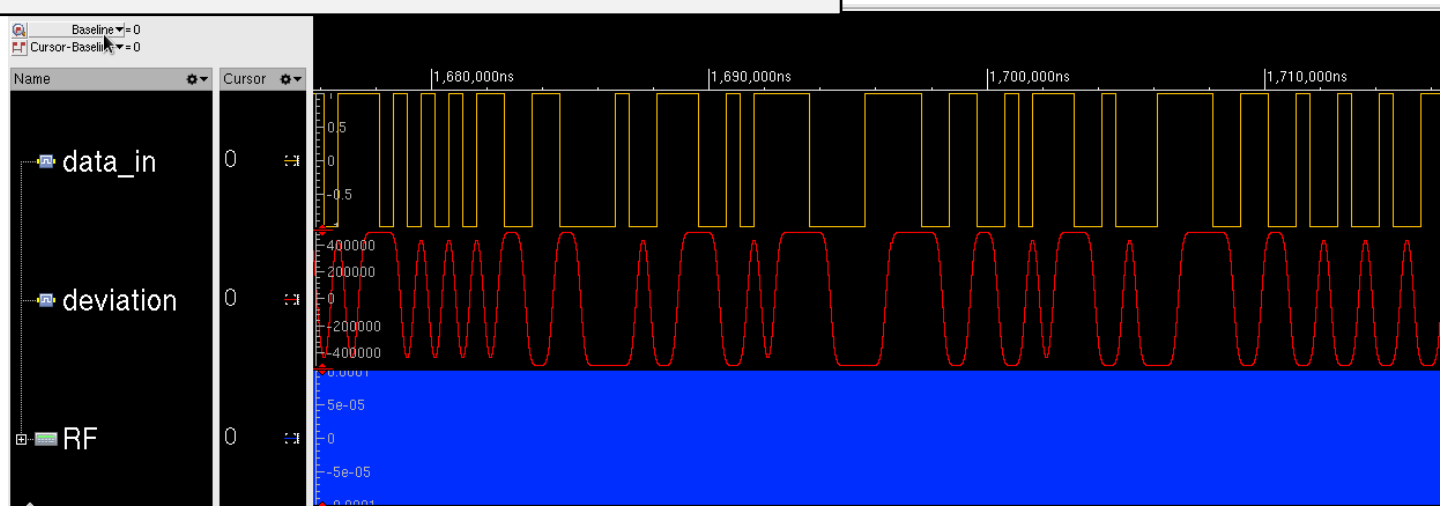

Name
Cursor
fmdac
0
frequency
2.36402e+09
deviation
-21485.5
1,720,000ns
1,740,000ns
1,760,000ns
1,780,000ns
0.02
-0.02
500000

RX Path



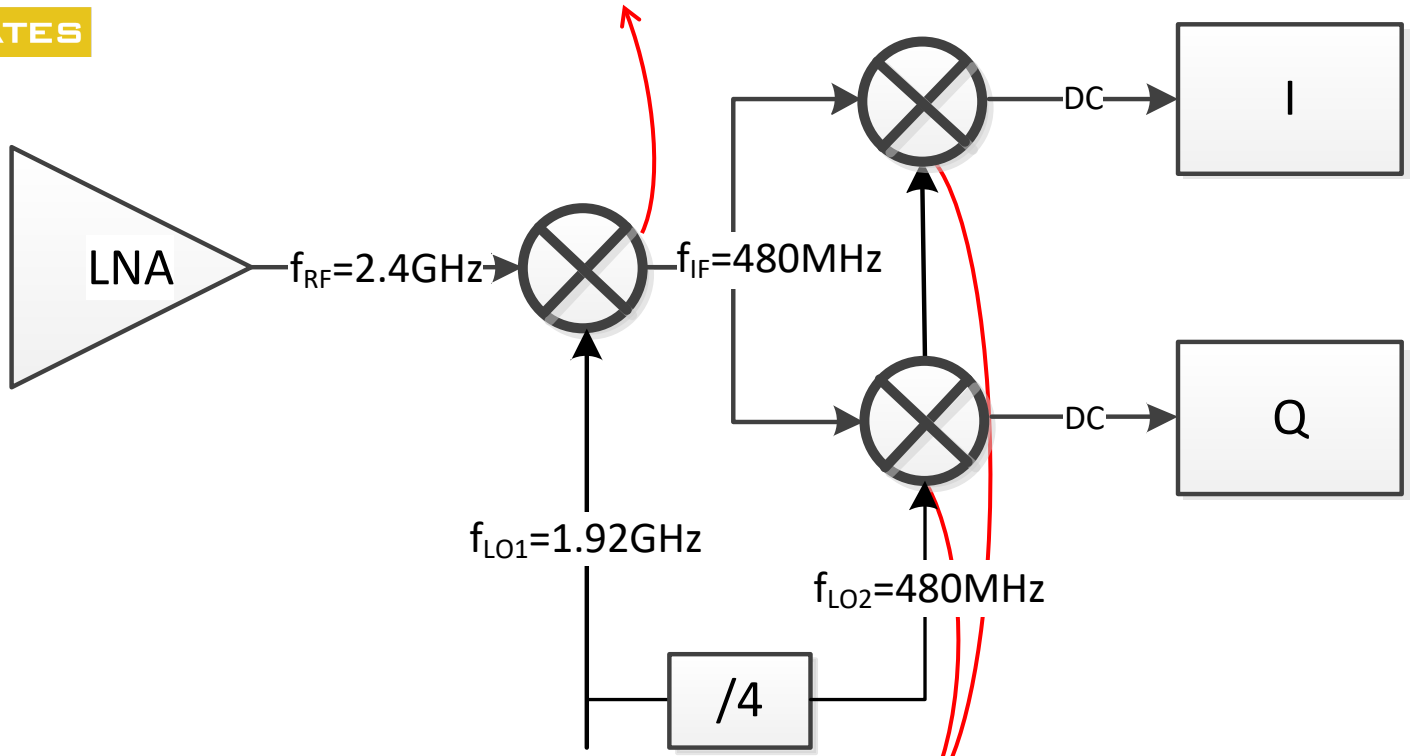
RF Stimulus

```
rf_tstep = 1/((fc+f_err+fdev+fdrift)/2);
task gen_rf;
  forever begin
    wait(rf_tstep > 0);
    #(rf_tstep *1s);
    vif.rf_r = (vif.rf_r<0) ? amp:-amp;
  end
endtask
```

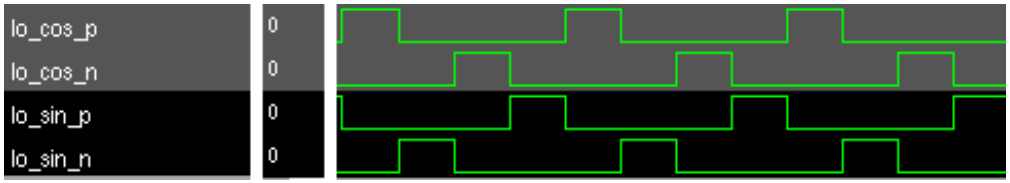


Mixer

```
assign i_f = lo ? r_f : -r_f;
```

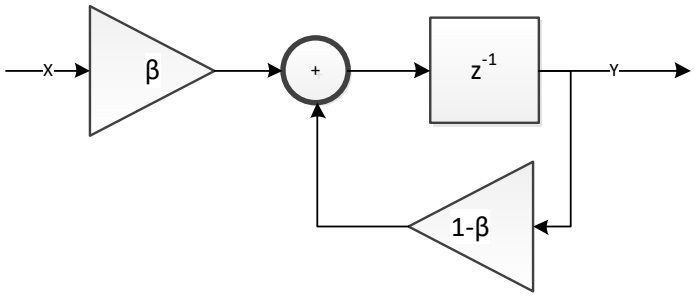



```
assign I = lo_cos_p ? +i_f : lo_cos_n ? -i_f : 0;
assign Q = lo_sin_p ? +i_f : lo_sin_n ? -i_f : 0;
```



Mixer Bandwidth

- Specification
  - RF mixer: 1st order cutoff at 1GHz
  - IF mixer: 1st order cutoff at 10MHz

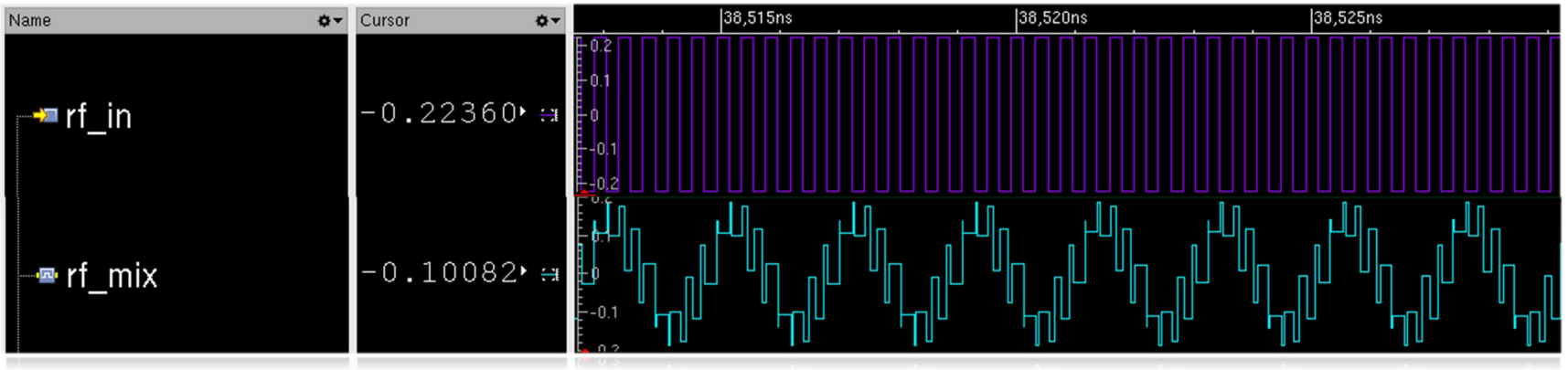


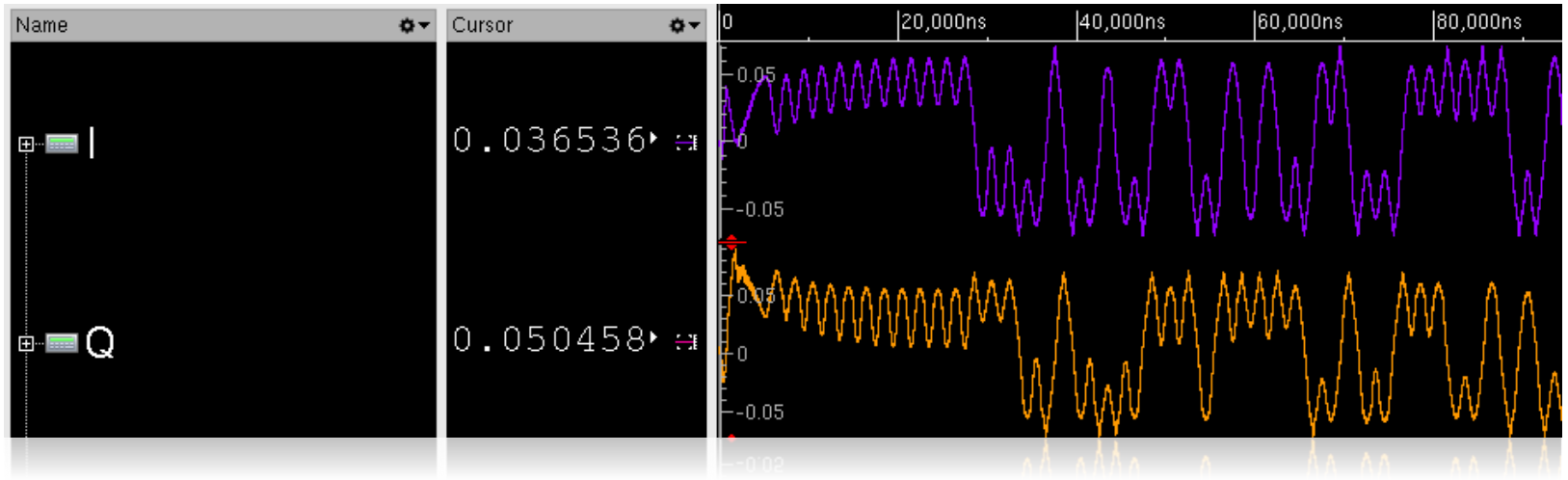
$$\omega_c = 2\pi \frac{f_c}{f_s} = 2\pi f_c T_s$$

$$\beta = -1 + cos(\omega_c) + \sqrt{(cos(\omega_c) - 3)(cos(\omega_c) - 1)}$$

$$\beta \cong \omega_c \; for \; f_c \ll f_s$$

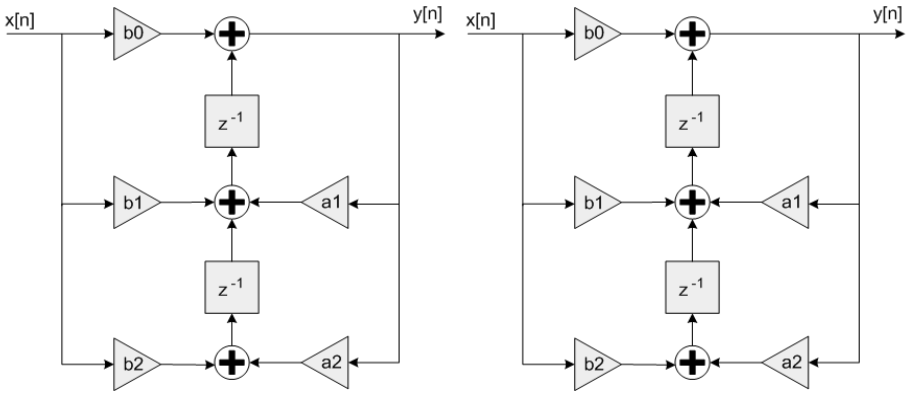
Mixer Bandwidth





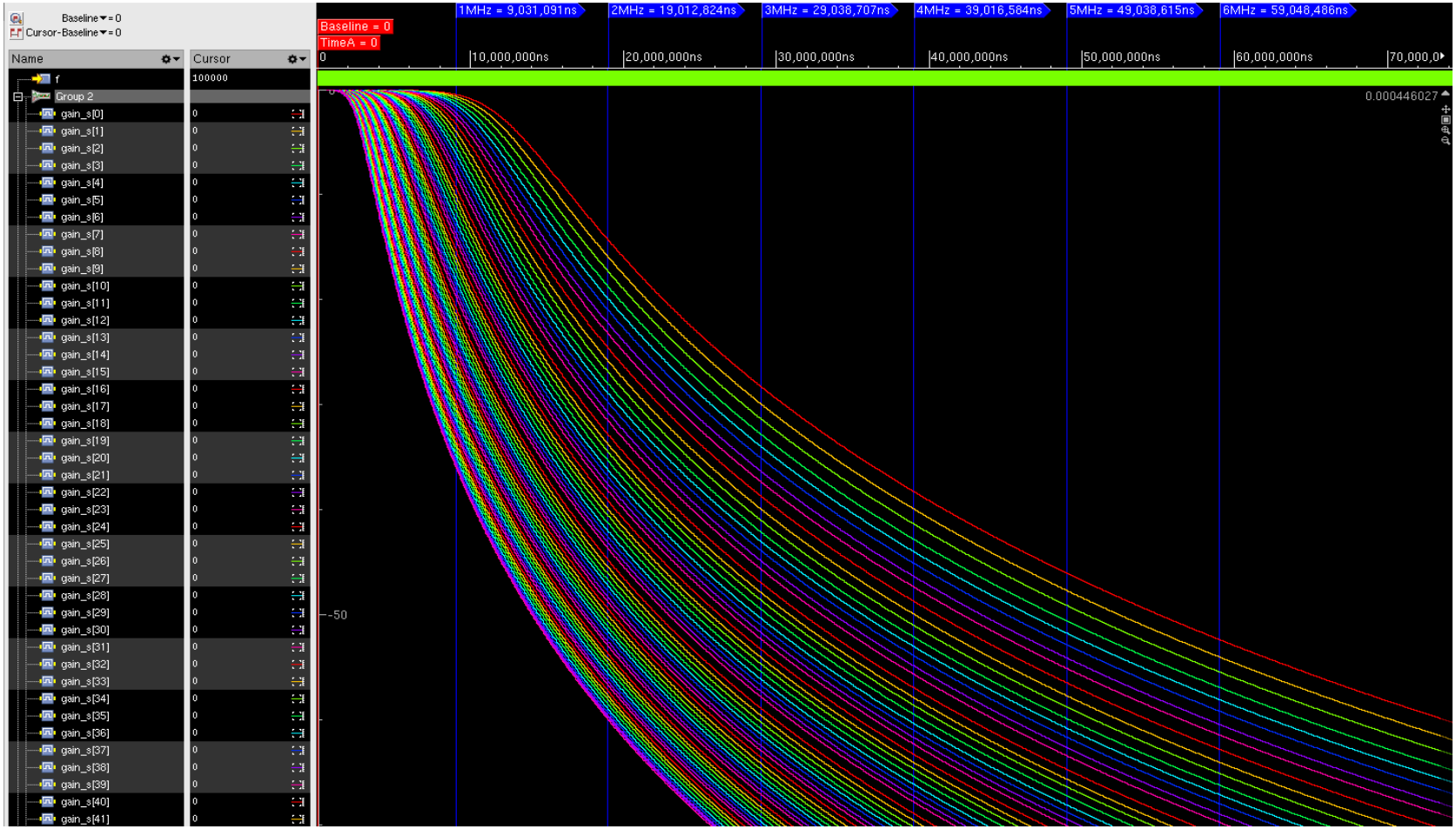
Baseband Filter

- BBF synthesized using bilinear transform
- Matlab function:
  - butter() => Butterworth filter
  - tf2sos() => biquads




```
// first biquad
always@(posedge clk) begin
    x01 <= in0*b01 - out0*a01 + x02;
    x02 <= in0*b02 - out0*a02;
end

always@(x01)
  out0 = (in0*b00+x01);n
assign in1 = out0;

// second biquad
always@(posedge clk) begin
    x11 <= in1*b11 - out1*a11 + x12;
    x12 <= in1*b12 - out1*a12;
end

always@(x11)
  out1 = (in1*b10+x11);

assign out = g*out1;
```

Baseband Filter Performance

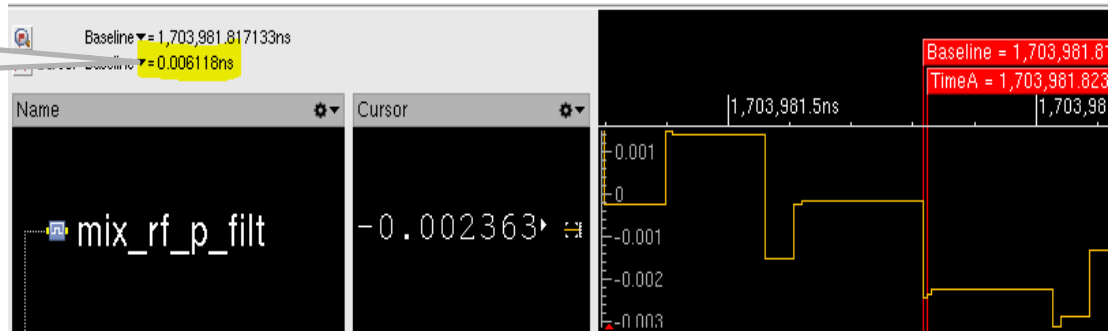


BBF Sampling Rate

Non uniform sampling at output of mixer

Some very high frequency components

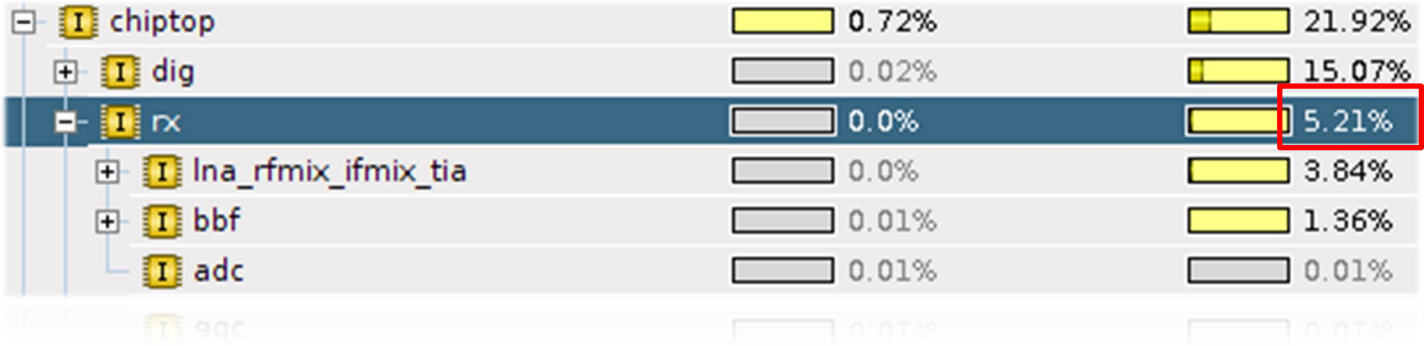
163GHz!



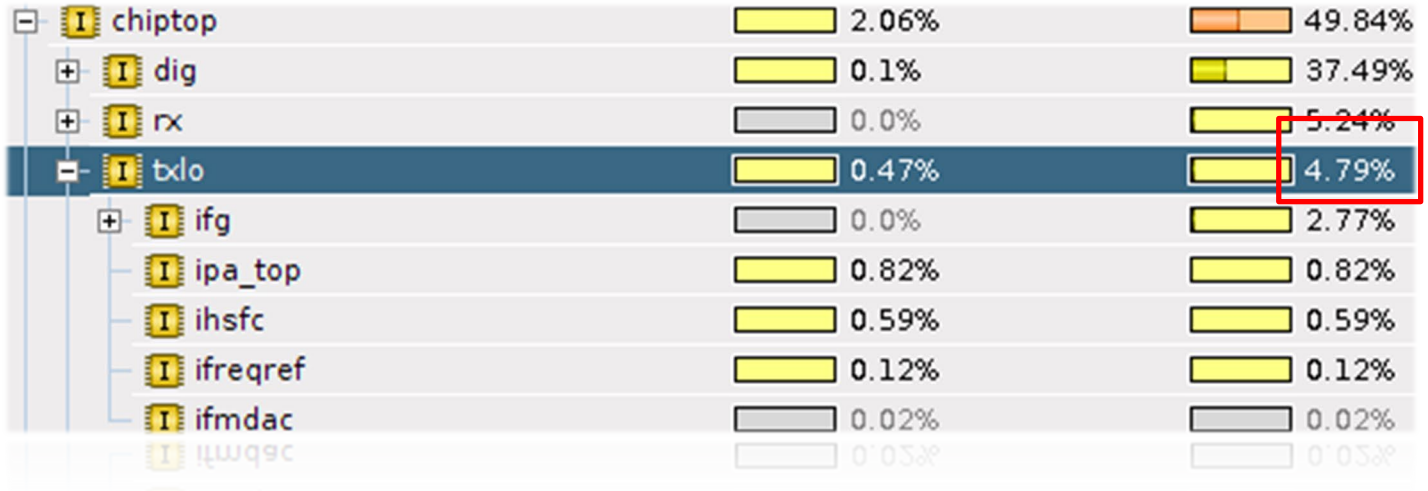
- Higher BBF sampling rate
  - better accuracy
  - precision loss in coefficients
  - slower simulation

Simulation Performance

RX

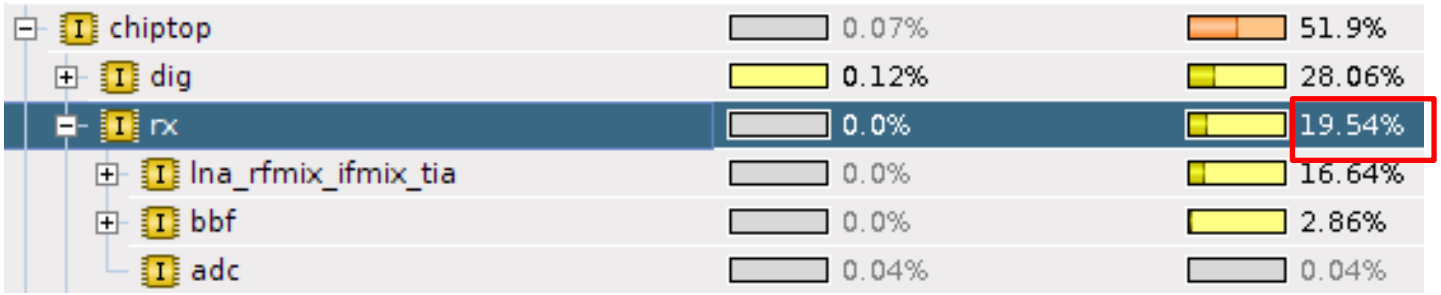


TX

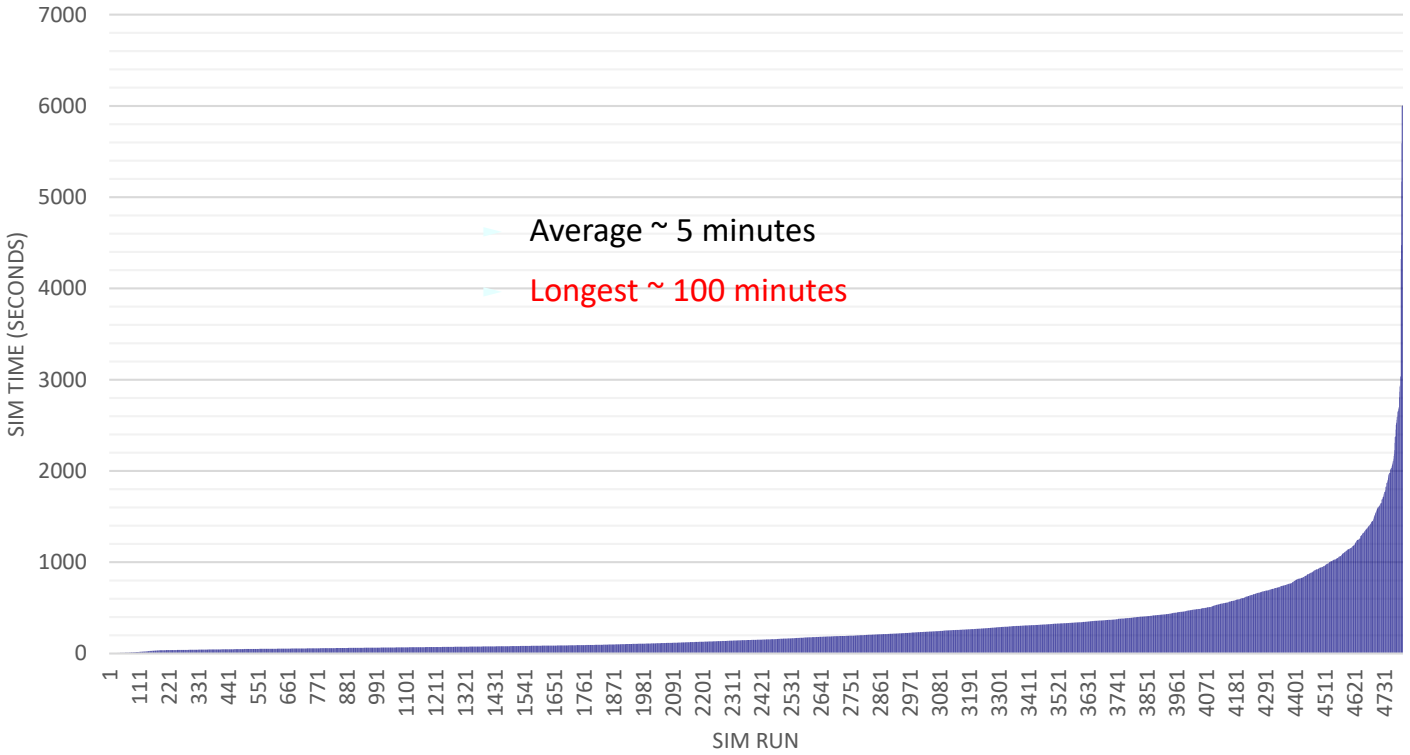


Simulation Performance

RX



Simulation Performance



Model Validation

- Model validation relies on performance measurement:
  - No signal comparison
  - Evaluation of system metrics
- Examples:
  - BBF frequency response
  - PLL lock time and frequency error
  - Spectral analysis of mixer outputs
  - etc…

Conclusion

- High Frequency Digital models are achievable with reasonable degree of performance.
- Complex circuits such as PLLs and mixers can be realized in the time domain with accuracy.
- Models enable
  - fast test development
  - use of randomization at system level
  - re-use across disciplines
- Limitation exists but are not detrimental to functional verification and coverage

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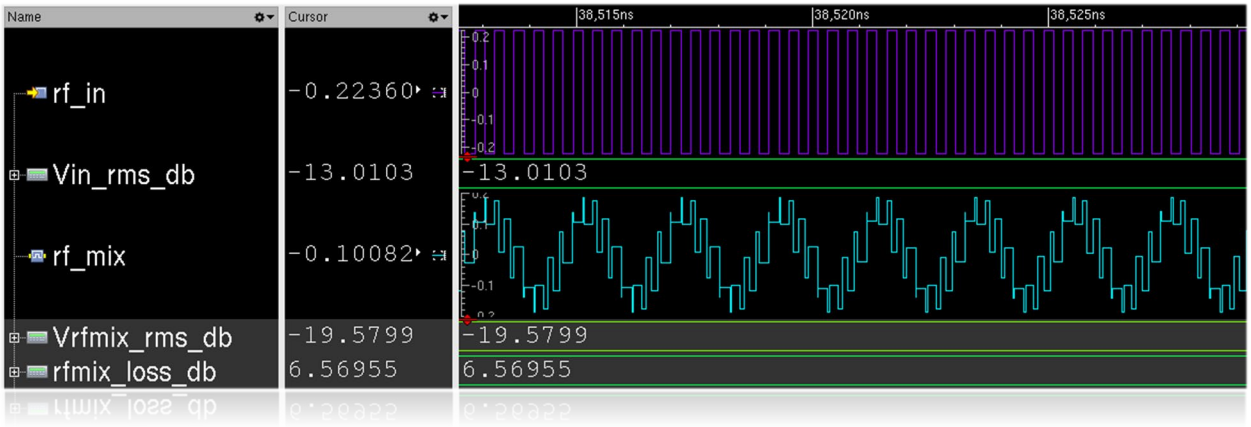
APPENDIX

Mixer Gain

- Mixer has an intrinsic gain
  - ½ gain for filtered f1+f2 component
  - fundamental frequency of square wave 4/pi
  - filter droop at f1-f2 around 0.8dB
  - Some of f1+f2 power to remain due to 1st order attenuation
  - Expect a loss around 7dB (observer 6.56dB)



Mixer Gain

- Mixer has an intrinsic gain
  - ½ gain for filtered f1+f2 component
  - Some of f1+f2 power to remain due to 1st order attenuation
  - Expect a loss <6dB (observed 4.5dB)