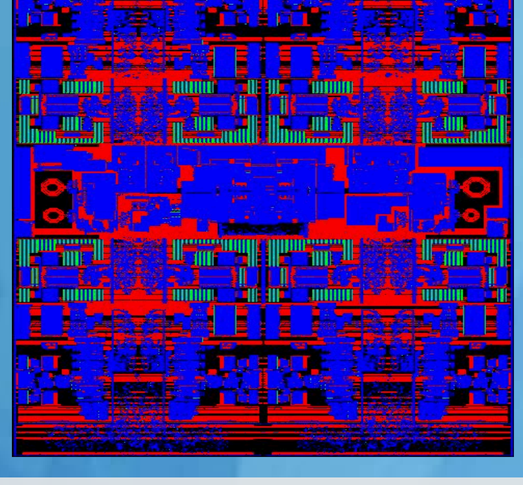
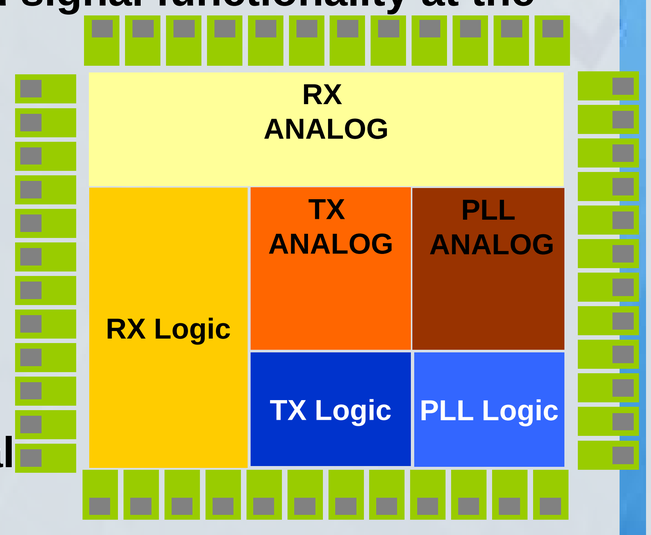
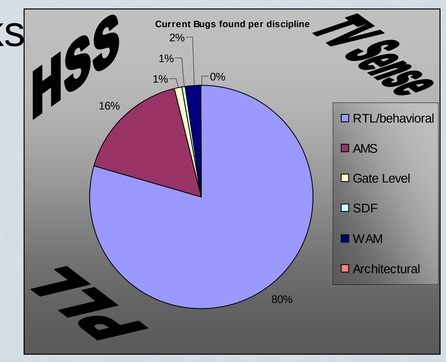


Real Number Modeling Enables Fast, Accurate Functional Verification

The Challenge

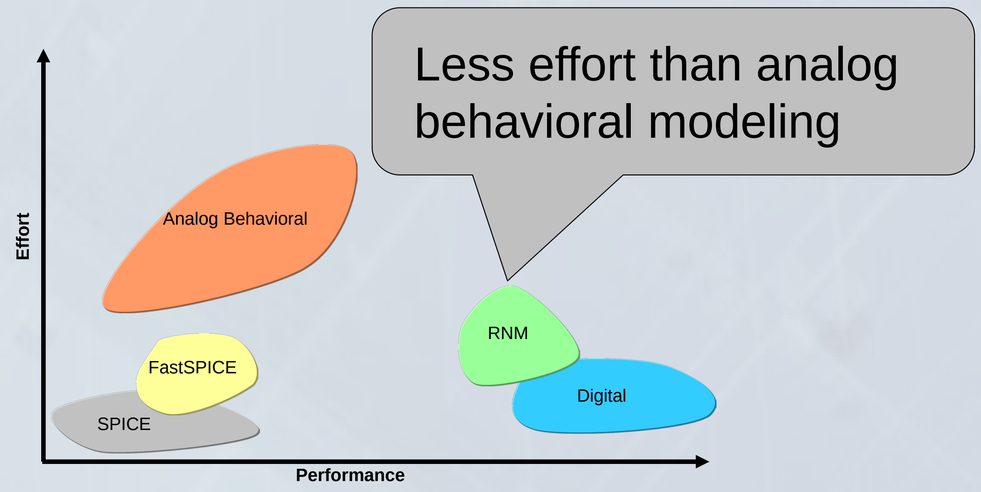
- **Making people believe**
- **Mixed signal functional verification required slow, detailed Verilog-A models**
- **Simulation of mixed signal functionality at the chip-level**
- **High-volume product**
- Functional failures would lead to **costly design iterations**
- **Digital abstracted behavioral** of analog blocks n**ot sufficient** for verifying mixed signal sub blocks





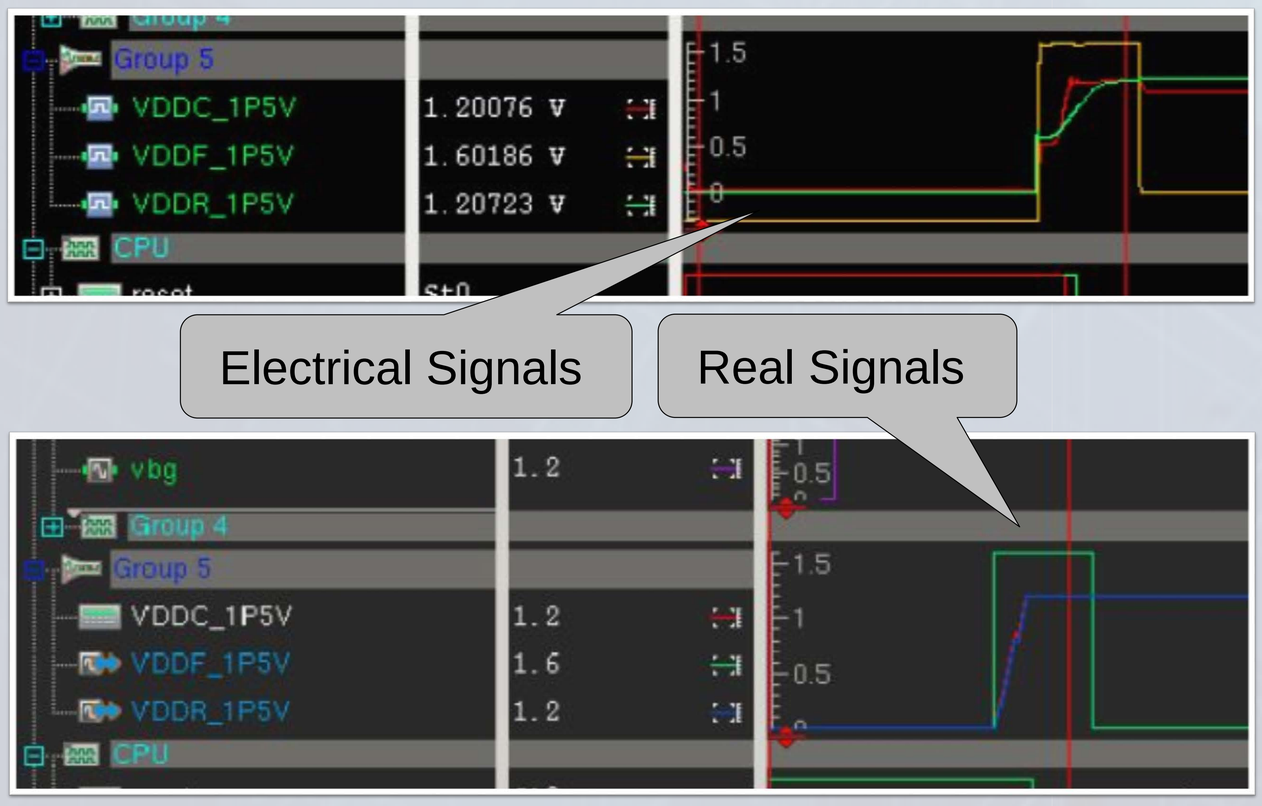
The Solution

- Use **Digital Mixed Signal (DMS)** verification strategy
- **Real Number Modeling**
- Model fidelity checking
- Analog assertions



Cultural Change

- AMS/DMS modeling required analog designers to work with digital verification engineers
- Management helped drive cultural change
- Required specific collaboration across the analog and digital teams to drive faster verification closure



~40X Faster

Results

- Achieved **~40x faster verification** compared to mixed-signal electrical modeling (va)
- **Improved product quality** with mixed-signal regression runs to ensure SoC met spec
- **Reduced re-spins** with high-performance, real-number modeling and top-level SoC verification
- Found and **fixed errors early** in the design cycle, which previously would have been found in hardware and would have caused project delays or even re-spins
- **10x cycle-time improvement** in mixed-signal verification

IBM ←**Wes Queen, Tom Cole**

Dan Romaine→ cadence™