2019 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

Product Life Cycle of Interconnect Bus: A Portable Stimulus Methodology for Performance Modeling, Design Verification, and Post-Silicon Validation

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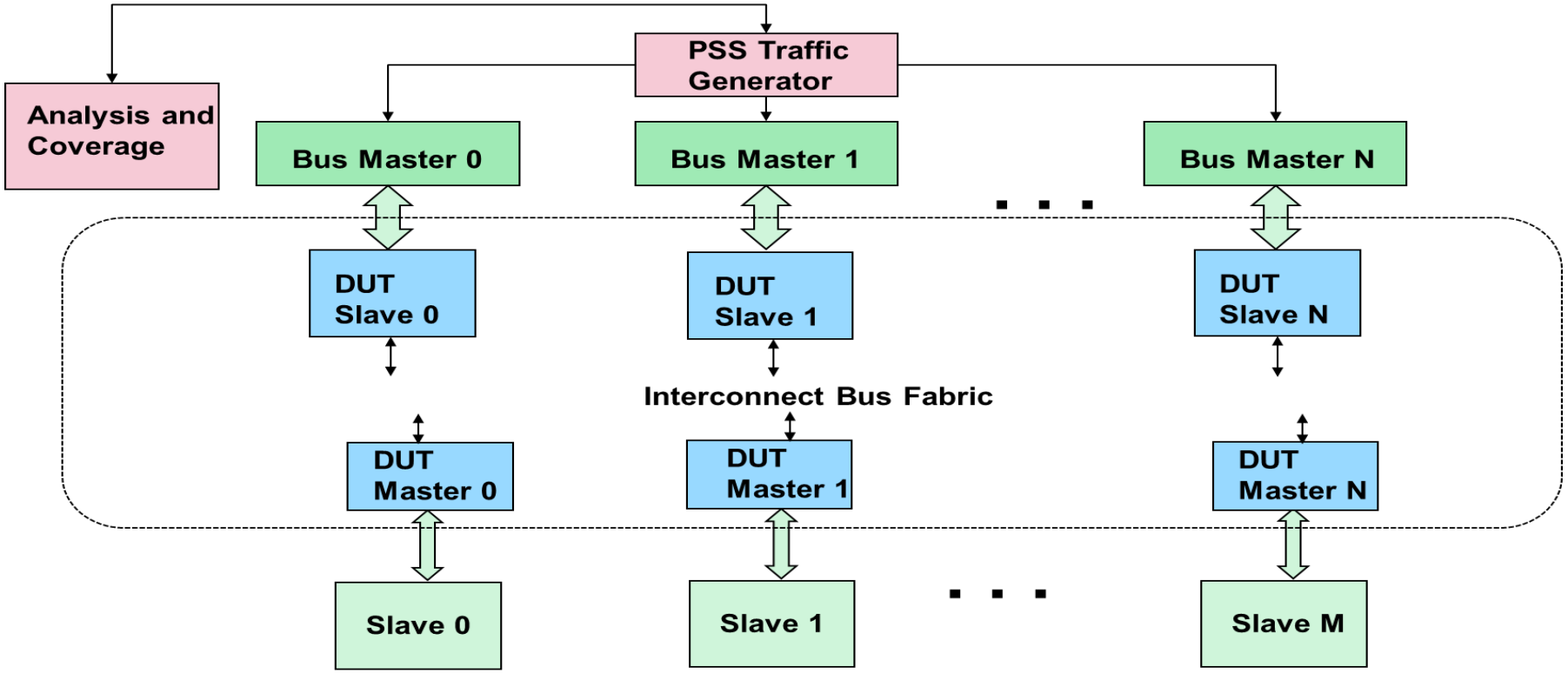
ANALOG DEVICES

accellera SYSTEMS INITIATIVE

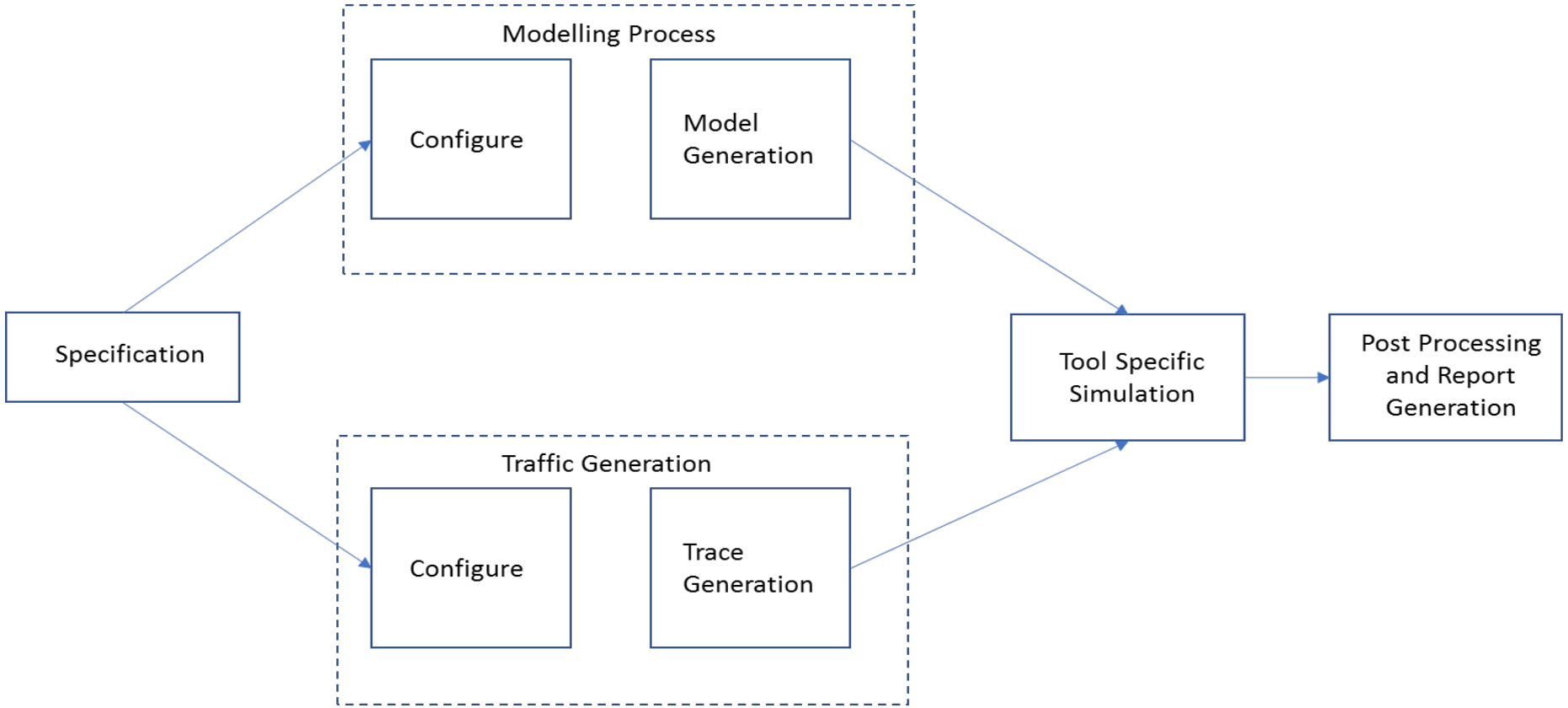
Interconnect Testing Challenges

- PSS is a new standard from Accellera
- Allows stimulus reuse across multiple platforms
- Generic Application Development using PSS
- Traffic Generator Application for Interconnect Testing Challenge
- Performance Analysis to generate best configuration
- Enhanced test quality with simplified test authoring
- Allows better coordination, resource sharing and increased productivity
- Reuse at IP, SoC level verification and Evaluation Board testing

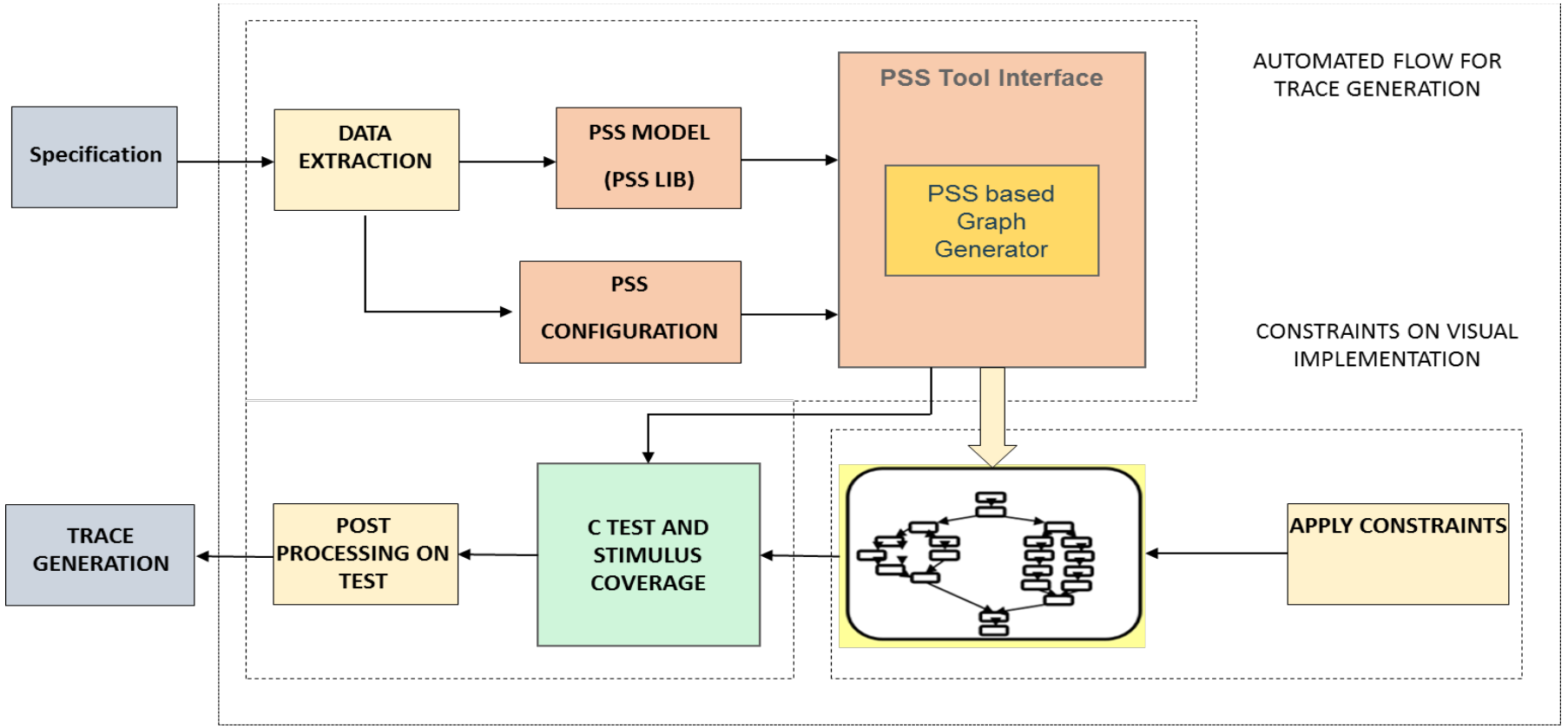
Performance Analysis and Verification of Interconnect Bus



Performance Analysis Flow using SystemC Modelling



PSS based Flow to generate Traffic Patterns



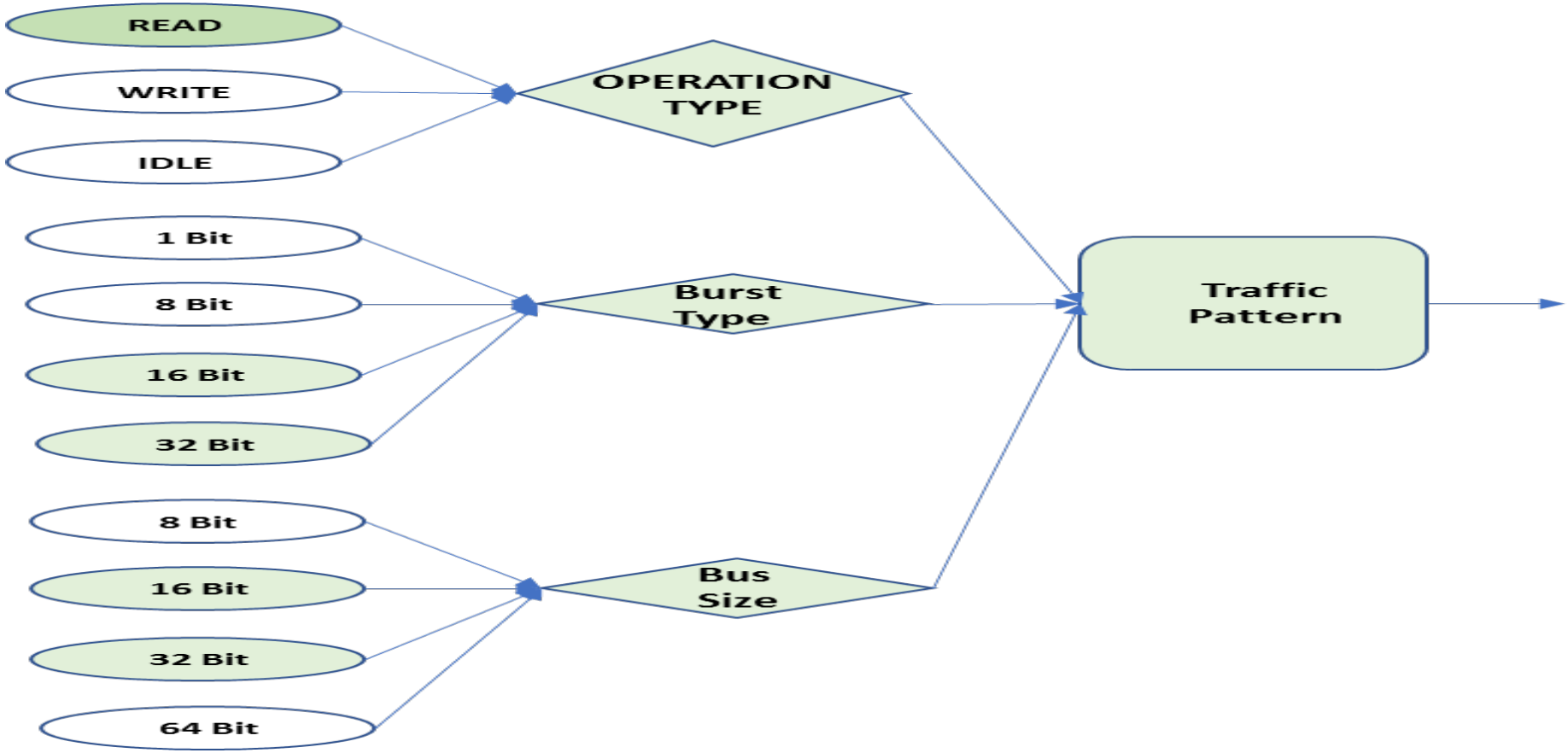
PSS based Traffic Generator

- Traffic Generator Model has multi-layered implementation
- Layer 1
  - Derived parameters from specifications written in document
  - The modeling part varies based on design specification
  - Script based code generation
  - Definition of allowed ranges for derived variables
- Layer 2
  - Constrained Randomization of the derived variables
  - Distribution to target PSS functions

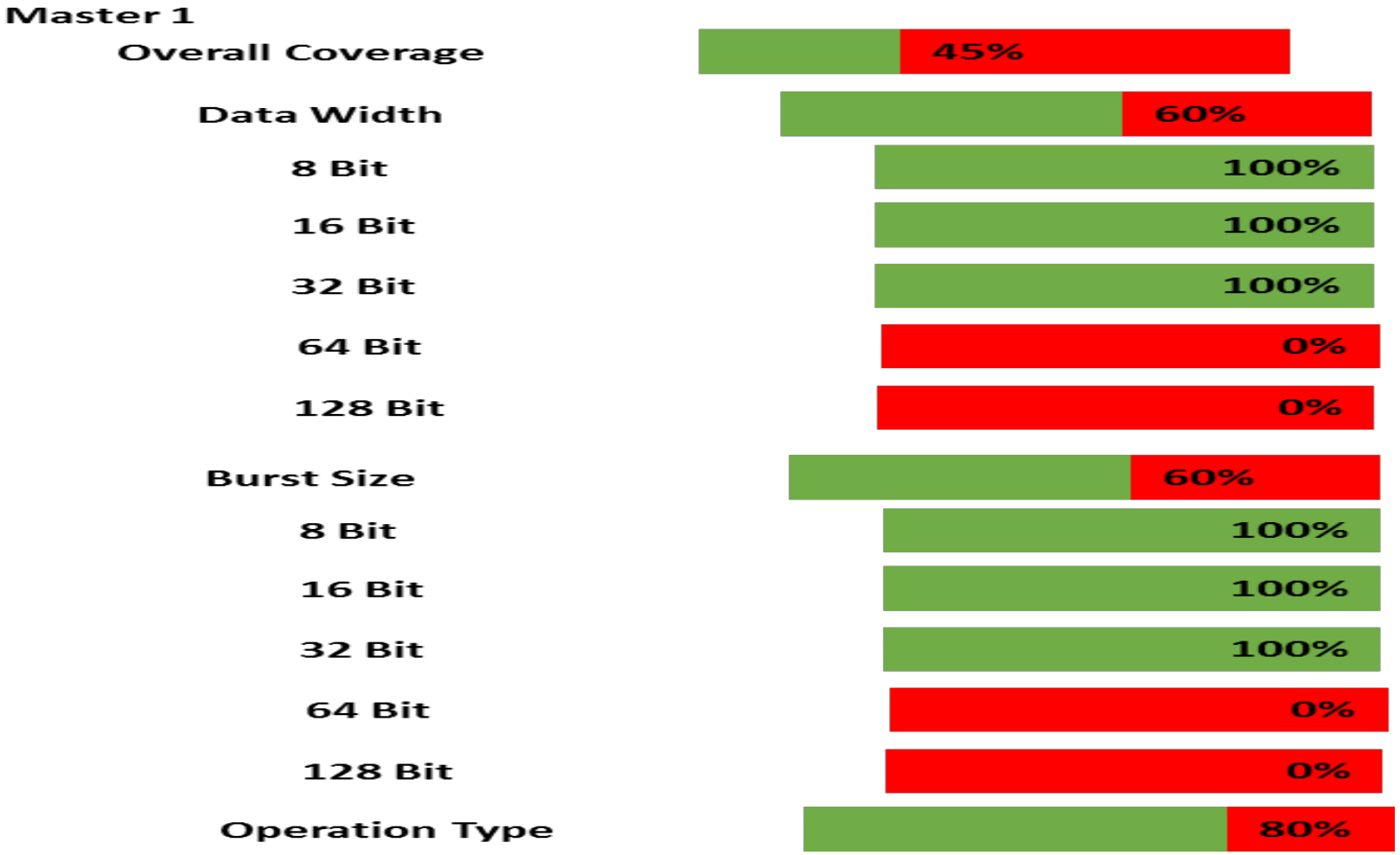
PSS based Traffic Generator

- Layer 3
  - Logical Implementation of the Traffic Generator functions
- Layer 1 to 3 are completely reusable for a given design
- Layer 4
  - Integration logic with target platforms
  - EXEC code implementation
  - Dynamically changes as per target platforms
  - SystemC, UVM and C based targets

Visual Representation of Test Intent



PSS based Coverage

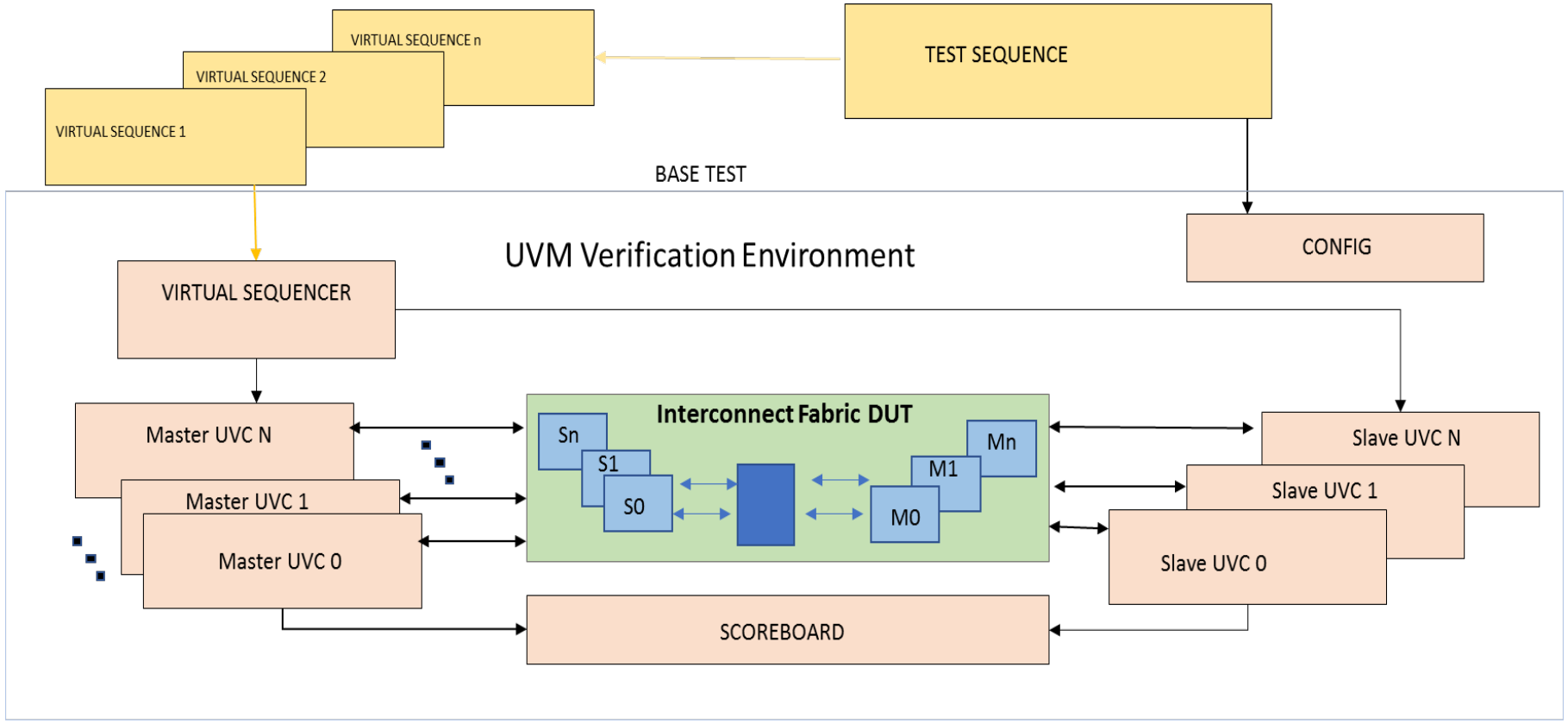


Performance Analysis Data with PSS Model

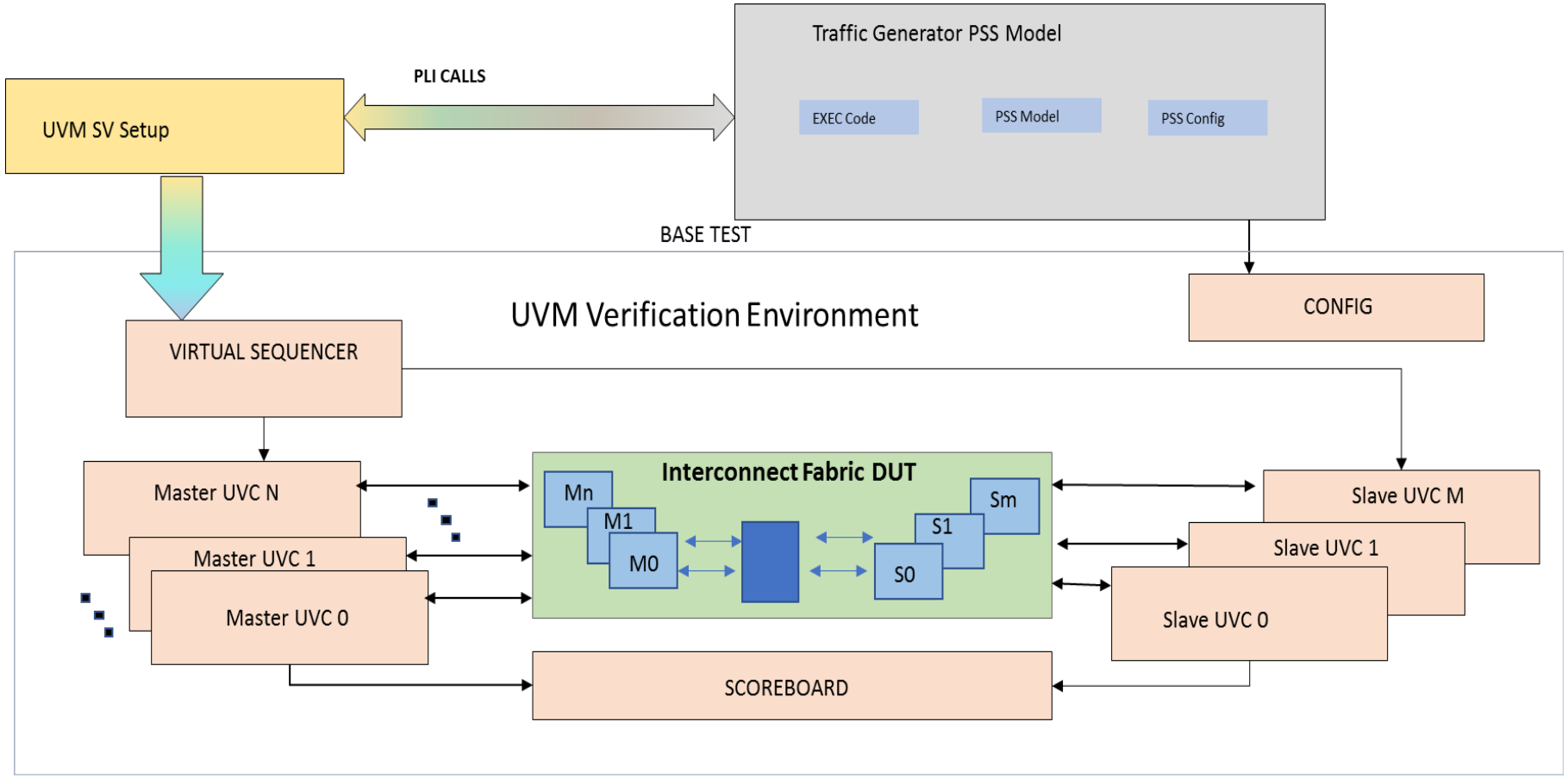
- PSS Model generates effective traffic patterns
- Increase in controllability based on parameters derived from design
- Reduction in the number of patterns and iterations

Experiment ID	Master	Slave	Direction	Mean Simulated Bandwidth	Mean Static Bandwidth	Mean Simulated Latency
5000	Core	SMMR	Read	1199.72	6000	24
5001	Core	SMMR	Write	999.79	6000	24
5002	Core	L2 Mem	Write	99.92	100	24
5003	Core	L2 Mem	Read	99.92	100	21.34

UVM based IP Verification of Interconnect Bus



PSS based IP Verification of Interconnect Bus

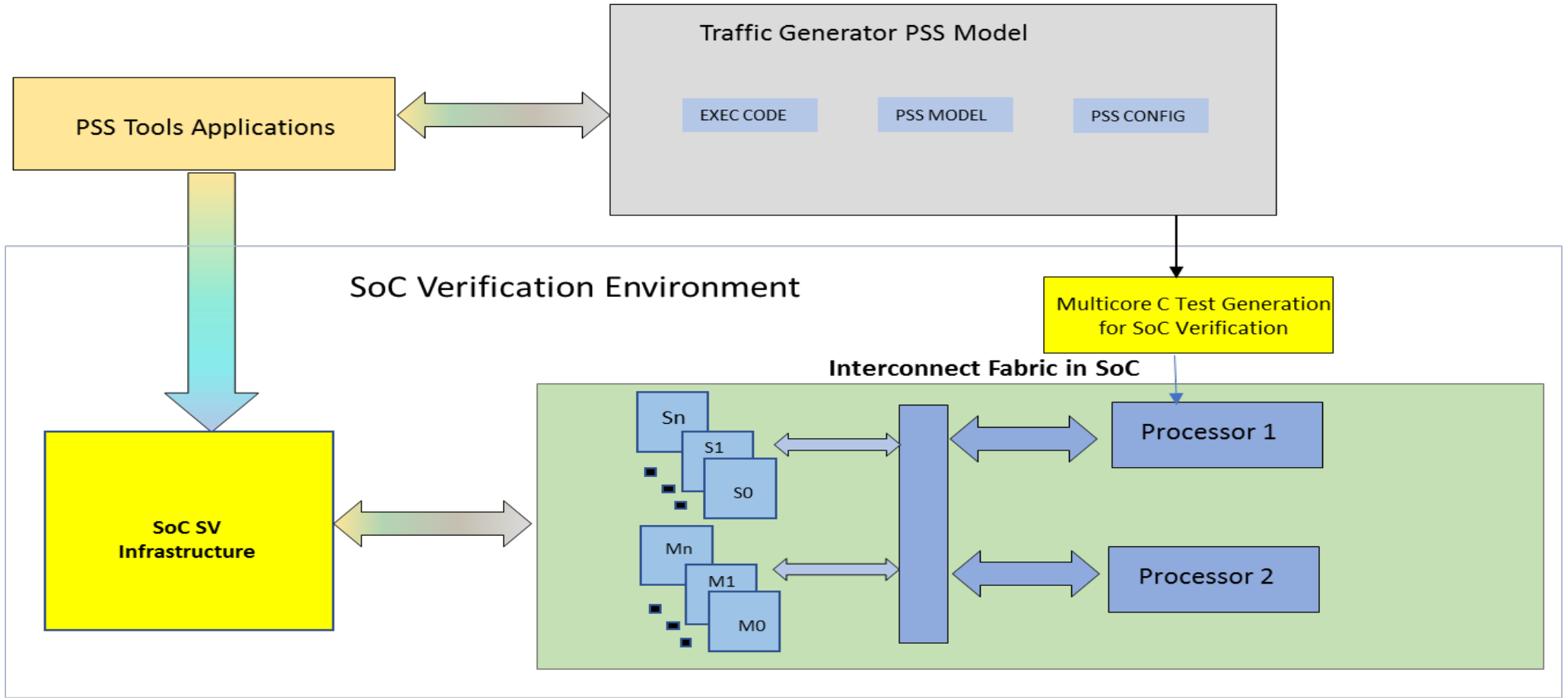


PSS UVM Setup and Regression

- The UVM based integration code is required to run the generated tests
- Visual representation of test intent
- Visual Coverage makes it easy to identify uncovered conditions
- High Quality tests covering more conditions
- More coverage with lesser number of test runs per regression

Tests Run	Passed	Failed	Not Run	Overall Code Coverage
(UVM only) 125	125	0	0	298034/388949(76.6%)
(UVM PSS) 75	75	0	0	298034/388949(76.6%)

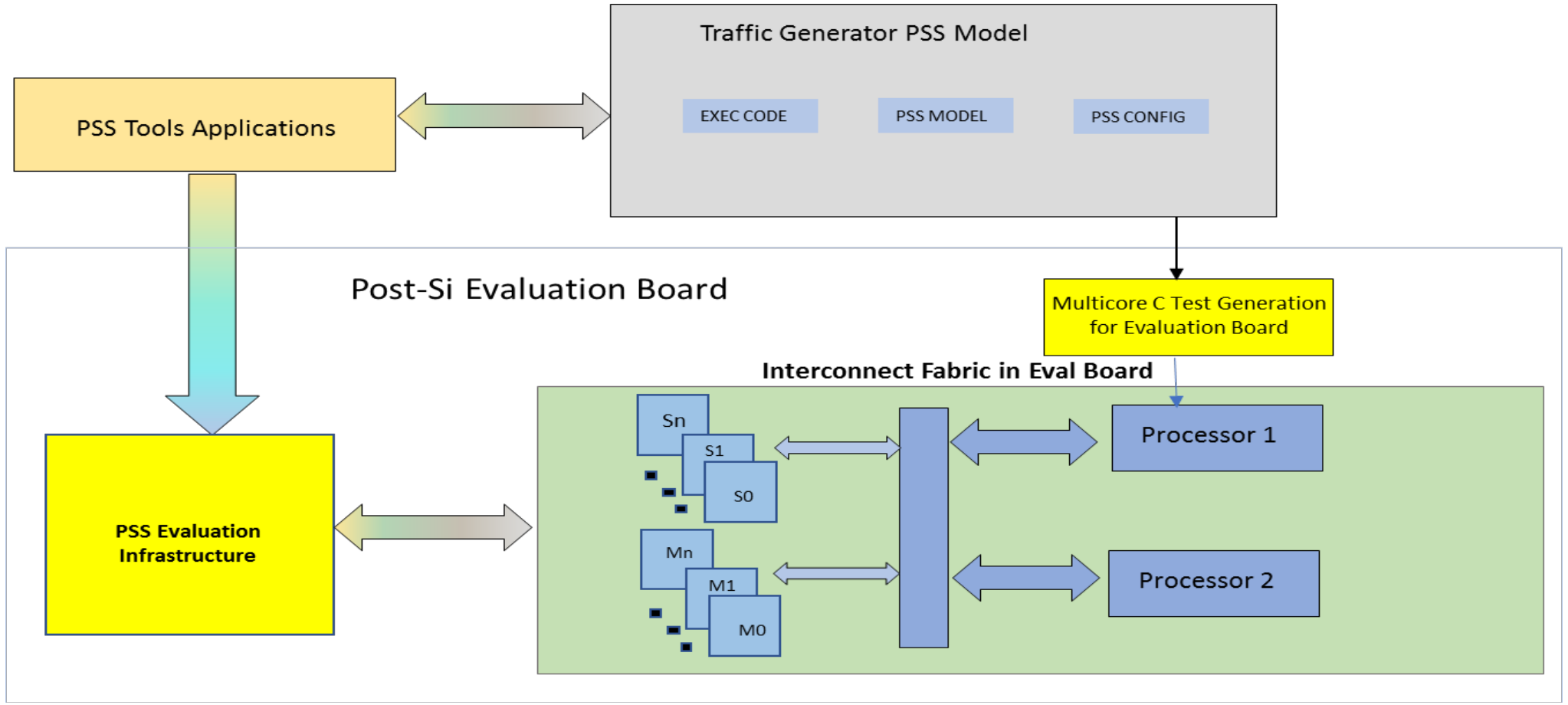
PSS based SoC Verification of Interconnect Bus



SoC based Verification Results

- PSS Model needs EXEC code related to the functions in SoC
- The functions themselves can be implemented as PSS routines or C functions
- Reuse of available SoC functions to program Bus Masters
- Model generated C tests, compiled and run on the processor for SoC simulation
- The tests inherit the same test quality as seen at the IP level
- The test generation can be directed to target SoC specific cases

PSS based Silicon Validation of Interconnect Bus



Conclusion

- PSS based approach allows reuse of the test intent from System-C based Performance Analysis to Verification and Validation
- High quality test generation with better coverage
- Lesser regression time
- One time Integration effort required for different target platforms
- The ability to create generic applications allows possibility of plug and play solutions which can further accelerate the verification and validation process.

QUESTIONS ???

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THANK YOU

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