Product Life Cycle of Interconnect Bus: A Portable Stimulus Methodology for Performance Modeling, Design Verification, and Post-Silicon Validation

Gaurav Bhatnagar
Staff Engineer, Analog Devices, Inc.

Courtney Fricano
Staff Engineer, Analog Devices, Inc.
Interconnect Testing Challenges

• PSS is a new standard from Accellera
• Allows stimulus reuse across multiple platforms
• Generic Application Development using PSS
• Traffic Generator Application for Interconnect Testing Challenge
• Performance Analysis to generate best configuration
• Enhanced test quality with simplified test authoring
• Allows better coordination, resource sharing and increased productivity
• Reuse at IP, SoC level verification and Evaluation Board testing
Performance Analysis and Verification of Interconnect Bus
Performance Analysis Flow using SystemC Modelling
PSS based Flow to generate Traffic Patterns
PSS based Traffic Generator

• Traffic Generator Model has multi-layered implementation
• Layer 1
  – Derived parameters from specifications written in document
  – The modeling part varies based on design specification
  – Script based code generation
  – Definition of allowed ranges for derived variables
• Layer 2
  – Constrained Randomization of the derived variables
  – Distribution to target PSS functions
PSS based Traffic Generator

• Layer 3
  – Logical Implementation of the Traffic Generator functions

• Layer 1 to 3 are completely reusable for a given design

• Layer 4
  – Integration logic with target platforms
  – EXEC code implementation
  – Dynamically changes as per target platforms
  – SystemC, UVM and C based targets
Visual Representation of Test Intent

- READ
- WRITE
- IDLE

OPERATION TYPE

- 1 Bit
- 8 Bit
- 16 Bit
- 32 Bit

Burst Type

- 8 Bit
- 16 Bit
- 32 Bit
- 64 Bit

Traffic Pattern

Bus Size
PSS based Coverage

Master 1

Overall Coverage

Data Width
- 8 Bit: 100%
- 16 Bit: 100%
- 32 Bit: 100%
- 64 Bit: 0%
- 128 Bit: 0%

Burst Size
- 8 Bit: 100%
- 16 Bit: 100%
- 32 Bit: 100%
- 64 Bit: 0%
- 128 Bit: 0%

Operation Type
- 45%
Performance Analysis Data with PSS Model

- PSS Model generates effective traffic patterns
- Increase in controllability based on parameters derived from design
- Reduction in the number of patterns and iterations

<table>
<thead>
<tr>
<th>Experiment ID</th>
<th>Master</th>
<th>Slave</th>
<th>Direction</th>
<th>Mean Bandwidth</th>
<th>Simulated Bandwidth</th>
<th>Mean Static Bandwidth</th>
<th>Mean Simulated Latency</th>
</tr>
</thead>
<tbody>
<tr>
<td>5000</td>
<td>Core</td>
<td>SMMR</td>
<td>Read</td>
<td>1199.72</td>
<td>6000</td>
<td>24</td>
<td></td>
</tr>
<tr>
<td>5001</td>
<td>Core</td>
<td>SMMR</td>
<td>Write</td>
<td>999.79</td>
<td>6000</td>
<td>24</td>
<td></td>
</tr>
<tr>
<td>5002</td>
<td>Core</td>
<td>L2 Mem</td>
<td>Write</td>
<td>99.92</td>
<td>100</td>
<td>24</td>
<td></td>
</tr>
<tr>
<td>5003</td>
<td>Core</td>
<td>L2 Mem</td>
<td>Read</td>
<td>99.92</td>
<td>100</td>
<td>21.34</td>
<td></td>
</tr>
</tbody>
</table>
UVM based IP Verification of Interconnect Bus
PSS based IP Verification of Interconnect Bus
PSS UVM Setup and Regression

- The UVM based integration code is required to run the generated tests
- Visual representation of test intent
- Visual Coverage makes it easy to identify uncovered conditions
- High Quality tests covering more conditions
- More coverage with lesser number of test runs per regression

<table>
<thead>
<tr>
<th>Tests Run</th>
<th>Passed</th>
<th>Failed</th>
<th>Not Run</th>
<th>Overall Code Coverage</th>
</tr>
</thead>
<tbody>
<tr>
<td>(UVM only)</td>
<td>125</td>
<td>0</td>
<td>0</td>
<td>298034/388949(76.6%)</td>
</tr>
<tr>
<td>(UVM PSS)</td>
<td>75</td>
<td>0</td>
<td>0</td>
<td>298034/388949(76.6%)</td>
</tr>
</tbody>
</table>
PSS based SoC Verification of Interconnect Bus
SoC based Verification Results

• PSS Model needs EXEC code related to the functions in SoC
• The functions themselves can be implemented as PSS routines or C functions
• Reuse of available SoC functions to program Bus Masters
• Model generated C tests, compiled and run on the processor for SoC simulation
• The tests inherit the same test quality as seen at the IP level
• The test generation can be directed to target SoC specific cases
PSS based Silicon Validation of Interconnect Bus

Traffic Generator PSS Model
- EXEC CODE
- PSS MODEL
- PSS CONFIG

Post-Si Evaluation Board

Multicore C Test Generation for Evaluation Board

Interconnect Fabric in Eval Board
- Processor 1
- Processor 2
Conclusion

• PSS based approach allows reuse of the test intent from System-C based Performance Analysis to Verification and Validation
• High quality test generation with better coverage
• Lesser regression time
• One time Integration effort required for different target platforms
• The ability to create generic applications allows possibility of plug and play solutions which can further accelerate the verification and validation process.
QUESTIONS ???
THANK YOU