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# Processing deliberate verification errors during regression

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## Quis custodiet ipsos custodes / Who will check the checkers?

- VIPs have teams of bodyguards but do they remain loyal?
- DV teams write many checkers but do they remain functional?







## The drive for automated regression

- As design complexity increases, so too do DV needs increase;
- The DV team will create a suite of testbenches and testcases.
  - Regression testing returns to, and reruns, the suite of testbenches and testcases;
  - Regression involves automatically producing coverage and pass/fail statistics;
  - We return in order to re-verify, as there will have been changes;
- While regressing, are all of our checks still functional, or are they compromised by the various changes?





While regressing, are all checks still functional, or are they compromised by the various changes?

- Why might a previous check cease to become active?
  - A qualifying condition is no longer met;
  - It gets disabled;
  - The sample clock is changed: deactivated, or masking duty-cycle;
  - 'define macros get redefined;
- Important that the DV regression proves all checks are still active;





#### Methodology to check checkers during regression

- Need agnostic method to check all checkers remain functional;
- Problem:
  - <u>Need to be deliberately producing errors;</u>
  - Standard processing of regression results reports tests as:
    - FAIL if they contain one or more errors;
    - PASS if they have no errors;
- New methodology:
  - On selected tests, introduce predefined number of deliberate errors provoke checkers;
  - Revised processing of regression results reports tests as:
    - FAIL if they do not match the predefined deliberate errors <u>or</u> have others errors;
    - PASS if they match the predefined number / style of deliberate errors **and** have no other errors;



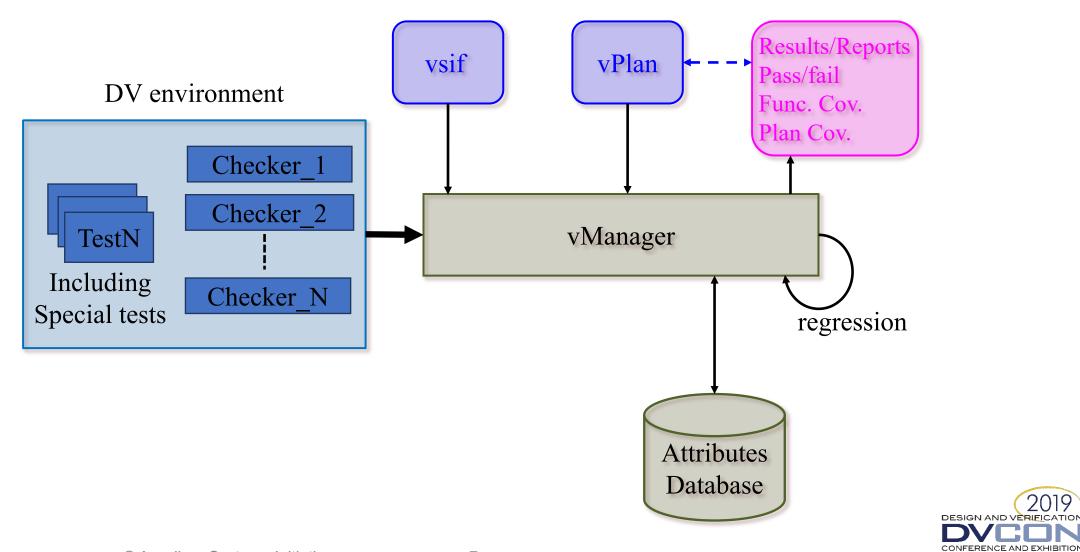
# Processing of regression results

- The regression setup will study two main aspects of the simulation data:
  - 1. The functional coverage data;
  - 2. The simulation log files containing error, warning and other information;
- The methodology proposed involves:
  - Using and adapting the Cadence<sup>®</sup> vManager<sup>™</sup> flow;
  - Adding extra intelligence to the parsing of the simulation log files;





#### Simplified vManager use-case flow

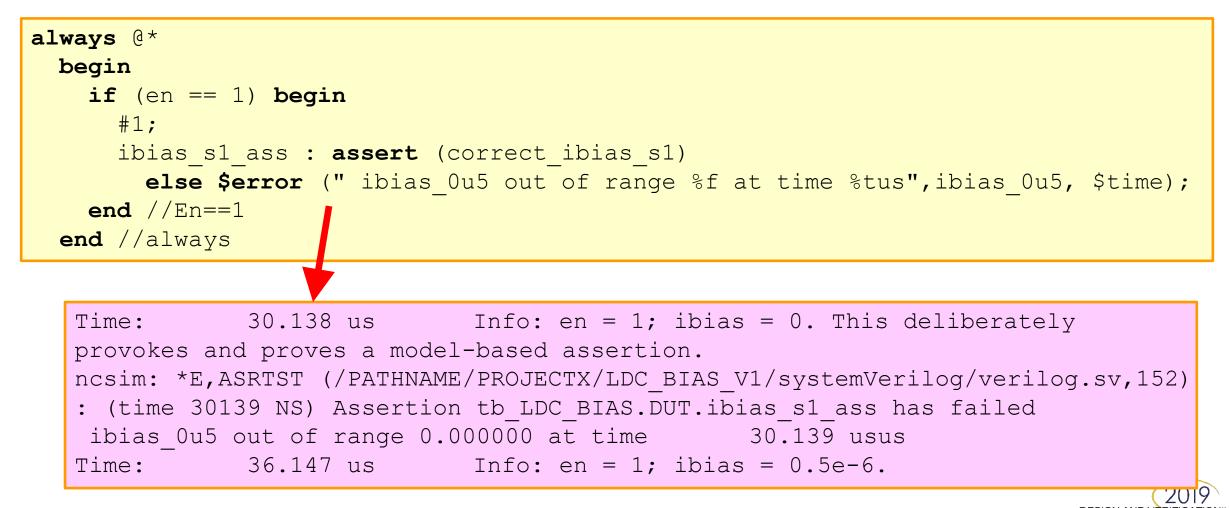




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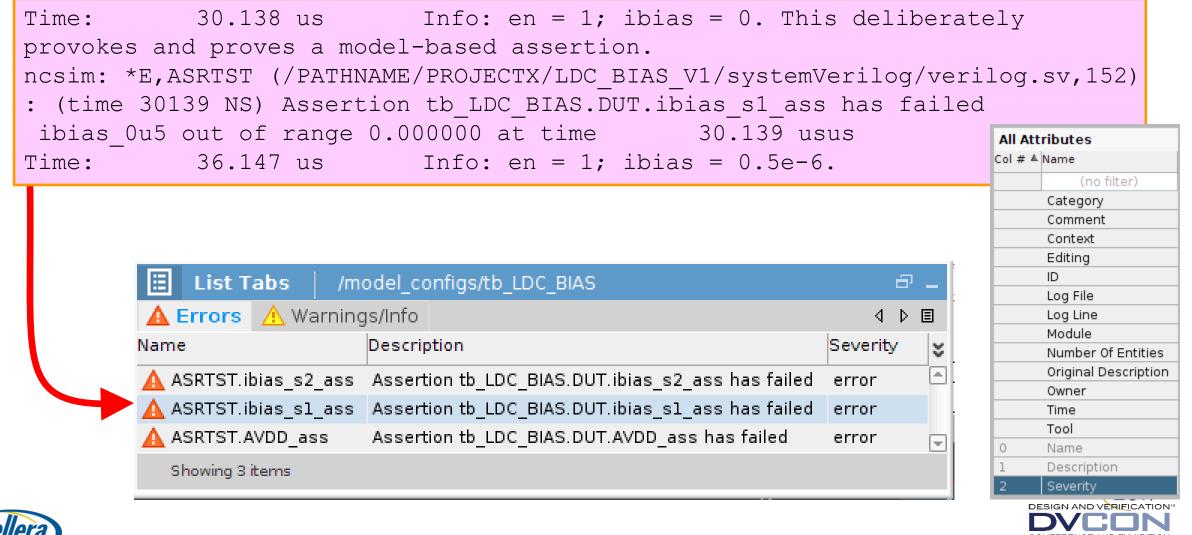
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## Assert : source code $\rightarrow$ log file



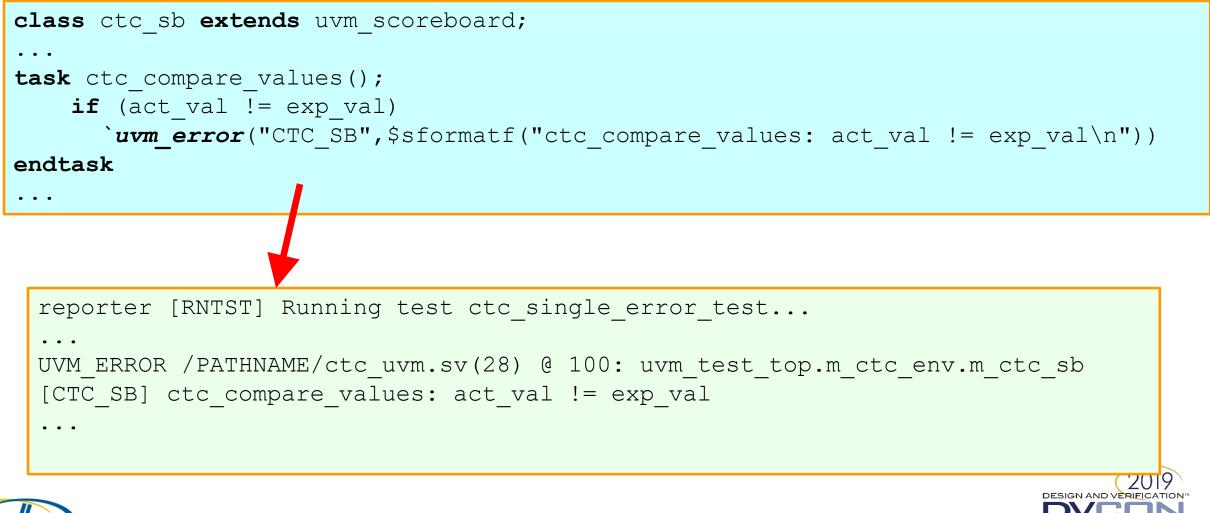


# Assert : log file $\rightarrow$ attributes in vManager DB





#### uvm\_error : source code $\rightarrow$ log file

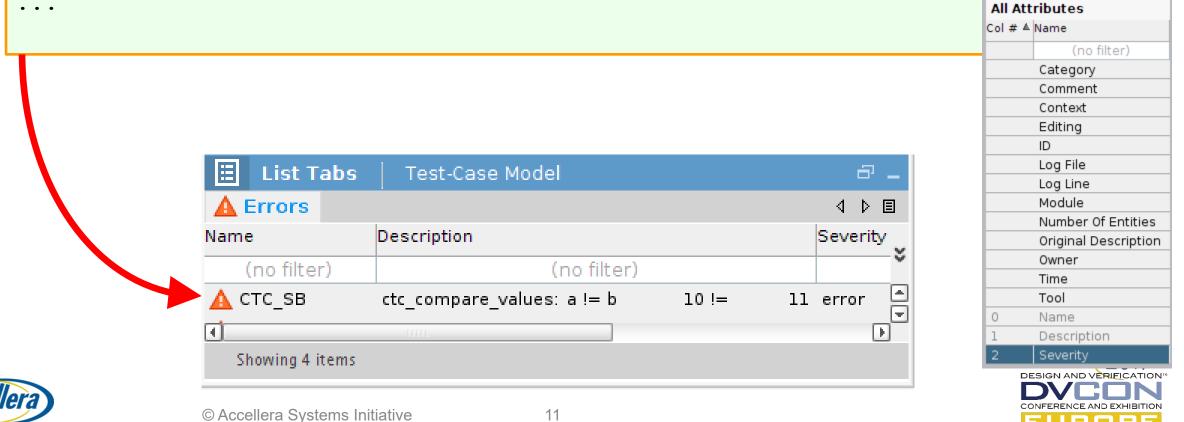




#### uvm\_error : log file $\rightarrow$ attributes in vManager DB

reporter [RNTST] Running test ctc\_single\_error\_test...

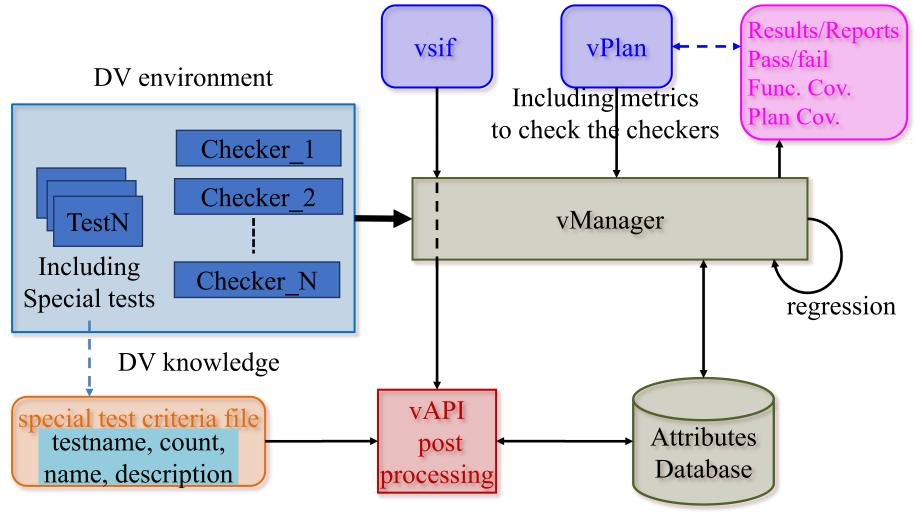
UVM\_ERROR /PATHNAME/ctc\_uvm.sv(28) @ 100: uvm\_test\_top.m\_ctc\_env.m\_ctc\_sb [CTC SB] ctc compare values: act val != exp val





. . .

### Adapted vAPI vManager use-case flow





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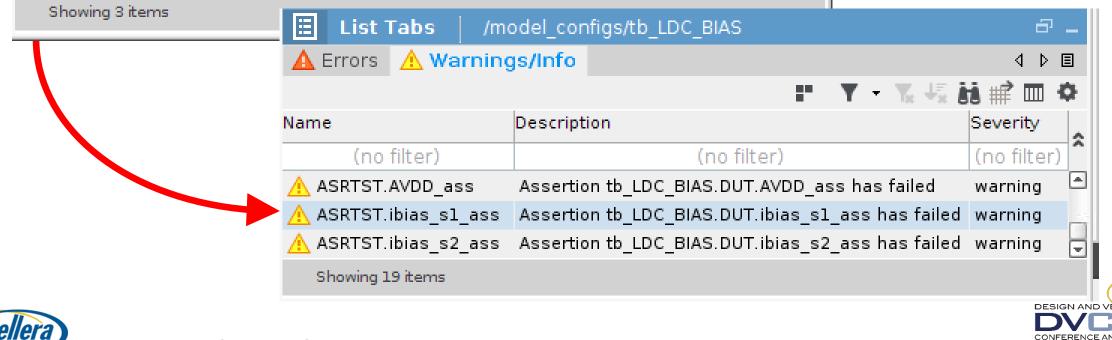
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JROP

## Down-grading of attributes in vManager DB

🗄 List Tabs /m	odel_configs/tb_LDC_BIAS	Ð	
🛕 Errors 🔥 Warning	js/Info	4 Þ	E
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🛕 ASRTST.ibias_s2_ass	Assertion tb_LDC_BIAS.DUT.ibias_s2_ass has failed	error	•
🛕 ASRTST.ibias_s1_ass	Assertion tb_LDC_BIAS.DUT.ibias_s1_ass has failed	error	
🛕 ASRTST.AVDD_ass	Assertion tb_LDC_BIAS.DUT.AVDD_ass has failed	error	





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## Down-grading of attributes in vManager DB

🗄 List Tabs	Test-Case Model		ē _
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e Model		- <sup>6</sup>
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000		
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#### New attributes in vManager DB – count mismatch

🗄 List Tabs	Test-Case Model		- <sup>-</sup>
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	🗄 List Tabs	Test-Case Model	- <sup>-</sup>
	A Errors		4 ▷ 国
	Name	Description	Severity
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	•		Ð
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)	© Accellera Systems Initiative	15	



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#### vManager DB – regression analysis, prior to vAPI

0 R	uns			5	_
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Index 🔺	Name	Status 🖓	#Errors	Duration (sec.)	
(no filte	(no filter)	(no filter)	(no filter	(no filter)	×
1	(model_configs/tb_LDC_BIAS	😮 failed	3	72	
2	(model_configs/tb_LDC_SWACC)	😮 failed	2	65	
3	/model_configs/tb_LDC_SWMGR	😮 failed	1	63	
4	(model_configs/tb_VDAC_TOP)	😮 failed	4	65	
5	(model_configs/tb_PWR_TEST)	😮 failed	1	65	
6	/schem_configs/tb_LDC_BIAS	📀 passed	0	126	
7	/schem_configs/tb_LDC_SWACC	📀 passed	0	251	
8	<pre>/schem_configs/tb_LDC_SWMGR</pre>	📀 passed	0	260	
9	/schem_configs/tb_VDAC_TOP	⊘ passed	0	1336	
10	/schem_configs/tb_PWR_TEST	⊘ passed	0	171	F
Show	ving 10 items				





### vManager DB – regression analysis, after vAPI

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1	(model_configs/tb_LDC_BIAS)	📀 passed *	0	76	
2	(model_configs/tb_LDC_SWACC	🥝 passed *	0	68	
3	/model_configs/tb_LDC_SWMGR	🥝 passed *	0	65	
4	(model_configs/tb_VDAC_TOP)	🥝 passed *	0	65	
5	(model_configs/tb_PWR_TEST)	🥝 passed *	0	65	
6	🔘 /schem_configs/tb_LDC_BIAS	📀 passed	0	108	
7	/schem_configs/tb_LDC_SWACC	📀 passed	0	206	
8	/schem_configs/tb_LDC_SWMGR	📀 passed	0	210	
9	/schem_configs/tb_VDAC_TOP	🥝 passed	0	1019	
10	/schem_configs/tb_PWR_TEST	🥝 passed	0	136	
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## vManager – vPlan metrics for special tests

🛃 vPlan Hierarchy				
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2.2.2 dual_error_dual_expected	,° (7		All	🕨 O 🌆 Types
				2010





### vManager – vPlan coverage for special tests

vPlan Hierarchy		
ctc_uvm 👻 📑		
Ex UNB Name	Overall Average Grade	Overall Covered
(no filter)	(no filter)	(no filter
🔺 💟 ctc_uvm	✓ 100%	4 / 4 (100%)
🖌 🗖 1 Checks	✓ 100%	1/1(100%)
🔺 🗖 1.1 Data model and design equivalent	✓ 100%	1/1(100%)
I.1.1 values_compared	✓ 100%	1/1(100%)
🖌 🗖 2 Tests	✓ 100%	3/3(100%)
2.1 Normal operation	✓ 100%	1/1(100%)
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🔺 🗖 2.2 Force checker error	✓ 100%	2/2(100%)
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## vAPI post-processing

- Controlled invocation from the vsif flow "post session";
- A python script is used but other formats, Perl, are alternatives;
  - 1. Read and parse the special test criteria file;
  - 2. Using REST / JSON: traverse the attributes database loop through all runs and all errors;
  - 3. Down-grade error attributes which match special test criteria; keep tally;
  - 4. If tally mismatches, introduce new error;
  - 5. Write back down-grades and new errors to the attributes database;





## Special test criteria file – \*.csv format – Ex. #1

test_name	count	name	description
tb_LDC_BIAS	1	ASRTST.AVDD_ass	Assertion tb_LDC_BIAS.DUT.AVDD_ass has failed
tb_LDC_BIAS	1	ASRTST.ibias_s1_ass	Assertion tb_LDC_BIAS.DUT.ibias_s1_ass has failed
tb_LDC_BIAS	1	ASRTST.ibias_s2_ass	Assertion tb_LDC_BIAS.DUT.ibias_s2_ass has failed
tb_LDC_SWACC	2	ASRTST.vdd_ass	Assertion tb_LDC_SWACC.DUT.vdd_ass has failed
tb_LDC_SWMGR	1	ASRTST.vdd_ass	Assertion tb_LDC_SWMGR.DUT.vdd_ass has failed
tb_VDAC_TOP	1	ASRTST.ibdacen_ass	Assertion tb_VDAC_TOP.DUT.ICORE.ibdacen_ass has failed
tb_VDAC_TOP	1	ASRTST.dacref_ass	Assertion tb_VDAC_TOP.DUT.ICORE.dacref_ass has failed
tb_VDAC_TOP	1	ASRTST.vref_ass	Assertion tb_VDAC_TOP.DUT.ICORE.vref_ass has failed
tb_VDAC_TOP	1	ASRTST.vdd_ass	Assertion tb_VDAC_TOP.DUT.ICORE.vdd_ass has failed
tb_PWR_TEST	1	ASRTST.vdd_ass	Assertion tb_PWR_TEST.DUT.vdd_ass has failed



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## Special test criteria file – \*.csv format – Ex. #2

test_name	count	name	description
single_error_expected	1	CTC_SB	ctc_compare_values
single_error_dual_expected	2	CTC_SB	ctc_compare_values
dual_error_dual_expected	2	CTC_SB	ctc_compare_values



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## Conclusions

- We started explaining the need to check the checkers;
- We showed that introducing deliberate errors will explicitly demonstrate that the checkers are active;
- We showed that a cleverer PASS/FAIL definition can understand realand deliberate-errors;
- This flow is now being actively used on a live project at ams;



#### Questions





## Miscellaneous supplementary slides

- vsif flow script excerpt;
- vAPI python several script excerpts;





#### Miscellaneous – vsif script excerpt

```
session MINI Projectx model vs schem {
  top dir : $ENV(SIM DIR)/../vmgr sessions;
  . . .
  post session script: "check the checker.py";
  group model configs {
    run script: "runams -cell $ATTR(test name) -view model config -simulate batch ..."
    special_test_criteria_file : "$ENV(DV DIR)/bin/vsifs/MINI model vs schem special-test-criteria-file.csv";
    . . .
    test tb LDC BIAS;
    . . .
  };
  group schem configs {
    run script: "runams -cell $ATTR(test name) -view schem config -simulate batch ...";
    . . .
    test tb LDC BIAS;
    . . .
  };
};
```



#### Miscellaneous – vAPI.py – REST definitions

```
set server(vmgr project="vmgr", server='https://'+vmgr server, user=vmgr username, passwd=vmgr password)
headers = \{
        'content-type':'application/json',
        'X-VMGR-Routing-Finalize' : 'true'
request={
         "filter" : { "@c" : ".AttValueFilter",
                      "attName" : "parent session name",
                      "operand" : "EQUALS",
                      "attValue" : session name
                    ł,
          "projection" : {
                       "selection" : ["id", "test name", "special test criteria file", "index",
"failures count", "failed runs count", "errors count", "sv seed", "log file"]
runs response = post(url='/runs/list', request=request, headers=headers)
runs response list = runs response.json()
```



#### Miscellaneous – vAPI.py – loop through runs

```
# Loop over all the runs of the current session
for run resp in runs response list :
 if (run resp.has key('special test criteria file')) :
   print " = POST PROCESSING ="
   print " Run: special test criteria file = " + run resp['special test criteria file']
   exists = os.path.isfile(run resp['special test criteria file'])
   if exists :
     with open(run resp['special test criteria file'], 'rb') as csvfile:
       spamreader = csv.reader(csvfile, delimiter=',', quotechar='/')
       for row in spamreader:
         if (HDR found & HDR real data) :
          expected test name = row[0]
          expected count = int(row[1])
          expected name = row[2]
          expected description = row[3]
 else :
   print " = N O P O S T P R O C E S I N G ="
```





#### Miscellaneous – vAPI.py – loop thru error attributes

# Read severe message for this run

```
severe_msg_response = post(url='/severe-messages/list',request=request,headers=headers)
severe_msg_response_list = severe_msg_response.json()
```

# Loop over all severe messages of this run.

for severe\_msg\_resp in severe\_msg\_response\_list :

• • •





#### Miscellaneous – vAPI.py – matching algorithm





#### Miscellaneous – vAPI.py – write-back attributes DV

request={





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- Please keep the default font size for main lines at 28pt (or 26pt)
   And use 24pt (or 22pt) font size for the sub bullets
- Use the default bullet style and color scheme supplied by this template
- Limited the number of bullets per page.
- Use keywords, not full sentences
- Please do not overlay Accellera or DVCon logo's
- Check the page numbering





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- Do not use recurring text in headers and/or footers
- Do not use any sound effects
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- Limit use of animations (not available in PDF export)





# Guidelines (3)

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- Embed pictures in vector format (e.g. Enhanced or Window Metafile format)



