Highlight the power aware verification challenges involved for a design having power states defined using add_power_state command.

Power State to PST Conversion: Simplifying static analysis and debugging of power aware designs

Case Study 2

Consistency / Error Checks in power state definitions

- **add_power_state command**, which is used to define power states and supply sets should have consistent and powerful command. It allows usage of boolean operators in supply and logic expression to define the relationship between two objects. Using random boolean operators like xor, xnor in power state definitions can result in power state definitions that are difficult to understand, debug and verify. For tools to analyze:
  - logic_xor in power state definition of power states should refer to supply signals.
  - logic_ne in power state definition of supply sets should refer to control signals.

Guidelines for modeling power states with add_power_state command

- UPF command should be used to define power states and supply sets in a clear, consistent, flexible and powerful command. It allows usage of boolean operators in supply and logic expression to define the relationship between two objects. Using random boolean operators like xor, xnor in power state definitions can result in power state definitions that are difficult to understand, debug and verify. For tools to analyze:
  - logic_xor in power state definition of power states should refer to supply signals.
  - logic_ne in power state definition of supply sets should refer to control signals.

Case Study 1

Even at this stage when implementation UPF is not present, the power state display can also be done. Verification tool provides to perform static analysis to determine the isolation requirements.

Conclusion

To specify the power modes, power states are now defined on supply sets & power domains using UPF add_power_state command. As this UPF command provides lot of flexibility and power, it often results in potentially complex and difficult to understand power state definitions with supply and logic nets. In this paper, we have highlighted the power aware verification challenges involved for a design having power states defined using add_power_state command. Additionally, we demonstrated how the process of static analysis & debugging of design is a fairly straightforward process. However, the static analysis & debugging is not intuitive with power state definitions involving supply and logic nets. In this paper, we have highlighted the power aware verification challenges involved for a design having power states defined using add_power_state command. Additionally, we demonstrated how the process of static analysis & debugging of design is a fairly straightforward process. However, the static analysis & debugging is not intuitive with power state definitions involving supply and logic nets. In this paper, we have highlighted the power aware verification challenges involved for a design having power states defined using add_power_state command. Additionally, we demonstrated how the process of static analysis & debugging of design is a fairly straightforward process.