Power Management Verification for SoC ICs

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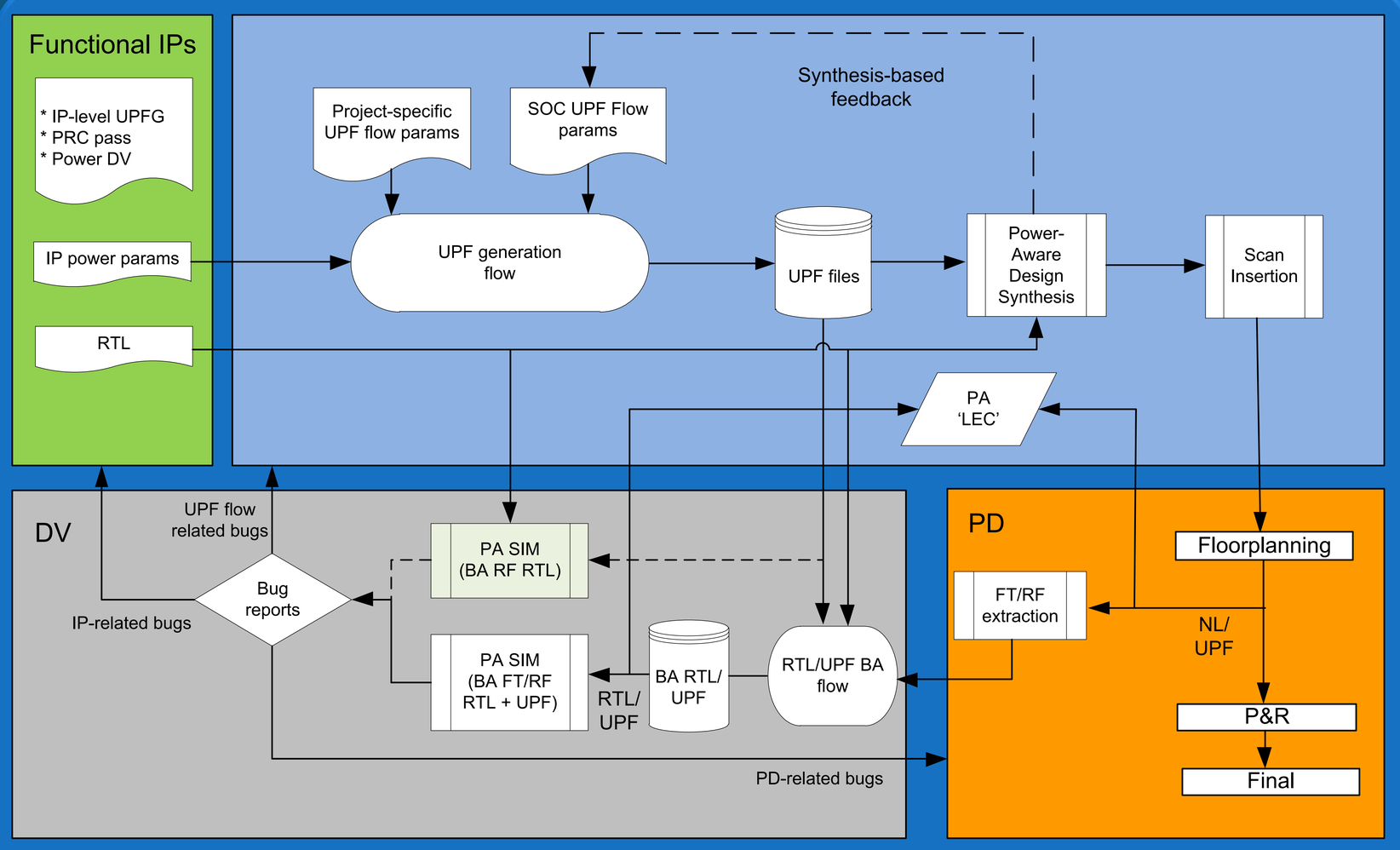
Abstract

- *We present an overview of power-aware verification methodology employed in verification of AMD's Accelerated Processor Units (APUs) and Graphics Processing Units (GPUs).*
- *The employed methodology balances the demands for optimal test coverage of power-management features of SoC Integrated Circuits (ICs) of growing complexity and narrowing windows of project duration.*

Power-Aware Design Flow

- UPF generation flow is a key element of Power Management implementation and Power-Aware verification of SOC ICs
- Functional IP teams provide parameters which include information about power-aware components and behavior of those IPs -- isolation, power domains, retention policies, always-on logic, among the other parameters.
- Those parameters are processed by SOC CAD flow which generates UPF files corresponding to supplied power parameters and RTL
- The generated UPF files are used for power-aware synthesis, scan insertion flow and Design Verification (DV).



Power Management Techniques	Internal Power Switch	Voltage changes	Clock gating	Frequency changes	External Power shutdown	Power Supply Interrupted
Frequency scaling	No	No	No	Yes	No	No
Clock gating	No	No	Yes	Yes	No	No
VFS	No	Yes	Yes	Yes	No	No
	Yes	Yes	Yes	Yes	No	No
Power Gating	Yes	Yes	--	--	No	Yes
Voltage Island shutdown	No	Yes	--	--	Yes	Yes
	Yes	Yes	--	--	No	Yes
Power State Transitions	No	Yes	Yes	Yes	No	No
Performance control	If PG enabled	No	Yes	No	No	No

Power Management verification – RTL level

- The non-power-gating verification category assumes that the power management of the circuitry in question is carried out without interrupting the power supply of the circuitry in question.
- In some of such techniques the voltage levels are regulated. However, power supply is never interrupted.
- Thanks to that, verification is carried out without employing power-aware tools that emulate power interruption to parts of the design.
- Power-aware verification category refers to the power-management techniques in which power supply to the areas in question is interrupted.
- For this category a power-aware simulation tools need to be employed for verification.
- Those tools, based on RTL and UPF description, emulate power events such as power gating. Those tools also infer design elements described outside RTL, in UPF, such as isolation ("clamp") cells and power switches.

Back-annotated verification flow

- Repeaters are introduced both during synthesis and physical design stages in order to satisfy chip's timing constraints and improve timing performance.
- The repeaters are implemented as either buffers or flip-flops.
- Flip-flop repeaters are back-annotated to the RTL view of the SoC. However, the power domain information contained in the UPF files is not back-annotated during this process.
- The repeater buffers introduced during synthesis and PD stages are usually not back-annotated since buffers don't change logic behavior of the RTL.
- Obviously, introduction of new elements at post-RTL stages presents a verification "hole" for power-aware verification since those elements were not verified at power-aware RTL verification stage.

To verify PD-added elements, a new flow was proposed and implemented:

- Power-Aware Repeater/Feedthrough Back Annotation (PARBA) flow simulates power-annotated repeaters and feed-through buffers
- PARBA flow takes place after repeaters and feedthrough buffers are inserted by PD flow
- PD-provided file with flip-flop repeaters and feedthrough buffers information, including power domain allocation, is used as input to CAD flow to re-group existing back-annotated repeater flip-flops based on power domains. The CAD flow also adds feedthrough buffers to the RTL. UPF files are updated with the respective power domains information for flip-flop repeaters and feedthrough buffers
- UPF flow uses same PD-provided file with back-annotated repeaters information to produce UPF containing repeater/feedthrough buffers power domains information.
- Static Power Rule Check (PRC) and power-aware Logic Equivalence Check (LEC) will ensure that synthesis and PD flow don't violate the power intent of the IC
- Other tools ensure that power connections for analog IPs and macros are connected properly in the physical design all the way up through the IO pads ("bumps"), also ensuring that no power or ground pins are unconnected.