

Power estimation – what to expect what not to expect

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Background

- Aquantia – Privately held company
- Delivers High Speed Ethernet connectivity solutions for large-scale Data Centers and Cloud computing
- Power estimation techniques were successfully used for various chips at Terantics/PLX/Aquantia

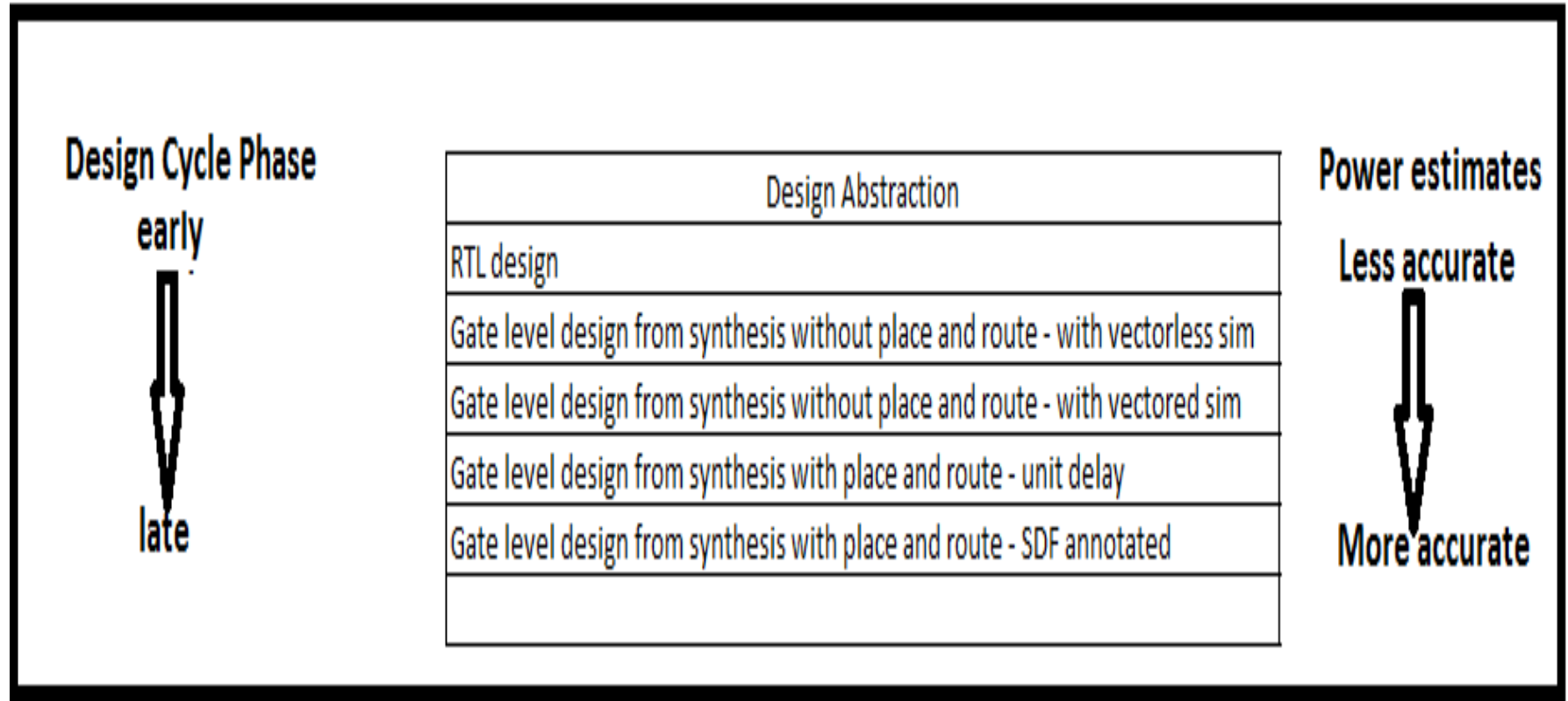
Why power estimation ?

- Selection of optimum architecture
- Hardware versus Software implementation
- Process node selection
- Voltage selection for the design
- Clock gating decisions
- Power gating decisions
- Package design

Why power estimation ? - continue

- Low power key feature of 10G-BaseT chip
- Accurate and efficient power estimation key for low power
- Explore different abstraction levels (Behavioral, RTL and Gate) for power estimation to study tradeoffs

Power estimates and accuracy tradeoffs



Design Cycle Phase

early



late

Design Abstraction

RTL design

Gate level design from synthesis without place and route - with vectorless sim

Gate level design from synthesis without place and route - with vectored sim

Gate level design from synthesis with place and route - unit delay

Gate level design from synthesis with place and route - SDF annotated

Power estimates

Less accurate



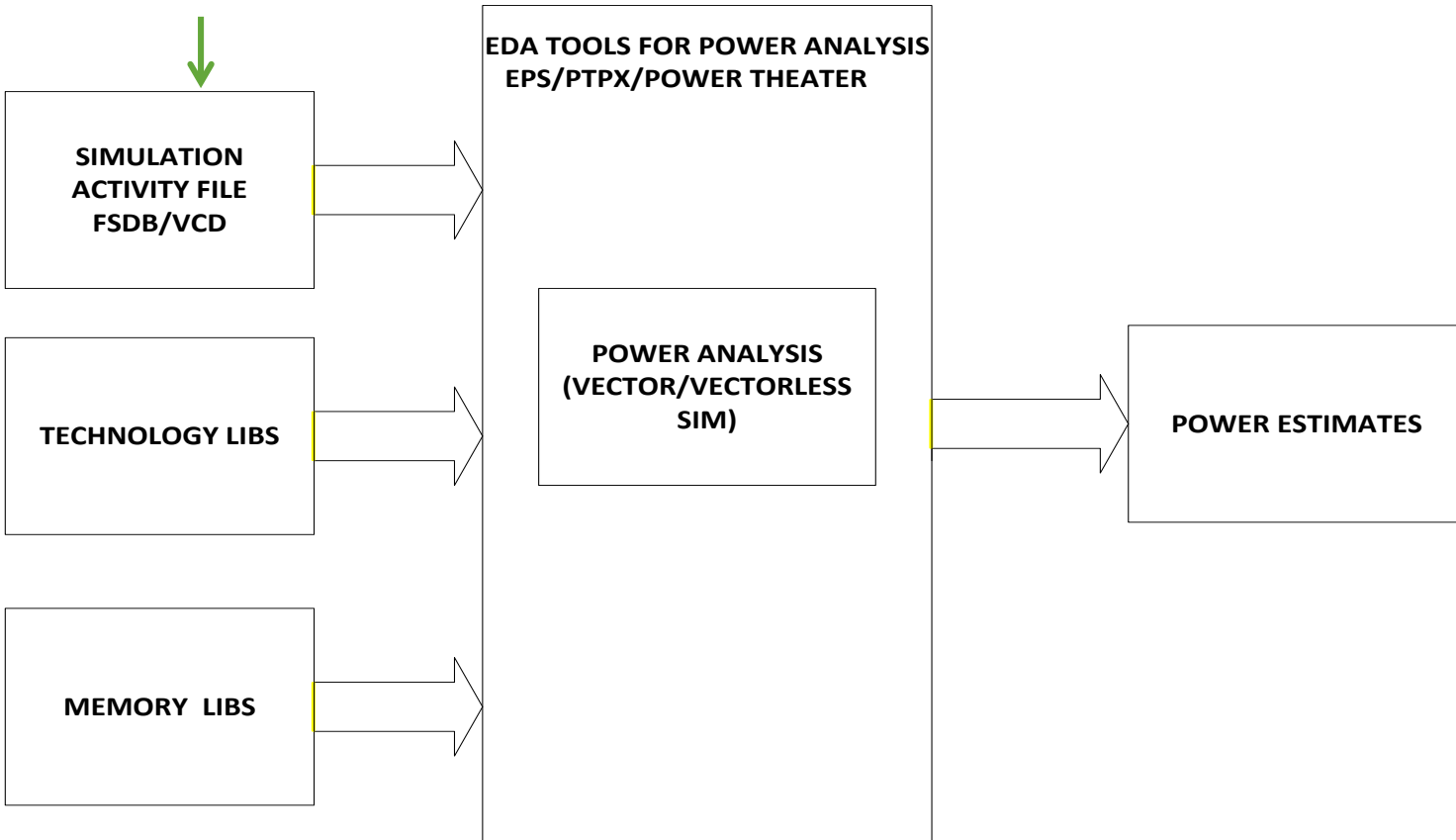
More accurate

Vector v/s Vectorless simulation

- Vectorless simulation
 - Early estimates
 - No simulation activity file
 - Assumes toggle activity
 - Less accurate
- Vectored simulation
 - Late in the design cycle
 - Actual simulation activity file
 - More accurate

Power estimation testbench

Used only for
Vectored sim



Activity file generation flow Capture and Playback

- Verilog RTL DUT + SV UVM testbench
- RTL sim and capture DUT Inputs/Outputs
- Verilog Gate Level Netlist DUT + SV UVM testbench
- Gate Level Sim with SDF annotation with Inputs from RTL sim
- Activity file from Gate Level sim with correct activity period

Capture playback vs Traditional method for activity file generation

- Traditional Method
 - Same testbench, replace RTL with Gate netlist
 - Difficult to debug
- Capture playback method
 - Does not require full chip testbench
 - Faster
 - Clock phasing, etc cannot be modelled

Power estimation – Different scenarios

- Compare different EDA tools results
- Can I rely on Vectorless sim ?
- Which blocks to power gate ?
- Which blocks to clock gate ?
- Select optimum architecture
- Select process node 40nm – 28 nm
- Select voltage for process node
- Select capacitance value for package design

Power comparison – Different EDA tools results match !!

TRUE LEAKAGE CORNER - power in mW			
DSP Block 40nm	Static	Dynamic	Total
PTPX	152.33	545.4	697.73
EPS	154.7	572.2	726.9
PowerTheater	151.29	535.3	686.75

Results within 7-8 %



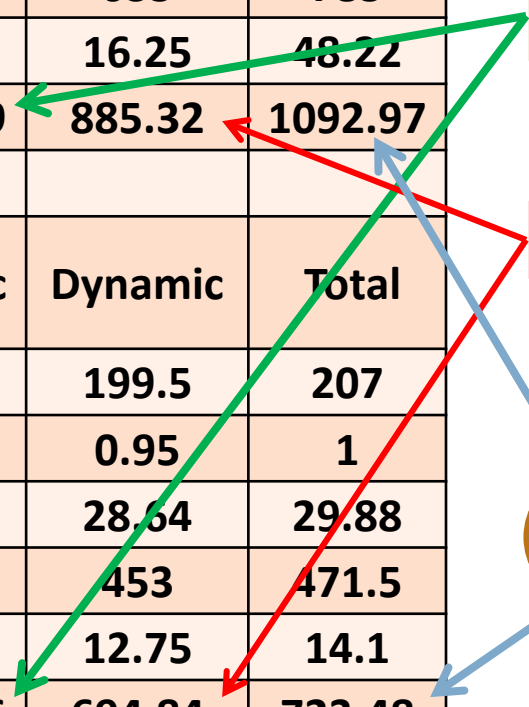
Vectorless sim - Is it accurate?

VECTORLESS SIM	TRUE LEAKAGE CORENER		
DSP Block 40nm - 0.88V, 125C	Static	Dynamic	Total
internal reg power	44.25	201.5	246
internal latch power	0	0.02	0.02
memory power	5.3	32.55	37.85
other internal power	152.5	635	787.5
clock power	7.85	16.25	24.1
Total power	209.9	885.32	1092.97
DSP Block 28 nm - 0.935V, 125C	Static	Dynamic	Total
internal reg power	7.65	199.5	207.15
internal latch power	0.05	0.95	1
memory power	1.23	28.64	29.87
other internal power	18.6	453	471.6
clock power	1.33	12.75	14.08
Total Power	28.86	694.84	723.48

Accurate

Inaccurate

Relative comparison



Vectorized simulation

VECTORED SIM	TRUE LEAKAGE CORENER		
DSP Block 40nm - 0.88V, 125C	Static	Dynamic	Total
internal reg power	33.95	183.5	217.5
memory power	39.4	55	94.5
other internal power	77.5	288.5	366
clock power	0.44	8.3	8.75
Total power	151.29	535.3	686.75
DSP Block 28 nm 0.825V, 125C	Static	Dynamic	Total
internal reg power	4.99	111.5	116.5
memory power	5.91	33	38.91
other internal power	13.9	227	241
clock power	0.12	3.8	3.92
Total Power	24.92	375.3	400.33

Accurate

Power gating, Clock gating decisions

Power gating candidate

VECTORLESS SIM	TRUE LEAKAGE CORENER		
DSP Block 40nm	Static	Dynamic	Total
Sub block A	23.7	95.32	119.02
Sub block B	18.42	70.4	88.82
Sub block C	89	365.3	454.3

Clock gating candidate

VECTOR SIM	TRUE LEAKAGE CORENER		
DSP Block 40nm	Static	Dynamic	Total
FIR (Filter)	22.32	89.4	111.72
FFT	60	180	240
IIR (Filter)	30.4	100.2	130.6

Process node comparison

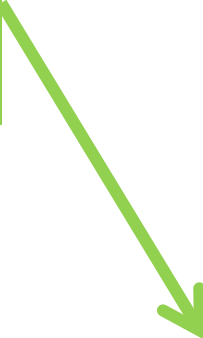
VECTORED SIM	TRUE LEAKAGE CORENER		
DSP Block 40nm - 0.88V, 125C	Static	Dynamic	Total
internal reg power	33.95	183.5	217.5
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40nm/
28nm

Architecture Selection

TRUE Leakage Corner			
DSP Block 40nm	Static	Dynamic	Total
FIR (Filter) - 2's complement format	22.32	89.4	111.72
FIR (Filter) - signed magnitude format	20.4	62.4	82.8

Select signed magnitude format



Architecture Selection - continue

TRUE Leakage Corner			
DSP Block 40nm	Static	Dynamic	Total
FIR (Filter) - data - 14 bits, coef - 10 bits	18.11	42.12	60.23
FIR (Filter) - data - 11 bits, coef - 9 bits	12.08	30.23	42.31

Select lower precision

Voltage Selection

28nm Netlists	Power in mW		
	Static	Dynamic	Total
True Lkg			
0.75V	84.3	250	335
0.85V	76.9	294	371
Diff (%)	-9.62	14.97	9.7

Stay with 0.85V
 Sacrifice 10% power
 Ease of timing closure



What we learned from actual power measurements in lab ?

- Power estimations for true leakage corner – worst case power
- Power estimations for typical corner – optimistic power

Summary

- Vectorless simulations – faster early estimates but less accurate dynamic power
- Vectored simulations – More accurate estimates but available late in the design cycle
- Actual power measured in lab correlates well with estimated power
- Useful data for power gating, clock gating, architecture tradeoffs, process node selection and package design decisions.
- Overall, it helped achieve our low power chip requirements