2014 DESIGN AND VERIFICATION DVCON CONFERENCE AND EXHIBITION EUROPE

Power-Aware Verification in Mixed-Signal Simulation

Atul Pandey[1], Mattias Welponer[2], Gregor Kowalczyk[2]
[1] *Mentor Graphics (Deutschland) Gmbh, Munich, Germany*, atul_pandey@mentor.com
[2] *Infineon Technologies Austria AG, Graz, Austria*
{mattias.welponer,gregor.kowalczyk}@infineon.com

Abstract— Power efficiency is a very important metric in designing mobile and other industrial SoCs. Various power saving techniques are used to reduce power consumption. To verify the power distribution network and power state transitions in SoC designs, power-aware verification is performed with the power architecture described in UPF. Many of those SoCs are mixed-signal in nature and have power-regulation functionality on the chip. Verifying such designs with mixed-signal simulation in power-aware mode complements digital verification by producing accurate results for the power management and analog units of a design. In this paper we present the basic concepts of power-aware verification in mixed-signal simulation and apply them to verify a tire pressure monitoring system SoC.

Keywords— Unified power Format (UPF), Power-Aware Verification, SoC, Mixed-Signal Verification, Power Management Unit (PMU), Boundary elements

I. INTRODUCTION

Scaling of process technology has enabled integration of more functionality on single chip. This trend has enabled the design of System on Chips (SoC) with ever increasing functional complexity. Portable and mobile devices have been key driver in the growing number of SoCs. Most of these SoCs consist of digital and analog/RF functional blocks interconnected to perform functions including data acquisition and processing, voltage generation and regulation, µCore to control various internal operations and multiple standard protocol support. Even non-portable systems must avoid wasting energy in order to minimize both power and cooling costs. Low power design is also driven by government and industry initiatives such as Energy Star, Green touch and the green grid to reduce global energy consumption. Such devices must have long battery life and therefore must minimize power consumption. This requires application and control of power reduction techniques to minimize power consumption.

The power consumption of a design consists of two components, dynamic (switching) and static power (leakage). In lower geometry designs static power can be up to or greater than 50% of total power consumption [1]. Active power management is required in low power designs to ensure energy efficiency. There are many techniques that have been developed to address the continuously aggressive power reduction requirements of SoC designs. They include clock gating, multi-switching (multi-Vt) threshold transistors, multi-supply multi voltage (MSMV), power gating with or without state retention, dynamic voltage and frequency scaling (DVFS), and substrate biasing. To further reduce power consumption, low power designs manage power actively by devising multiple operating modes as well as multiple power domains associated with different voltage levels which may be varied dynamically based on the operating state.

Active power management enables the design of low power chips and systems but also creates many new verification challenges. Verification of such designs requires exercising design functions that also cover all power modes and state transitions ensuring that state retention, isolation, voltage level-shifting and power-on and power shutoff are handled properly in the design. The power management architecture and power intent verification has been standardized on the IEEE Std 1801 Unified Power Format (UPF) [2] for specification of active power management. Power-aware verification allows designers to functionally verify their power management techniques at the RTL level hence reducing costs significantly in terms of effort and time.

Most mixed-signal SoCs have on-chip power generation and management blocks. The power generation blocks consist of voltage regulators and control signals. Circuits involved in power management function are analog in nature. Such functional blocks as voltage regulators and power switches are designed and verified using analog flow consisting of schematic capture and SPICE simulation tools. Power-aware verification has

traditionally been applied to digital verification methods using RTL and UPF description. Analog effects of power management blocks are not considered in such a verification environment. This often results in incomplete verification of power intent in low-power designs and leads to errors related to power distribution network signal connectivity and incomplete verification of power states. Mixed-signal verification enables verification of digital and analog specifications along with connectivity at the interfaces.

This paper will describe concept which enables extension of digital power-aware verification to mixed-signal verification. Section II will describe concept of electrical-to-power (E2P) and power-to-electrical (P2E) boundary interactions between UPF and analog ports and how power intent information is used in logic connectivity between digital and analog ports. Section III will present the application of the above concepts to verify a tire pressure monitoring SoC. In section IV results achieved and a summary will be presented.

II. Extending UPF based power-aware verification to mixed-signal verification

Power architecture is defined for low-power designs that partitions the design into functional units and determines which power-saving techniques are used by different design components. UPF provides the necessary notation to capture power intent and is used by functional verification as well as implementation tools. The concepts and constructs of power-aware verification using UPF has been presented in detail at the verification academy website [3]. The Designs implementing power saving techniques such as multi-voltage and DVFS technique etc have a power management unit (PMU) that generates and regulates different voltage states required for the design functions. The voltage regulation function is analog in nature and is designed by analog designers using an analog design and verification environment. The voltages generated by these on-chip regulators are the source for primary power/ground of power domains in power architecture. The power supply for some analog units of the design may also be controlled through a power network described in UPF to reduce power consumption in powerdown or standby mode. To ensure design robustness and increase verification coverage of the design it is imperative to perform mixed-signal power-aware verification incorporating UPF and analog models. Power-aware verification using UPF augments digital design (RTL) verification which doesn't include a notion of power. In contrast, the analog portion of the design is described by a SPICE netlist along with mixed-signal languages such as VHDL-AMS and Verilog-AMS and it requires an explicit declaration of power supply and control. Electrical models are fundamentally dependent on appropriate power for correct operation. Mixed-signal power-aware verification requires that the analog power supplies must be synchronized with the power state of the UPF power domain. UPF is a standard description used in functional verification as well as by implementation tools hence mixed-signal power-aware verification environment shall reuse the standard UPF constructs.

In mixed-signal power-aware verification, connectivity of power ports of analog electrical models and UPF power signals has to be done in such a way that the power management architecture is consistent between the analog and digital portion of the design and the information flow between analog and UPF/digital domains is consistent. Figure 1 shows important components of a power-aware mixed-signal verification environment.

1. The standard methods used in digital verification for capturing power intent are supported. The power-management architecture created in UPF for the digital verification environment is reused in mixed-signal verification.
2. The mixed-signal verification tool elaborates the analog-UPF boundary and inserts appropriate boundary connect elements (interface elements), power-to-electrical (P2E) and electrical-to-power (E2P).
3. Analog power supplies connected to UPF ports are in sync with the state of power in the UPF hierarchy. The mechanism to turn-on/off power domain is extended to the boundary connect elements.
4. The logic signal boundary connect elements, which are at the boundary of analog-digital for logic signals, derive the voltage level information from the state of primary power and ground of the power domain to which the logic signal belong (auto-calibrated or power sensitive boundary elements).

The above features of mixed-signal power-aware verification are explained in detail in publication in reference [4]. P2E and E2P boundary elements perform conversion of power signal state and value between analog and UPF domain. Auto-calibrated logic boundary connect elements use the state of primary power/ground

of power domain to which the logic signals belong and pass appropriate information across boundary. When power domain of the signal is OFF digital signal is represented as "X" and appropriate value is propagated to analog side.

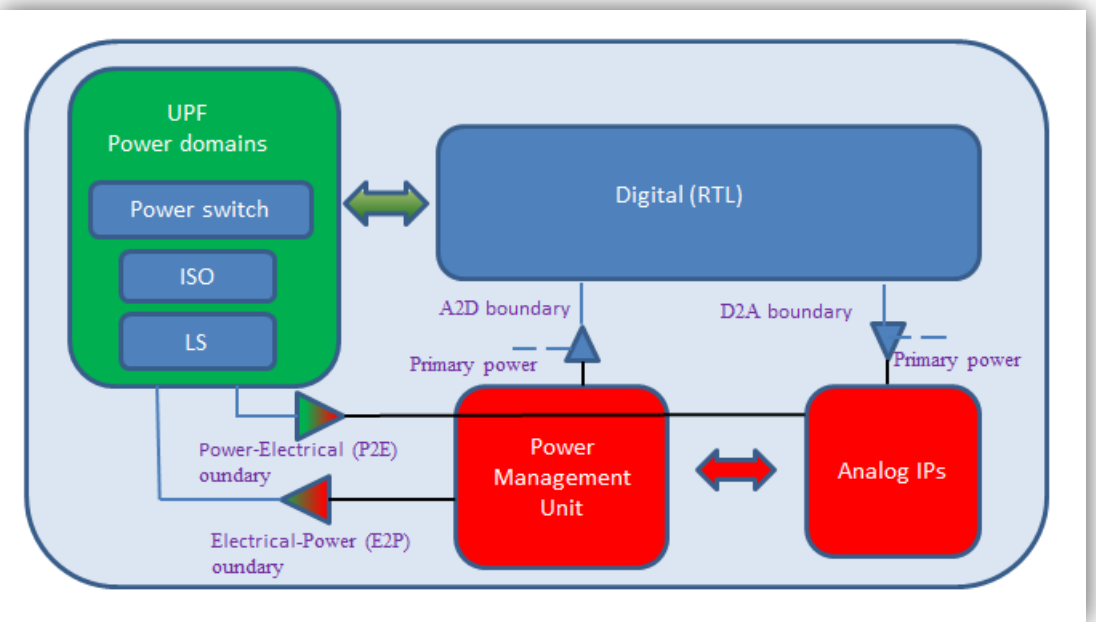

Figure 1: Power-aware mixed-signal verification

III. POWER-AWARE MIXED-SIGNAL VERIFICATION FOR A TIRE PRESSURE MONITORING SYSTEM CHIP

Power-aware mixed-signal verification is applied to a tire pressure monitoring system (TPMS). The design and its power architecture are represented in an abstract form in figure 2. The product has 10

power domains and multiple operating modes and power states such as low-frequency (LF), low and ultra low power (LP/ULP), high performance (HP), power down (PD) and standby modes.The power consumption ranges from few hundred nanoAmp in PD mode to many microAmps in HP mode.

UPF has been in use in this design primarily for physical implementation (synthesis and Place and Route) of the digital part of the design.As it is evident in figure 2, the design has onchip voltage regulators that generate and regulate voltage levels in the range of 1 to 5 volts These voltages form primary power to the power domains in UPF.

A. Former approach to verify power states

The mixed-signal verification of this design is setup as Analog-on-Top (schematic driven). In the previous mixed-signal verification flow, the power distribution and power state was emulated by creating power-conversion models in the verification environment. The power conversion unit would send either a „X" or valid logic signal based on value of the voltages from PMU. The voltage port in this model is of real number data type and connected to analog power ports. This power-conversion model is not part of the design. As shown in figure 3, the digital part of the design was wrapped in a model and all the digital signals were interfaced to analog portion via power-conversion model instances. As usual in mixed-signal verification boundary elements are inserted at the boundary of analog and digital nets.

This approach required a lot of manual changes to the netlist. Inserting power conversion model instances based on appropriate power domain and logic signals is tedious and may not correspond to power distribution network of UPF. It is possible to test PSD, power-on and to some extent DVFS states but a check for correct level shifting, isolation and retention cell placement is not possible.

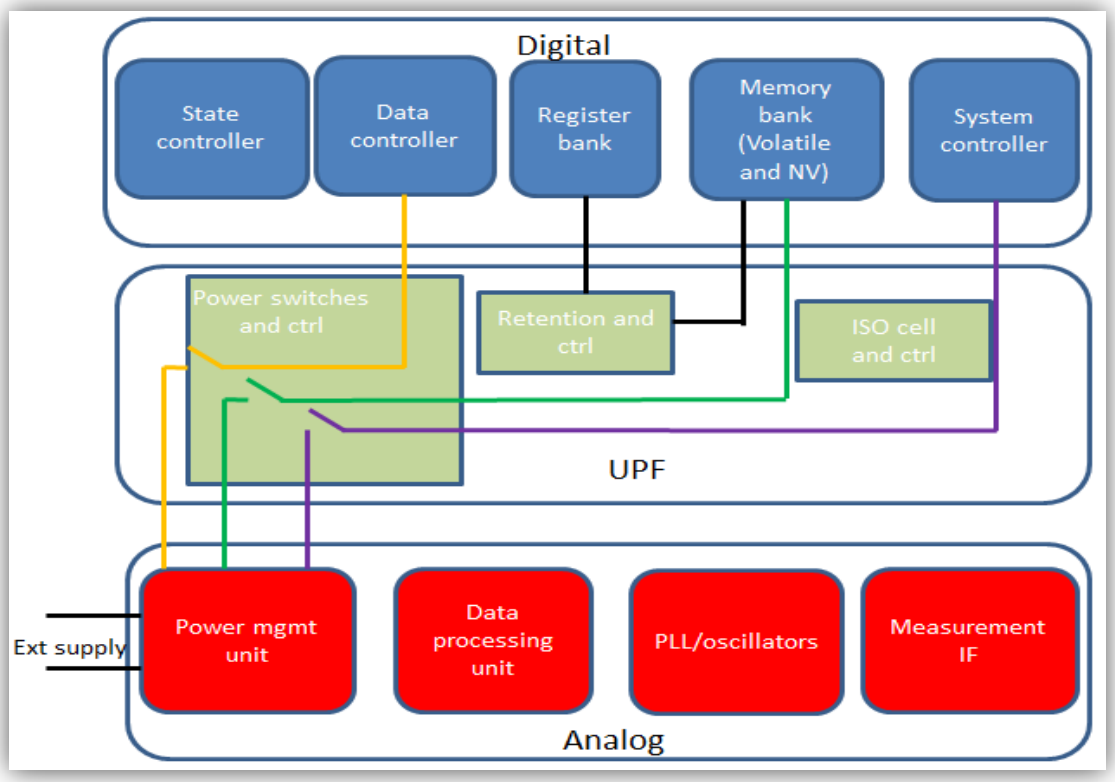

Figure 2: Design blocks of TPMS design

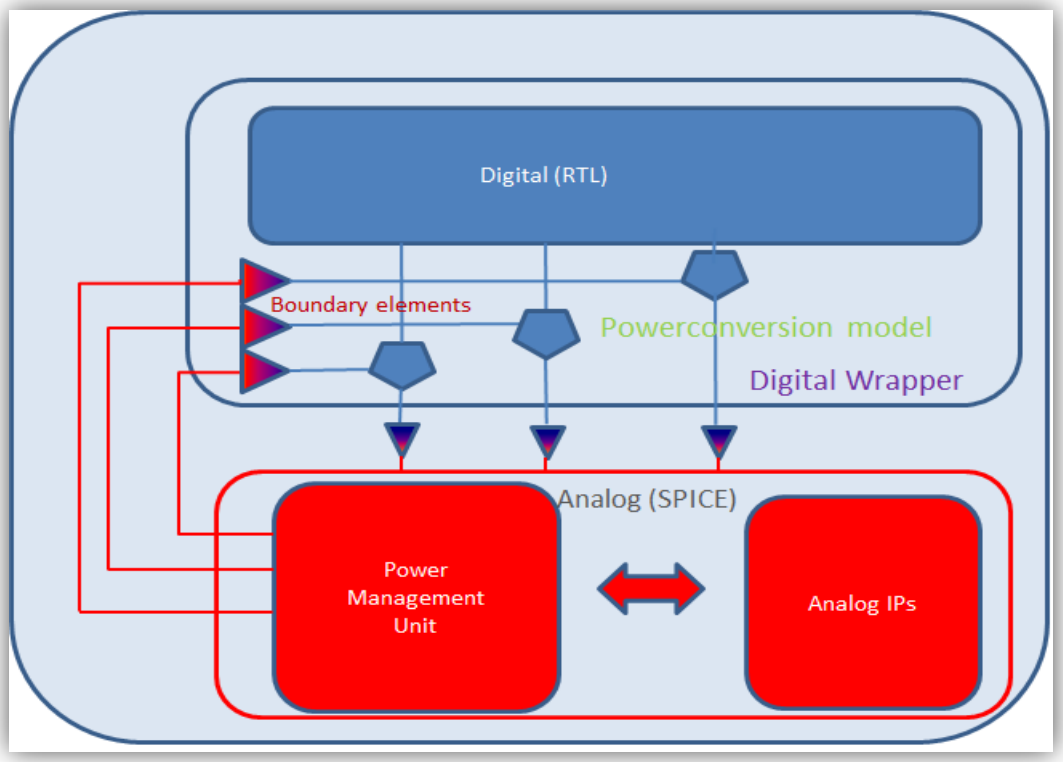

Figure 3: Previous power-aware mixed-signal verification setup

B. Power-aware mixed-signal verification

To overcome the above limitations and to make the flow compatible to a digital verification flow, the power-aware mixed-signal verification is setup for the design using the Mentor Graphics QuestaADMS® [5] simulator. QuestaADMS® supports UPF version 1.0 and 2.0 . The simulator inserts boundary elements between UPF and analog ports (power-to-electrical as well as electrical-to-power) so that the power state and value is in sync between analog and digital domains. To facilitate verification of DVFS states of design, the logic boundary elements (A2D and D2A) have been enhanced to incorporate primary power and ground port state and the value of the power domain logical signal belongs to. Figure 4 shows behavior of auto-calibrated (or power-aware) logical boundary elements. When primary power/gnd of power domain is in "OFF" state the digital signal value is "X" and analog value is a predefined value. When primary power of power domain the signal belongs to is in "ON" state the analog signal takes value of the primary power for digital value of "1" and primary ground value for "0", the threshold for A2D boundary elements are set according to the primary power/gnd .If value of primary power/gnd changes (for ex: from 3.0 volt to 4.5 volt) thresholds of A2D boundary elements and VHI/VLO corresponding to digital value of "1"/"0" are changed automatically to reflect changes in power supply on the logic signals.The connectivity to UPF ports in the design verification is setup by using a wrapper around RTL models but the difference with respect to former approach is that the analog voltages are connected to UPF ports (supply_net_type) as shown in figure 5a. This setup corresponds to the setup of power-aware mixed-signal verification represented in figure 1. This setup eliminates the need for power conversion models as the power information is directly derived from UPF. The wrapper is required because we setup this verification flow as Analog-on-top. In Digital-on-top flow the power ports that are inherent in electrical models are connected to UPF power ports. The power ports in RTL of supply_net_type data type are connected to supply_net in UPF as shown in figure 5b. The boundary elements for E2P, P2E and logic signals are defined in a control file and insertion of the boundary elements is taken care of by the simulator. This setup makes mixed-signal simulation compatible with power-aware verification for this design.

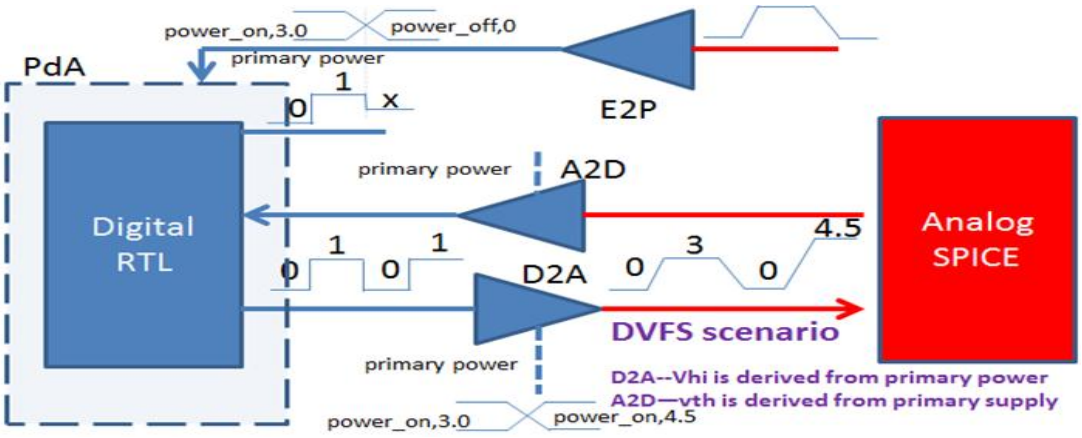

Figure 4 Power-Aware logical boundary element behavior

```
library IEEE;
use ieee.std_logic_1164.all;
use ieee.upf.all;

entity dcore_wrapper is
port (
--
pwr1v5  : in supply_net_type    := (OFF,(others=>'0')) ;
pwr2v0  : in supply_net_type    := (OFF,(others=>'0')) ;
pwr3v0  : in supply_net_type    := (OFF,(others=>'0')) ;
gnd1    : in supply_net_type    := (OFF,(others=>'0')) ;

        d1v5    : in std_logic;
        d2v0    : in std_logic;
        por     : in std_logic;
        sel     : in std_logic_vector (1 downto 0);
        en1v5   : out std_logic ;
        en2v0   : out std_logic;
        en3v0   : out std_logic;
        out_1v5   : out std_logic;
        out_2v0   : out std_logic
```

Figure 5a: mechanism to connect analog power supply to UPF supply_net

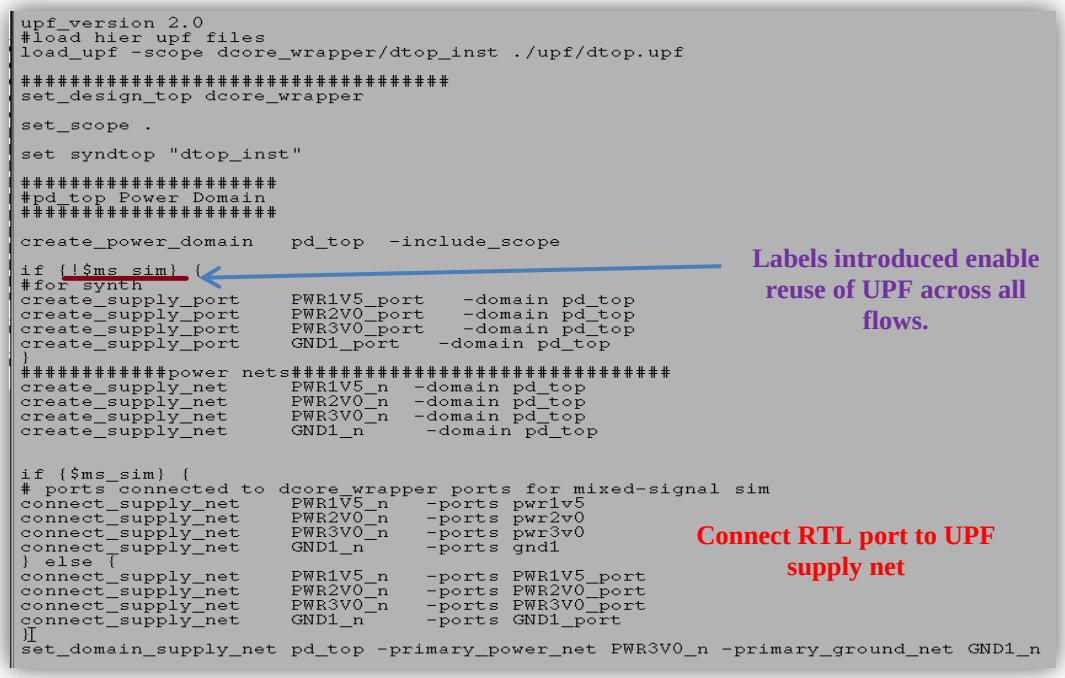

Figure 5b: Snapshot of UPF file

Some of the power switch used in power network for this design are custom designed and voltage switching and control sequence timing on them required accurate verification. SPICE netlist for custom power switches were used to achieve required simulation accuracy. A mechanism based on labels depending on flow type (digital power-aware, mixed-signal power-aware or synthesis) was introduced in UPF file (figure 5b). This enabled use of SPICE description for custom power switches for desired mixed-signal test scenario and using UPF description in other test scenarios. The output of custom switches in SPICE is connected to UPF power nets that are outputs of power switches. However, analog domain signal only have power net value information but no power state information. The power net state was derived by using E2P boundary element shown in figure 6. In the boundary element model, value of parameters “von” and “voff” are specified depending on power domain of custom power switch output. Correct power state for power switch outputs are generated by the E2P boundary element.

```
Library ieee;
  use ieee.electrical_systems.all;
  use ieee.upf.all;

entity E2P is
  generic (voff : real := 0.2;
           von  : real := 0.5;
           eps  : real := 1.0e-3);

  port (signal upfout : out supply_net_type;
        terminal vdd, vss : electrical);
end entity E2P;

architecture ams of E2P is

  quantity vds across vdd to vss;

  signal sds : real := 0.0;

  begin

    upf : process(vds'above(sds+eps),vds'above(sds-eps))
      variable returnSupply : boolean;
    begin
      sds <= vds;
      if sds < voff then
        returnSupply := supply_off("upfout");
      elsif sds > von then
        returnSupply := supply_on("upfout",vds);
      else
        returnSupply := supply_partial_on("upfout",vds);
      end if;
    end process upf;

end architecture ams;
```

Figure 6: Electrical to power boundary element

Power-aware mixed-signal verification was performed for this design for multiple functional and power state transition scenarios using the methods described above. Figure 7 shows an example test scenario in which design transitions from high performance state to power shut off and then to one of the low power states. Three of the primary power nets of associated power domains in the design are represented on the top portion of the figure. Logic signals (ex: xtoplevel_u:ydcore_u:en2v0) can be seen as "X" when power domain (PWR3V0), the logic signal belongs to, is OFF and valid logic value when state is ON. In the low power mode, voltage regulators regulates to lower voltage levels and hence supply nets in UPF has lower voltage value and the effect is that the boundary signals driven from digital to analog side (ex: xtop:xtoplevel_u:dout_1v5) through boundary elements also have scaled down voltage (from 1.4 to 0.9 volts).

One of the problems discussed earlier with previous approach was the inability to verify whether correct levelshifter units were inserted at signal crossings from one power domain to another as well as whether isolation and retention behaviour was as expected. In power-aware mixed-signal verification such checks are enabled just as in digital power-aware simulation and displayed in simulation logfiles. Writing assertions for such checks is also possible though not used in this project. Figure 8 shows example of messages in the simulation logfile which helpto debug the power distribution network.

The messages in figure 8 are status info of power domains, isolation/retention control and power switch state at certain times during simulation. Further, this approach can be extended to unified coverage driven verification [6],[7] by creating testplan and merging the simulation results.

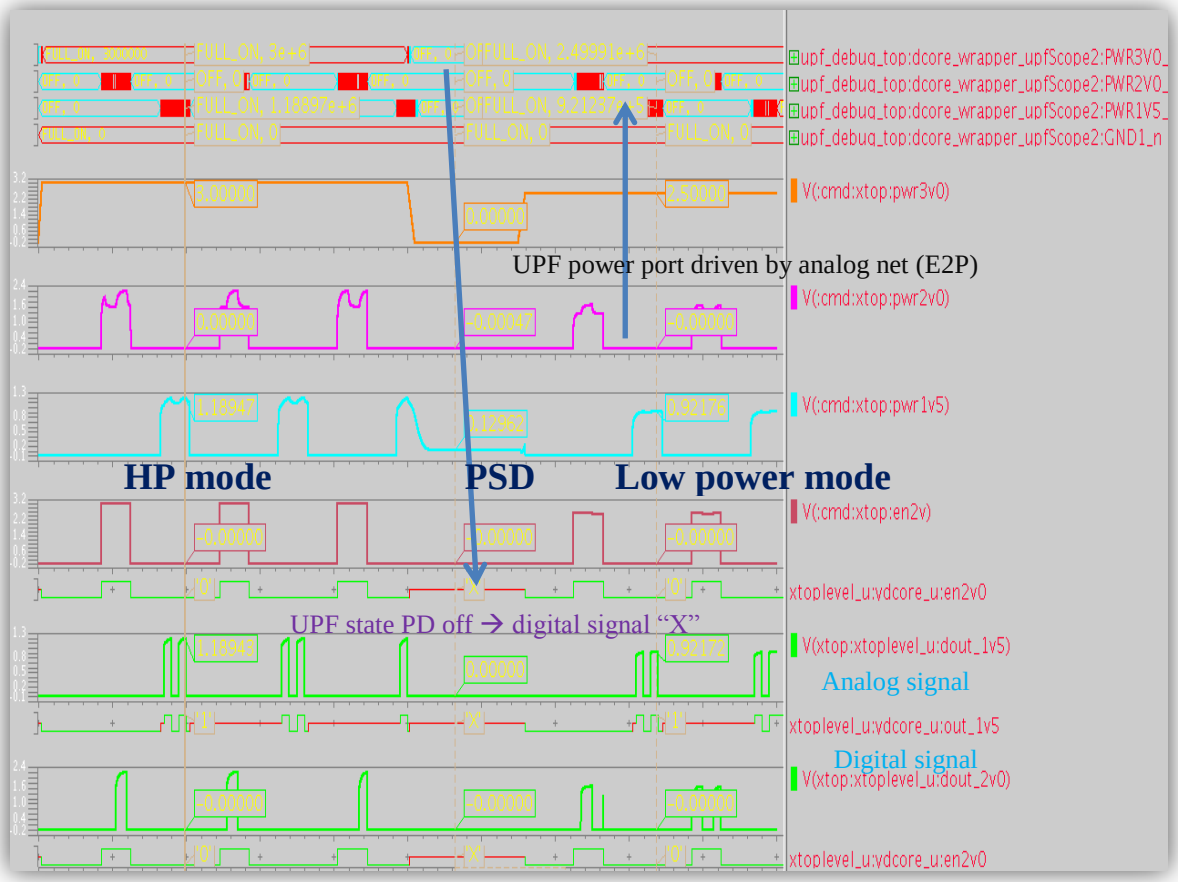

Figure 7: Modes of operation and state of analog and digital signals

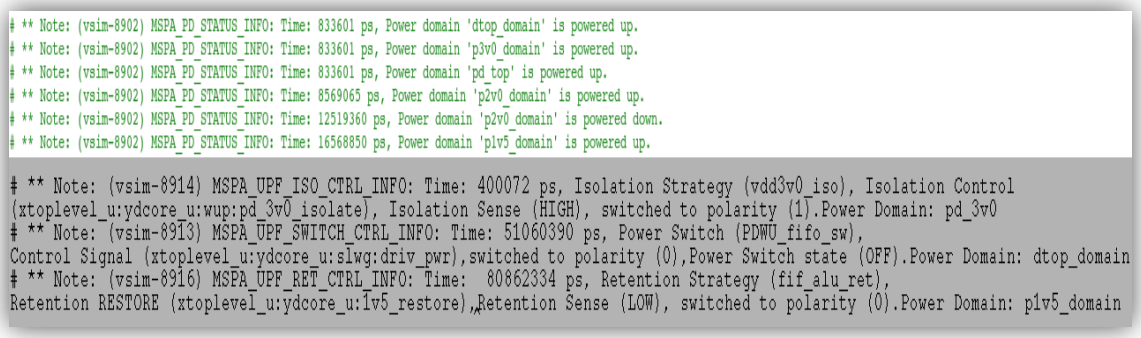

Figure 8: power-aware checks available in Mixed-Signal simulation

IV. RESULTS AND CONCLUSION

Power-aware mixed-signal verification for a TPMS design was used to verify the robustness of the power distribution network and the power state transitions in concert with functional specifications. This methodology achieves faster verification performance, higher accuracy for analog design units and enables verification of power architecture, power state and transition. It enabled accurate simulation of behavior of the voltage regulator outputs connected to power network along with other analog functional units. Types of errors found by mixed-signal simulation were power-blackout, incorrect power-up/down sequence, missing levelshifters, incorrect polarity applied in isolation cell insertion (iso-control and iso-clamp values).Early verification using UPF,RTL and SPICE netlist could be done without waiting for gate-level implementation. The methods used in this project will be further used in other projects with Digital-on-top mixed-signal setup as concepts are equally applicable.

V. REFERENCES

[1] Stefan Rusu, Trends and Challenges in High Performance Microprocessor Design, **Electronic Design Process Symposium,** 2004.

[2] Institute of Electronic and Electrical Engineers, The IEEE Standard for Design and Verification of Low Power Integrated Circuits (IEEE Std1801-2009), 2009.

[3] https://verificationacademy.com/courses/power-aware-verification

[4] Ken Bakalar, Eric Jeandeau, Interpreting UPF for a Mixed-signal design under test, DVCon 2014.

[5] Questa ADMS User's Guide *online*, www.supportnet.mentor.com

[6] Unified Coverage Interoperability Standard : http://www.accellera.org/activities/committees/ucis

[7] Atul Pandey, Guido Clemens, Marius Sida, Coverage-Driven Verification for Analog Design Based on UCIS, Design Automation conference 2013