Power-Aware Verification in Mixed-Signal Simulation

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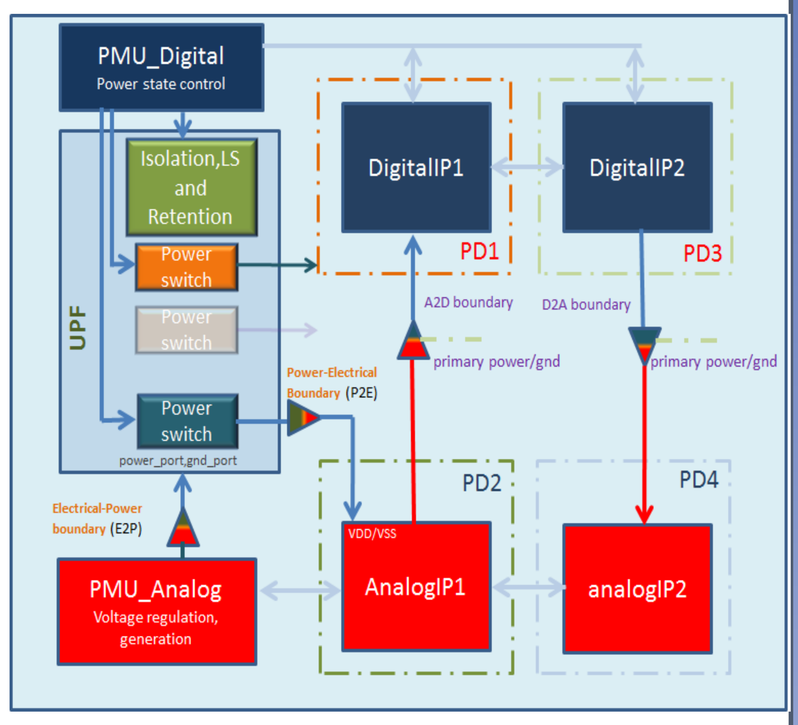
Overview

- Power efficiency is key metric for mobile and industrial SoCs
- Active power management techniques are used to ensure low power consumption
- Power management architecture and intent is captured in UPF format and verified by Power-Aware (PA) verification
- Mixed-signal(MS) SoCs have on-chip power generation and management units
- PA verification extended to Mixed-Signal verification to increase verification coverage

Power Aware MS verification

- Reuse digital PA verification flow
- Analog-UPF boundary is connected through appropriate boundary connect elements (interface elements), power-to-electrical (P2E) and electrical-to-power (E2P)
- Analog power supplies are in sync with the state of power in the UPF hierarchy.
- The logic signal boundary elements derive voltage information from the state of primary power and ground of the power domain to which the logic signal belong

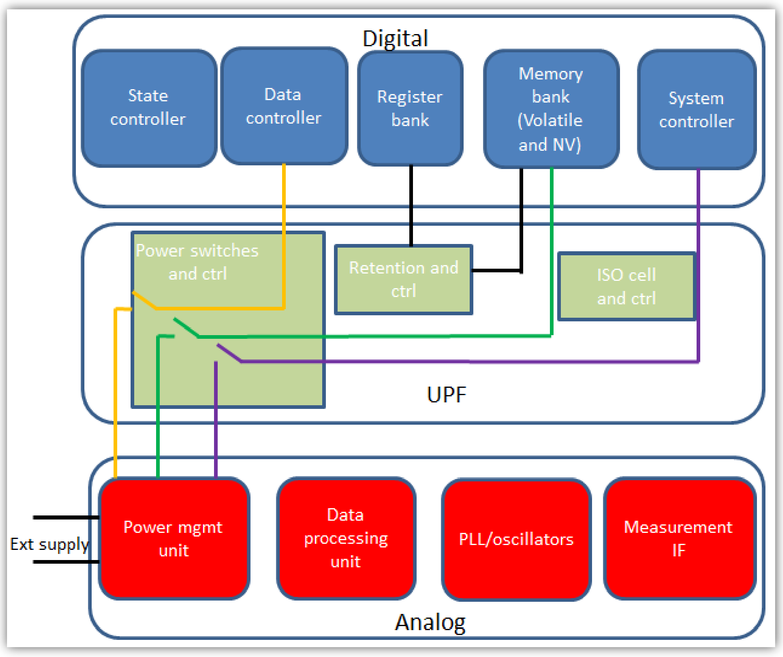
Power-Aware MS verification



MSPA verification for TPMS design

- MSPA verification is implemented for a Tire Pressure Measurement System (TPMS)
- The TPMS product has 9 power domains
- Has multiple operating modes and power states such as LF, LP/ULP, HP,PD and standby modes
- The power consumption ranges from few hundred nanoAmp in PD mode to many microAmps in HP mode
- UPF description used for power architecture definition of digital design

TPMS Design description



Power network and state verification

- Analog-on-Top MS verification environment derived from previous MS verification flow is re-used.
- Tests during MSPA verification verified power modes and state transitions covering state retention, isolation, voltage level-shifting and power-on and power shutoff scenarios
- SPICE netlist is used for custom power switches in power architecture to increase verification accuracy for few testscenarios.

Connectivity Mechanism

Power port connectivity to digital model

```
library IEEE;
use ieee.std_logic_1164.all;
use ieee.upf.all;

entity dcore_wrapper is
port (
--
pwr1v5 : in supply_net_type    := (OFF,(others=>'0')) ;
pwr2v0 : in supply_net_type    := (OFF,(others=>'0')) ;
pwr3v0 : in supply_net_type    := (OFF,(others=>'0')) ;
gnd1   : in supply_net_type    := (OFF,(others=>'0')) ;

        d1v5    : in std_logic;
        d2v0    : in std_logic;
        por     : in std_logic;
        sel     : in std_logic_vector (1 downto 0);
        en1v5   : out std_logic ;
        en2v0   : out std_logic;
        en3v0   : out std_logic;
        out_1v5  : out std_logic;
        out_2v0  : out std_logic
```

```
upf_version 2.0
#load hier upf files
load_upf -scope dcore_wrapper/dtop_inst ./upf/dtop.upf

#####################################
set_design_top dcore_wrapper

set_scope .

set syndtop "dtop_inst"

#####################
#pd_top Power Domain
#####################

create_power_domain   pd_top  -include_scope

if {$ms_sim} {
#for synth
create_supply_port     PWR1V5_port    -domain pd_top
create_supply_port     PWR2V0_port    -domain pd_top
create_supply_port     PWR3V0_port    -domain pd_top
create_supply_port     GND1_port    -domain pd_top
}
############power nets#################################
create_supply_net      PWR1V5_n   -domain pd_top
create_supply_net      PWR2V0_n   -domain pd_top
create_supply_net      PWR3V0_n   -domain pd_top
create_supply_net      GND1_n     -domain pd_top


if {$ms_sim} {
# ports connected to dcore_wrapper ports for mixed-signal sim
connect_supply_net     PWR1V5_n   -ports pwr1v5
connect_supply_net     PWR2V0_n   -ports pwr2v0
connect_supply_net     PWR3V0_n   -ports pwr3v0
connect_supply_net     GND1_n     -ports gnd1
} else {
connect_supply_net     PWR1V5_n   -ports PWR1V5_port
connect_supply_net     PWR2V0_n   -ports PWR2V0_port
connect_supply_net     PWR3V0_n   -ports PWR3V0_port
connect_supply_net     GND1_n     -ports GND1_port
}
set_domain_supply_net pd_top -primary_power_net PWR3V0_n -primary_ground_net GND1_n
```

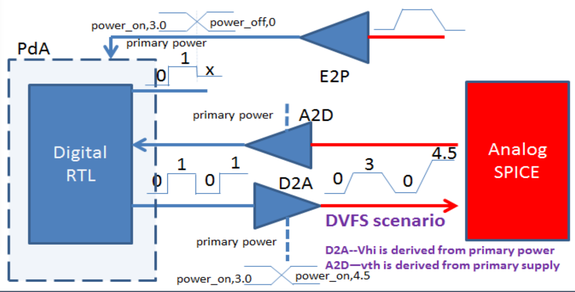
Labels introduced enable reuse of UPF across all flows

Connect RTL port to UPF supply net

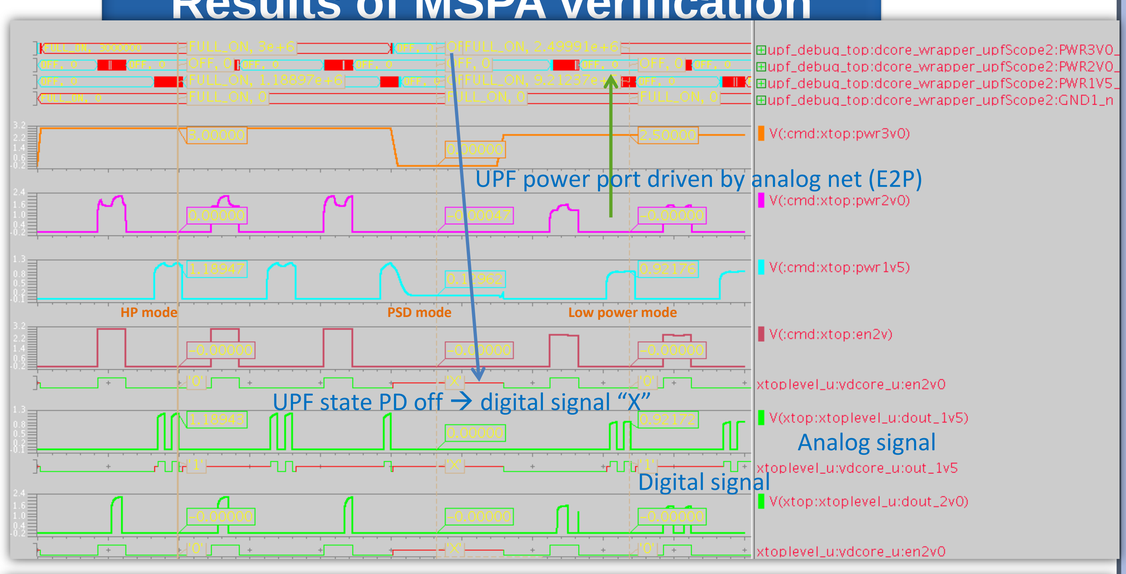
An example E2P

```
Library ieee;
use ieee.electrical_systems.all;
use ieee.upf.all;
entity E2P is
  generic (voff : real := 0.2;
           von  : real := 0.5;
           eps  : real := 1.0e-3);

  port (signal upfout : out supply_net_type;
        terminal vdd, vss : electrical);
end entity E2P;
architecture ams of E2P is

  quantity vds across vdd to vss;

  signal sds : real := 0.0;

  begin

    upf : process(vds'above(sds+eps),vds'above(sds-eps))
      variable returnSupply : boolean;
    begin
      sds <= vds;
      if sds < voff then
        returnSupply := supply_off("upfout");
      elsif sds > von then
        returnSupply := supply_on("upfout",vds);
      else
        returnSupply := supply_partial_on("upfout",vds);
      end if;
    end process upf;
end architecture ams;
```

Boundary element behavior



Results of MSPA verification




```
# ** Note: (vsim-8902) MSPA_PD_STATUS_INFO: Time: 833601 ps, Power domain 'dtop_domain' is powered up.
# ** Note: (vsim-8902) MSPA_PD_STATUS_INFO: Time: 833601 ps, Power domain 'p3v0_domain' is powered up.
# ** Note: (vsim-8902) MSPA_PD_STATUS_INFO: Time: 833601 ps, Power domain 'pd_top' is powered up.
# ** Note: (vsim-8902) MSPA_PD_STATUS_INFO: Time: 8569065 ps, Power domain 'p2v0_domain' is powered up.
# ** Note: (vsim-8902) MSPA_PD_STATUS_INFO: Time: 12519360 ps, Power domain 'p2v0_domain' is powered down.
# ** Note: (vsim-8902) MSPA_PD_STATUS_INFO: Time: 16568850 ps, Power domain 'p1v5_domain' is powered up.
```

Report of static checks on power distribution network and states.

```
# ** Note: (vsim-8914) MSPA_UPF_ISO_CTRL_INFO: Time: 400072 ps, Isolation Strategy (vdd3v0_iso), Isolation Control
(xtoplevel_u:ydcore_u:wup:pd_3v0_isolate), Isolation Sense (HIGH), switched to polarity (1).Power Domain: pd_3v0
# ** Note: (vsim-8913) MSPA_UPF_SWITCH_CTRL_INFO: Time: 51060390 ps, Power Switch (PDWU_fifo_sw),
Control Signal (xtoplevel_u:ydcore_u:slwg:driv_pwr),switched to polarity (0),Power Switch state (OFF).Power Domain: dtop_domain
# ** Note: (vsim-8916) MSPA_UPF_RET_CTRL_INFO: Time:  80862334 ps, Retention Strategy (fif_alu_ret),
Retention RESTORE (xtoplevel_u:ydcore_u:1v5_restore),Retention Sense (LOW), switched to polarity (0).Power Domain: p1v5_domain
```

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- Power network and states of a TPMS design is verified in Mixed-Signal environment to verify robustness of the power distribution network and the power state transitions in concert with functional specs
- Accurate and fast verification of power distribution network (UPF) connected to analog voltage generation unit along with other analog and digital functional units
- Early design verification using UPF,RTL and SPICE netlist can be done without waiting for gate-level implementation