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Power Aware CDC Verification of Dynamic Frequency and Voltage Scaling (DVFS) Artifacts

Mark Handover, Mentor Graphics Corporation, Newbury, UK (*Mark_Handover@mentor.com*)

Jonathan Lovett, Mentor Graphics Corporation, Newbury, UK (*Jonathan_Lovett@mentor.com*)

Kurt Takara, Mentor Graphics Corporation, Fremont, United States (*Kurt_Takara@mentor.com*)

***Abstract*— Reducing power consumption is essential to both mobile and data center applications, where lower power contributes to either longer battery life or savings in HVAC while minimally impacting performance. Traditional low power verification only validates the functional correctness of power control logic, but it does not validate the impact of power logic on multi-clock logic.**

Today, designers understand clock domain crossing (CDC) design and verification[1], but leading-edge design teams must incorporate low power techniques as part of their CDC analysis to detect CDC issues which are introduced as a result of the low power design approaches. First generation low power CDC analysis techniques[2] have been successful in identifying problems resulting from incorrect power control logic insertion, but the evolution of low power design techniques has resulted in new challenges which requires new design practices and new verification techniques. In this paper, we will discuss the effects of advanced low power design on CDC design and verification. Specifically, we will describe the new CDC issues caused by the addition of power control logic including isolation cells, retention cells, level shifters, and dynamic voltage scaling:

- **Metastability introduced by isolation and retention cells**
- **New asynchronous clock relationships created by voltage domains and power switches**

We will describe the resolution of these CDC issues by employing netlist analysis, assertions and formal verification:

- **Low power-based clock and reset analysis**
- **Identification of low-power CDC paths and synchronization structures**

Finally, we will illustrate these issues and solutions with real life Unified Power Format (UPF) [3] examples and designs.

Keywords—Design Verification, Verification, Clock Domain Crossing, CDC, Voltage Domain Crossing, VDC, Low Power, UPF, Isolation, Retention, Level Shifter, Voltage Domain, Successive Refinement, DVFS, Dynamic Voltage Frequency Scaling, Formal Analysis

I. INTRODUCTION

With the advances in low power design, new low power artifacts have been introduced that cannot be detected with traditional verification techniques and may cause clock domain crossing (CDC) issues in silicon. This paper explains the new low power CDC issues and the CDC and voltage domain crossing (VDC) verification techniques developed to verify low power designs.

Initially, CDC verification for low power designs was run at the gate-level. For larger designs, designers achieve greater efficiencies through abstraction. Here, the abstraction involves running power aware CDC analysis at the RTL instead of the gate-level. Power aware CDC verification at the RTL increases productivity by allowing designers to run the CDC analysis and fix CDC problems earlier in the design cycle to achieve time and resource savings. When designers run low power CDC verification at the gate-level, the CDC violations identified would require expensive, late-stage design modifications. In addition, running low power CDC verification at the RTL will allow architects to do what-if analysis by testing power architecture scenarios.

In this paper, we begin by discussing the low power challenges for CDC design and verification including dynamic frequency and voltage scaling (DVFS). The following section describes the low power CDC verification methods and how these methods address the low power issues. Finally, we review some application examples for low power DVFS CDC verification.

II. LOW POWER DESIGN CHALLENGES

For most designs, the power logic is not instantiated in the design, so the power intent is absent in the RTL and extracted from the Unified Power Format (UPF) file during synthesis. The UPF is the universal standard for specifying the power control logic and its design connections. This late implementation of the power intent information into the gate-level design may delay the start of power verification until after the gate-level representation is available. When a power-related CDC issue is found late in the design flow, the cost for fixing this bug is higher than if the bug was caught earlier in the design cycle.

Most design teams are aware of possible design problems that can be introduced by the power control logic implementation. Clock, reset, and CDC errors can occur when the power elements are incorrectly inserted in the clock tree, the reset tree or the CDC paths. These errors may result in incorrect functionality such as data loss or data corruption. In other cases, the power logic may cause setup-hold timing violations that result in metastability on registers. Register metastability results in unpredictable values and intermittent errors that may not be reproduced in simulation and are extremely difficult to debug in silicon. These intermittent metastability-induced errors may appear or disappear when the operating conditions such as temperature, voltage, or frequency change.

Advanced techniques such as dynamic frequency and voltage scaling are enabling better power efficiencies while maintaining optimal performance. These advance techniques are introducing new CDC artifacts into low power designs.

A. *Unified Power Format (UPF) and Successive Refinement*

The latest UPF standards, UPF 2.0 and UPF 2.1, introduce successive refinement which is a recent concept for low power design and verification. Successive refinement supports the System-on-Chip (SoC) design and verification flow by allowing the UPF file to be refined and updated as it travels from IP design to SoC design to SoC implementation to SoC place and route. The UPF will also be refined as it is updated to support both front-end tools such as verification tools as well as back-end tools such as physical implementation tools. Successive refinement also allows design tools, such as CDC verification tools, early access to power information that would only have been accessible later in the design flow with the UPF 1.0 standard. [3]

The power distribution network is a physical implementation feature that is added to the design late in the project cycle. In UPF 1.0, the power distribution network is defined by the power supply ports, nets, and switches and the power domains are connected directly to the power supply nets (See Fig. 1). In this case, the design and verification teams must wait to verify the effects of the voltage domains on their design until after the implementation team has specified the power distribution network architecture.

```
# Specify Supply Ports
create_supply_port  VDD1 -domain PD1
create_supply_port  VDD2 -domain PD2
create_supply_port  VSS -domain PD1

# Specify Supply Nets
create_supply_net  VDD1 -domain PD1
create_supply_net  VDD2 -domain PD2
create_supply_net  VSS -domain PD1
create_supply_net  VSS -domain PD2

# Connect Supply Nets to Ports
connect_supply_net VDD1 -ports VDD1
connect_supply_net VDD2 -ports VDD2
connect_supply_net VSS -ports VSS

# Declare primary power and ground nets for the power domains
set_domain_supply_net PD1 -primary_power_net VDD1 -primary_ground_net VSS
set_domain_supply_net PD2 -primary_power_net VDD2 -primary_ground_net VSS
```

Figure 1. UPF 1.0 for Power Distributed Network

In UPF 2.0 and UPF 2.1, a new power network grouping option, the power supply set, has been introduced. The new power grouping option allows design teams to specify power groups without defining the voltage group's power and ground ports and nets [3]. The power supply set does not require the definition of the power ports, nets,

and switches and their connection to the power domains. The power supply set allows designers to define and test the power distribution network earlier in the project cycle before the power distribution network has been implemented (See Fig. 2).

```
# Specify Supply Set
create_supply_set PRIMARY1
create_supply_set  PRIMARY2

# Declare primary power and ground nets for the power domains
associate_supply_set PRIMARY1 -handle PD1.primary
associate_supply_set PRIMARY2 -handle PD2.primary
```

Figure 2. UPF 2.1 for Power Distributed Network

B. Isolation and Retention Cells

Isolation and retention cells are examples of power logic described in the UPF files that may introduce new CDC paths into designs.

An isolation cell will introduce a new path from the isolation enable signal to the destination register and in doing so, may introduce a new CDC path between the enable signal and the destination register (see Fig. 3). If the isolation enable signal is in a clock domain that is asynchronous to the destination register's clock domain, the assertion and deassertion of the isolation cell enable may cause an asynchronous edge at the receive register. The asynchronous isolation enable may violate the setup-hold timing requirements at the receive register and cause the register to go metastable. When a missing synchronizer is detected, designers will correct the power control logic by synchronizing the isolation enable signal to the destination register's clock domain.

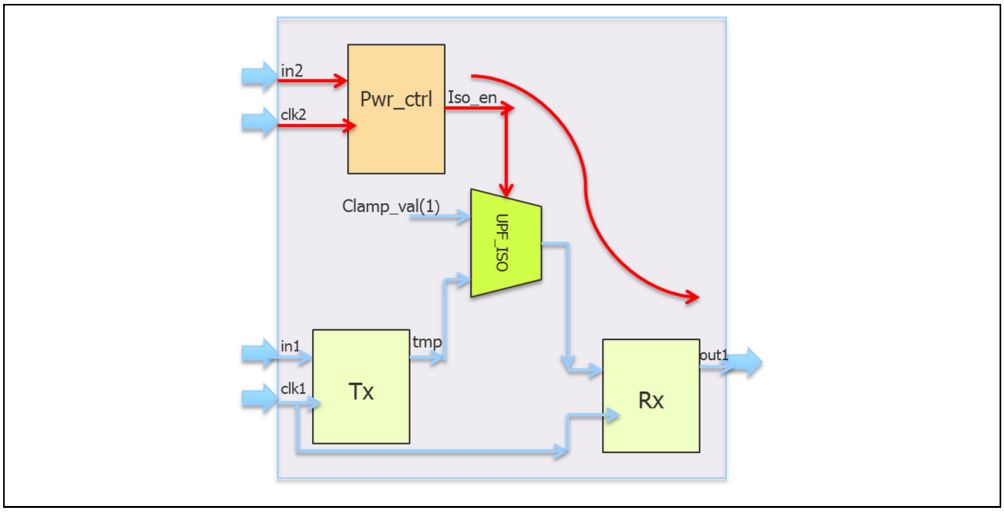

Figure 3. Isolation cell introduces a CDC path between synchronous registers

On properly synchronized CDC paths, isolation cells may introduce glitches and increase the occurrence of metastability that would reduce the reliability and mean-time-between-failures (MTBF) of these CDC paths (see Fig. 4).

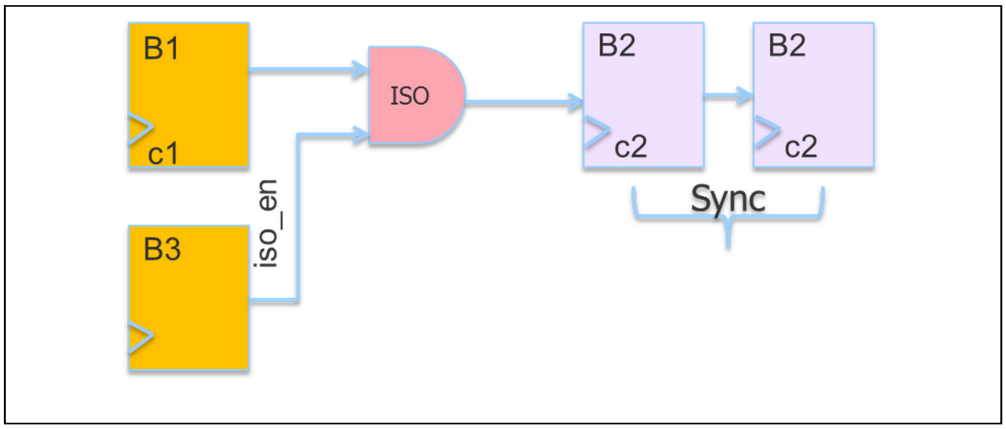

Figure 4. Isolation cell introduces a combinational logic violation

Design teams were not previously concerned about CDC crossings to and from retention cells, because they believed that the save and restore protocol protected the retention logic from adverse effects due to metastability. Now, design teams are also concerned about CDC crossings involving both isolation and retention cells. The save and restore pins on retention cells may create new CDC paths (Fig. 5). Designers must ensure that the save and restore logic is properly synchronized before use on retention cells.

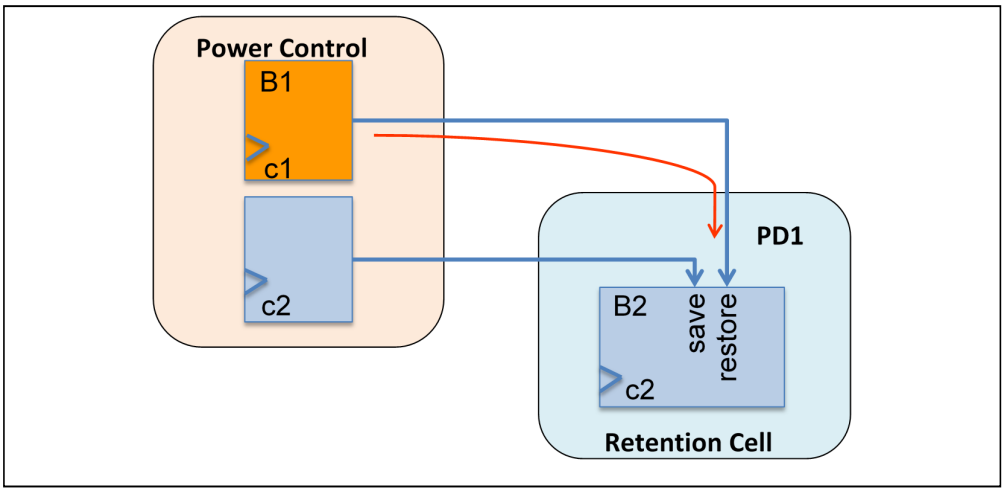

Figure 5. Retention cell introduces a CDC path to its restore pin

C. Dynamic Voltage and Frequency Scaling (DVFS)

Design teams are constantly deploying new techniques for low power design and sometimes these techniques may adversely affect design logic. One such case that has affected CDC design is the presence of dynamic voltage scaling. Advanced low power designs take advantage of dynamic voltage frequency scaling to further improve power savings while maximizing performance. By reducing the voltage and/or frequency, designs can reduce power consumption and heat dissipation when performance is not needed.

The maximum operating frequency is dependent on the voltage and requires a minimum voltage. When a design does not require performance, the frequency and voltage may both be reduced. The reduction in the voltage of a power domain results in a reduction in power consumption for that domain. Research has shown that in processor designs, energy consumption is proportional to the square of the supply voltage as described by equation (1). Therefore, small voltage reductions will lead to large power savings.

$$E \alpha V^2 \quad (1)$$

(Burd and Broderson 1995)

Initially, implementation teams were not aware of the effects of DVFS on clocks and clock trees. Design teams have found new metastability issues in designs that implement DVFS techniques. After long and painful debug sessions in the lab, designers have found metastability issues between registers in the same synchronous clock group. Further exploration has found that paths to or from variable voltage domains behave the same way as paths to or from asynchronous clock domains. The conclusion is that synchronous clocks on a variable voltage domain do not have a synchronous relationship with other clocks in the design and these clocks should be treated as new asynchronous clocks. As the voltage level for a specific voltage domain changes, the clock in that voltage domain does not maintain a deterministic phase relationship to the synchronous clocks in other variable voltage groups. Every control and data signal that runs to or from DVFS voltage domains must now be considered CDC paths including signals between synchronous registers (See Fig. 6).

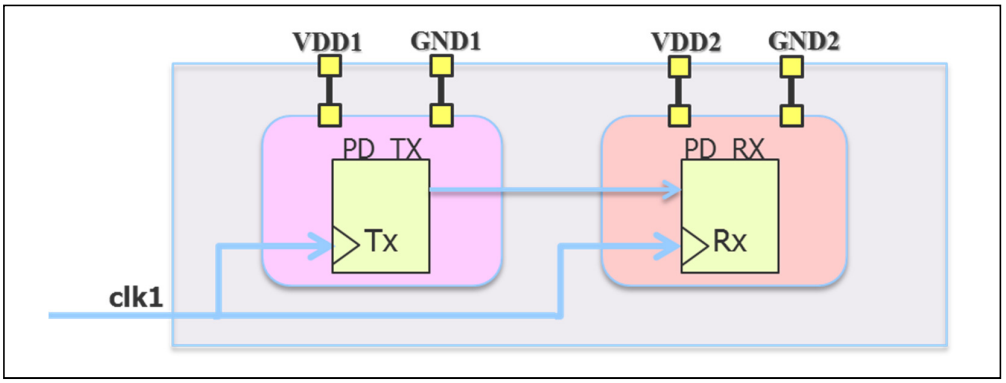

Figure 6. Synchronous registers on different voltage domains considered new CDC path

Previously, design teams only inserted level shifters on paths between voltage domains. The realization that the synchronous clocks behave asynchronously between variable voltage domains means that CDC synchronizers must be added on the receiver side of the data transfer between these voltage domains (See Fig 7).

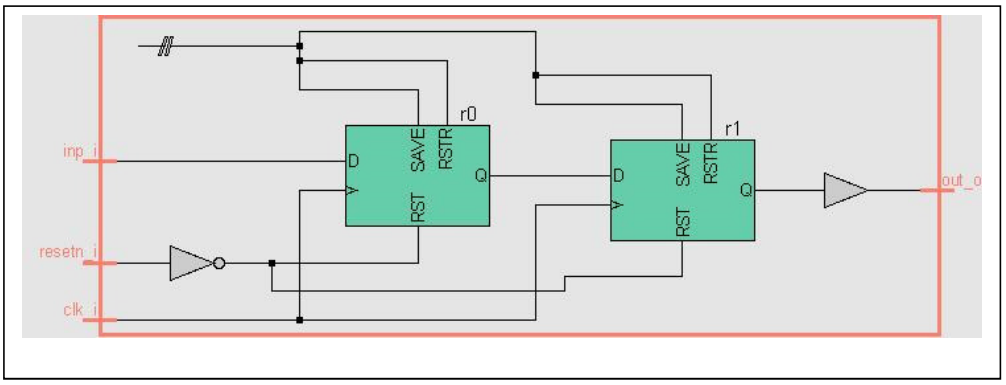

Figure 7. Retention synchronizer for VDC paths

Design teams are aware of these ways that low power design can adversely affect design logic and recognize that advanced low power CDC solutions are required to verify their designs. New CDC design and verification capabilities and methodologies are now being deployed for designs to avoid low power artifacts in silicon.

III. LOW POWER CDC VERIFICATION

Traditional CDC verification involves understanding the clocks, clock trees, and CDC paths in a design. Power aware CDC verification involves understanding how the power domains and power control logic affect the clocks,

clock trees, and CDC paths. Similar to low power design, low power CDC verification has evolved to support the latest design techniques such as DVFS.

A. Basic Low Power CDC Verification

Basic power aware CDC analysis compiles the UPF and adds the power elements to the RTL design. Initially, only paths involving isolation cells were analyzed for CDC errors. The isolation cells are modeled as combinational logic and may create combinational logic or missing synchronizer violations. Power aware CDC tools operate on the RTL design and UPF and would detect combinational logic violations and new CDC paths created between the isolation cell enable and the destination register.

Recently, CDC analysis tools model retention cells and the logic driving the save and restore pins. Even though the save and restore logic is not modeled in the RTL, CDC analysis is able to detect errors in logic driving the save and restore pins. Avoiding metastability in retention cells will prevent data loss or corruption during the save and restore operations of the low power logic.

With power aware verification tools, designers can detect and fix errors associated with these power elements early in the design flow.

B. Beyond Static Low Power CDC Verification

Advanced low power flows are taking advantage of common CDC verification techniques to ensure that data transfer between power and voltage domains are not corrupted by metastability. These CDC verification techniques include both static and dynamic verification of CDC paths. The dynamic verification techniques leverage both simulation and formal model checking technologies on CDC protocol assertions and metastability delay models.

In addition to incorrect structures, it is important to identify correct synchronization structures, so CDC protocol assertions and metastability delay models can be generated for use with dynamic CDC verification techniques. Dynamic CDC verification involves verifying both CDC protocols and reconvergence logic. Each CDC synchronization structure type requires that the design logic adhere to a structure-specific set of protocols. A simple example of a CDC protocol is the stability requirement for 2DFF synchronizers to avoid data loss or data corruption.

For more complex synchronizers, adherence to the CDC protocol is needed to avoid metastability on the CDC transfer path. Additionally, we can expect certain CDC and VDC synchronization structures to have probabilistic delays due to metastability that is not modeled in traditional RTL simulation. The fan-in of reconvergence logic must be verified to ensure that there are no timing dependencies between synchronized CDC or VDC paths. Any timing dependencies between synchronized paths would result in functional errors in silicon.

During the static structural CDC analysis, both CDC synchronizer-specific protocol assertions and metastability delay models can be generated for each CDC path. The CDC protocol assertions can be used to check the synchronizer-specific rules in simulation or static timing analysis.

Metastability delay models should also be generated for each CDC path including VDC paths. The metastability delays occur in silicon, but this silicon-accurate metastability behavior does not occur in RTL simulation. Automatically generated, metastability delay models can be added to the RTL simulation. These models monitor the CDC path for conditions that would cause metastability in silicon and when metastability conditions are witnessed, the delay model randomly adds a cycle of delay at the RX register for setup violations or subtracts a cycle of delay at the RX register for hold violations. Using metastability models will ensure that each design is able to tolerate the metastability delays found in the design silicon.

C. Advanced Low Power CDC Verification

Advanced CDC solutions such as Questa CDC have the capability to more accurately model the asynchronous low power domains associated with DVFS. For designs which utilize DVFS, CDC analysis must determine the power domains in each voltage group based on the UPF file. Every clock group in the DVFS power domains must be considered asynchronous to all clock groups external to these power domains. Now, the asynchronous clocks identified in the design are the aggregate of the initial clock groups detected in the design and the new clock groups in the variable voltage power domains.

Once the design clocks have been accurately grouped, static structural analysis is used to verify both clock domain crossing paths and the voltage domain crossing paths. The CDC analysis will flag violations on the CDC and VDC paths that do not contain synchronizers or implement incorrect synchronizers. In addition, the correctly synchronized CDC and VDC paths will also be reported, so additional protocol and reconvergence checks can be run.

Advanced tools will not only instrument the power logic in the context of the RTL design, but will also visualize the VDC paths for review and debug. In typical CDC analysis solutions, paths between synchronous clock logic are not analyzed, but power aware CDC analysis solutions will detect new VDC paths between these synchronous crossings (See Fig. 8). In the illustrated case, the left and right power domains are on different voltages, so the synchronizer is required in the destination domain for this path. In order to facilitate review and debug, the asynchronous clock domains are color-coded and the color-coding can also be adjusted to implement power domain-specific color-coding. This path also demonstrates a case where combinational logic in the fan-in of a VDC path synchronizer would reduce the reliability of the synchronizer. This VDC violation would not have been detected with typical CDC analysis, since this design has only one clock domain.

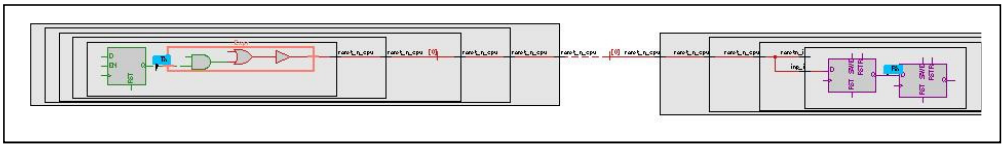

Figure 8. Combinational logic violation on synchronous voltage domain crossing

When a VDC error is reported, designers have the option to either fix the VDC error or add a waiver for any exception cases. The fixes to VDC errors occur in many forms. In the VDC case of a missing synchronizer violation, a synchronizer must be added to the destination power domain. In the above combinational logic violation, designers will need to ensure that a signal is registered in the source power domain before entering the destination power domain.

IV. Application of Low Power CDC Verification

Questa CDC was run twice on three different design subsystems. In the first run for each design, the CDC analysis was run on only the RTL representation of the design. In the second run on the three designs, power aware CDC analysis was run on both the RTL and UPF for the design. One design subsystem was a CPU core design with only one clock domain. Without the consideration of voltage domains, there are no CDC paths in this single clock design and CDC analysis would not normally be required. Although there was a low number of power and voltage domains, the number of asynchronous clocks increased by up to six times over the initial number when the voltage domain-related clock groups were taken into account.

The CPU core design demonstrates the effect of voltage domains on a single clock design (Table 1). When voltage domains are taken into consideration, this CPU core design is considered to have six asynchronous clocks and 4893 VDC paths. For the Subsystem 1 and Subsystem 2 designs, these designs have not been fully instrumented with power management logic, so the designers are must review the VDC paths to determine the appropriate power management strategies.

	Clocks	Power Domains	Voltage Domains	Asynchonrous Clocks	Isolation Cells	Retention Registers	VDC Paths
CPU Core	1	6	6	6	438	134690	4893
Subsystem 1	10	4	4	26	439	0	8404
Subsystem 2	10	5	2	7	142	0	10610

Table 1: CPU core design with power control logic

Surprisingly, a large number of VDC paths were generated when DVFS voltage domains are taken into account. This is an indication that DVFS design techniques may significantly lower MTBF and cause reliability issues when the VDC paths are not verified. The VDC errors may cause intermittent failures under corner case conditions. These

corner case conditions may occur in scenarios that have not been accounted for during static timing analysis. Static timing analysis may have assumed a deterministic phase relationship between synchronous clocks that run into or out of a DVFS power domain. In this case, the intermittent VDC errors are likely to occur when the design is in a power-saving mode.

V. SUMMARY

Power management continues to be a critical need for mobile systems. With the advances in low power design, the low power design and verification methodologies and techniques continue to evolve. The successive refinement features in IEEE 1801 allow designers to begin the design and verification of power distribution networks earlier in the design flow and continue to refine the power networks throughout the design cycle. Designers can start CDC verification for the power distribution networks at the RTL level and avoid detection of CDC errors late in the design flow at the gate-level.

In addition to the CDC verification for paths with isolation and retention cells, design teams have found that the VDC paths are analogous to CDC paths and additional verification is required. The Mentor Graphics Questa CDC solution verifies paths between DVFS voltage domains that may cause reliability or functional problems in silicon.

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