Power Aware CDC Verification of Dynamic Frequency and Voltage Scaling (DVFS) Artifacts

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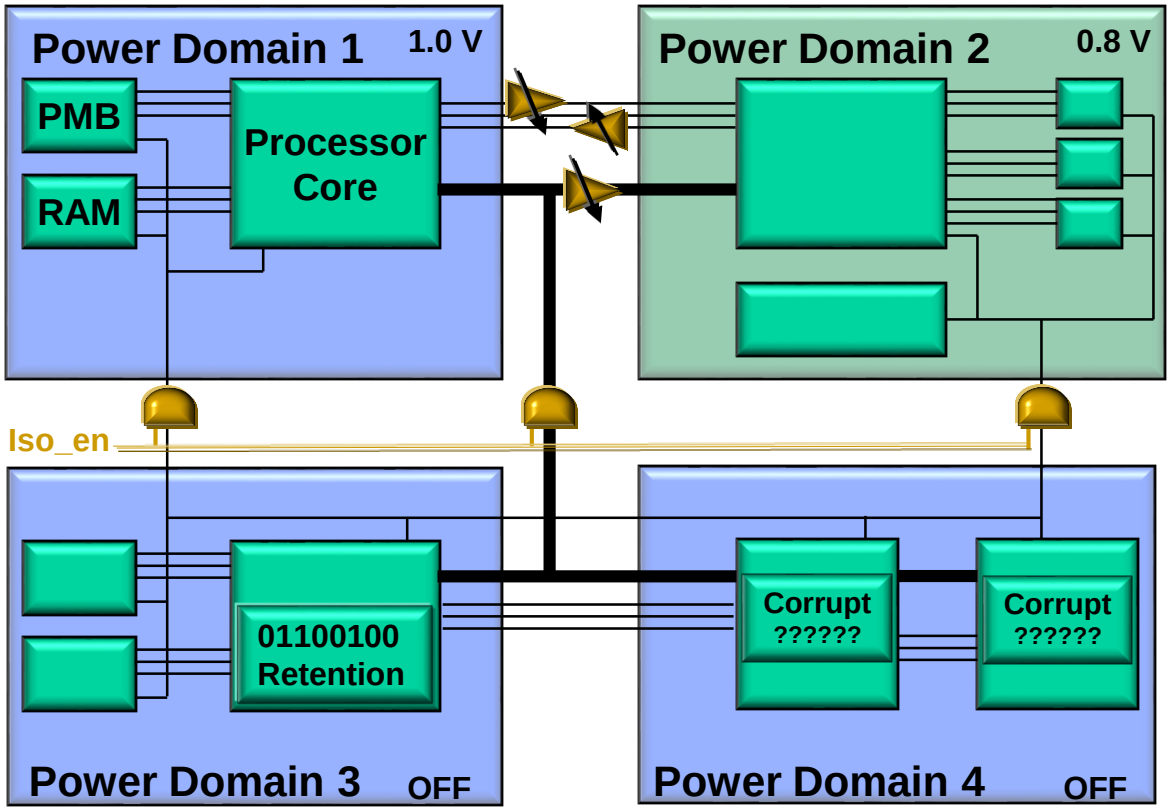
Power Management is Critical Today

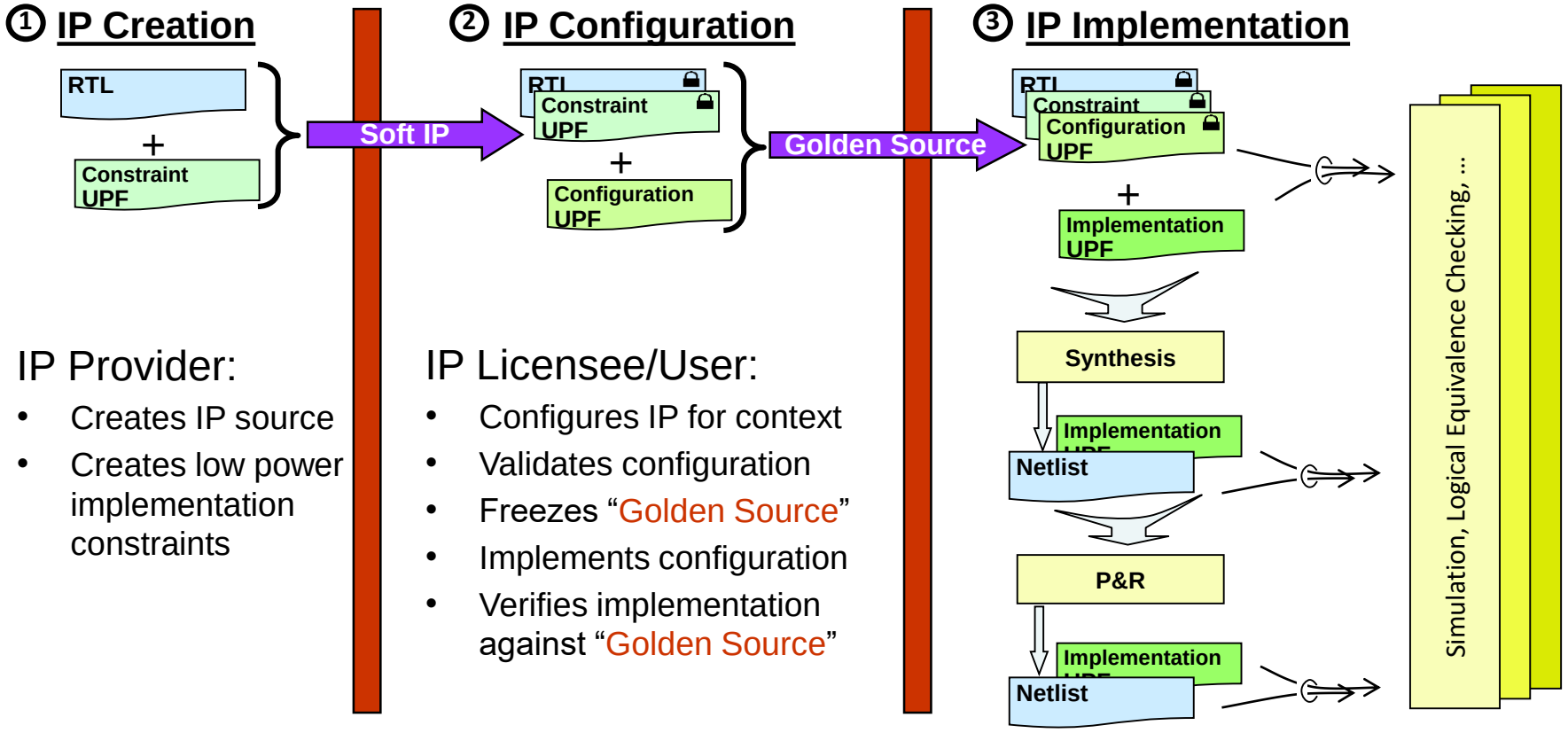
- Driving for finer process technology
  - Smaller, lighter products
  - Longer battery life
  - More functionality
- Dynamic power
  - Signal switching consumes energy
  - Was the major contributor to power consumption
- Static power
  - Static leakage can consume 50% of power!
  - Now the major concern for power optimization
- Government and industry regulation

SOC Power Management Techniques

- Leakage Power Reduction is Key in Low-Power Design
- Chief Aspects of Power Management
  - Power Shut-off
  - Isolation
  - Retention
  - Corruption
  - Multiple Voltages
  - Level shifters
- UPF (Unified Power Format)
  - Define Power Management independent of design



IEEE 1801 Unified Power Format (UPF)



IP Provider:

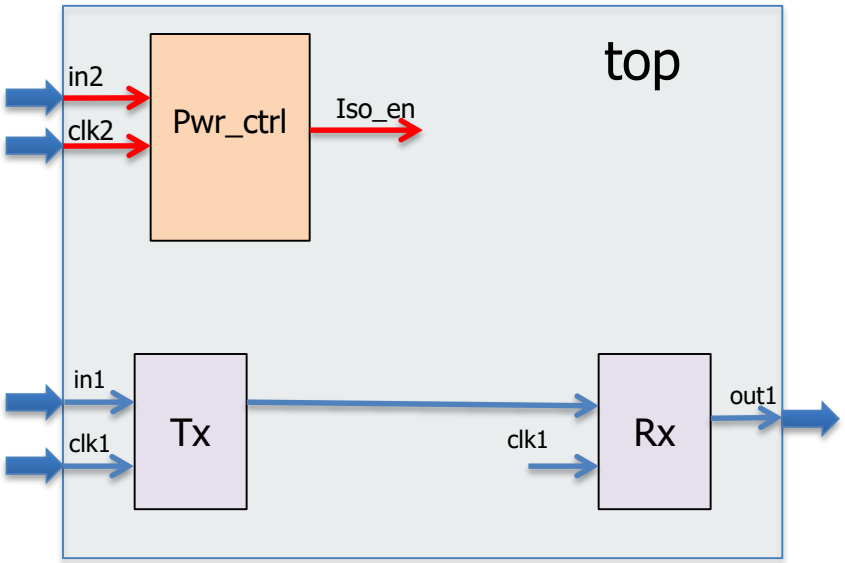
- Creates IP source
- Creates low power implementation constraints

IP Licensee/User:

- Configures IP for context
- Validates configuration
- Freezes "Golden Source"
- Implements configuration
- Verifies implementation against "Golden Source"

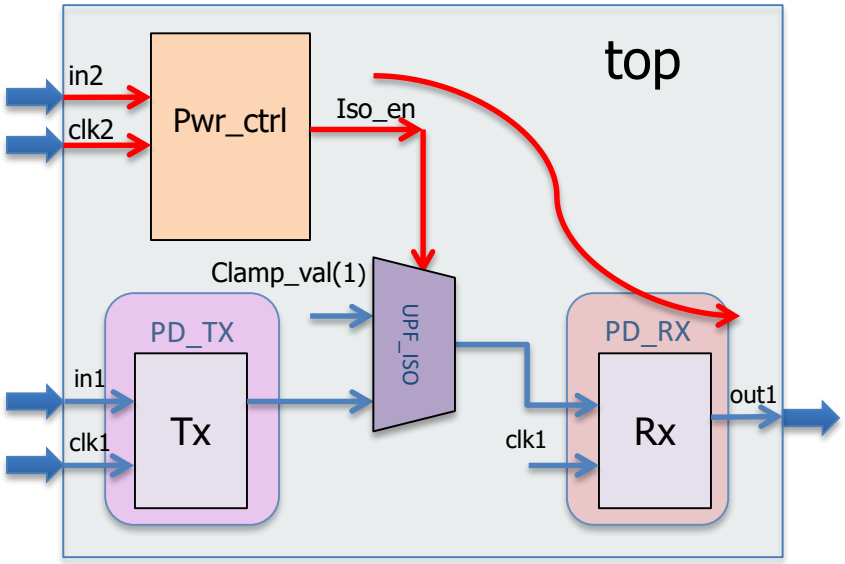
CDC Paths without UPF

- Power control logic unconnected in RTL
- CDC analysis on RTL will not verify power control logic
  - RTL functional paths only



CDC Paths with UPF

- UPF specifies Power Artefacts
  - specifies power domains, isolation strategies etc.
- Addition of UPF may add new CDC paths



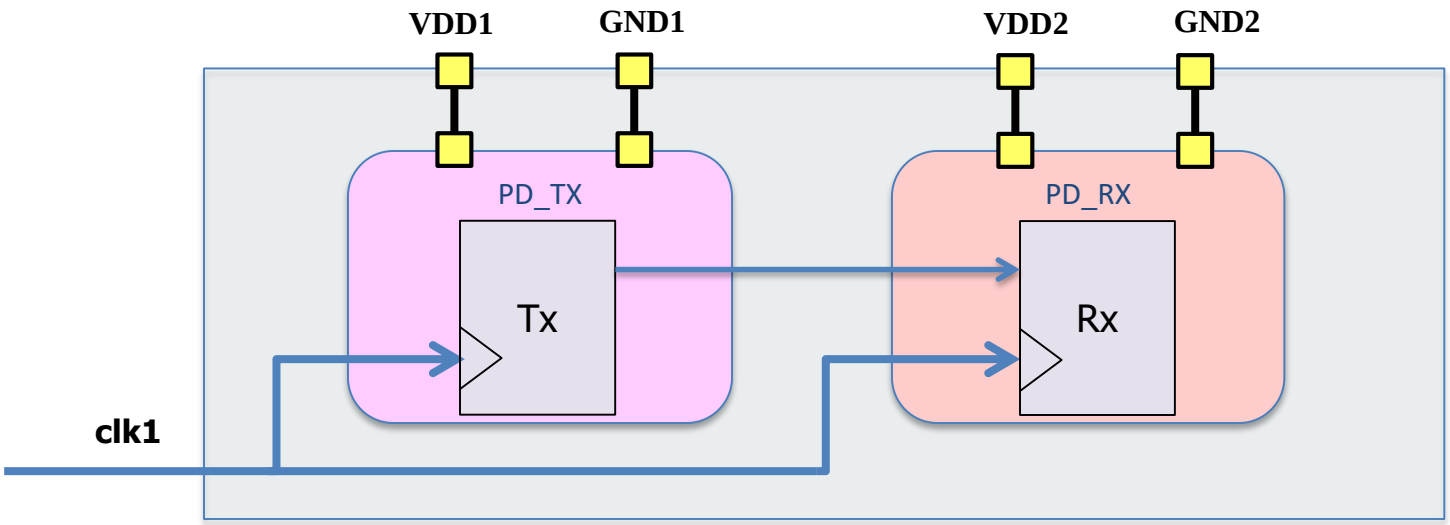
Dynamic Frequency and Voltage Scaling

- Frequency and Voltage interdependence
  - Max operating frequency dependent on voltage
  - Reducing frequency allows voltage & power reduction
- Small voltage reductions = large power savings
  - Energy consumption proportional to supply voltage

Processor E α V^2 *

* Burd, T. D. and Brodersen, R. W. Energy efficient CMOS microprocessor design. HICSS 1995.

Voltage Domain Crossing (VDC)



- DVFS domains create asynchronous clock groups
- Identify crossings between synchronous paths on different voltage domains

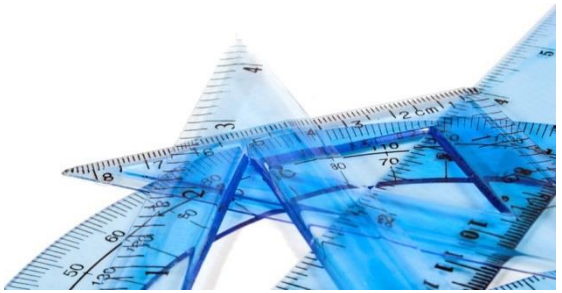
Impact of Low Power CDC Issues

- Missed CDC paths will …
  - Reduce product reliability
  - Cause intermittent failures
- Gate-level CDC analysis
  - Extremely noisy & time consuming
- Debug of Low Power CDC issues cause …
  - Many debug man-hours of intermittent issues
  - Silicon vs. RTL inconsistencies
    - Difficulty of correlating silicon failures to RTL simulation
    - Difficult of verifying fixes to intermittent issues

Low Power CDC Verification Challenges

UPF Support Requirements for CDC Analysis

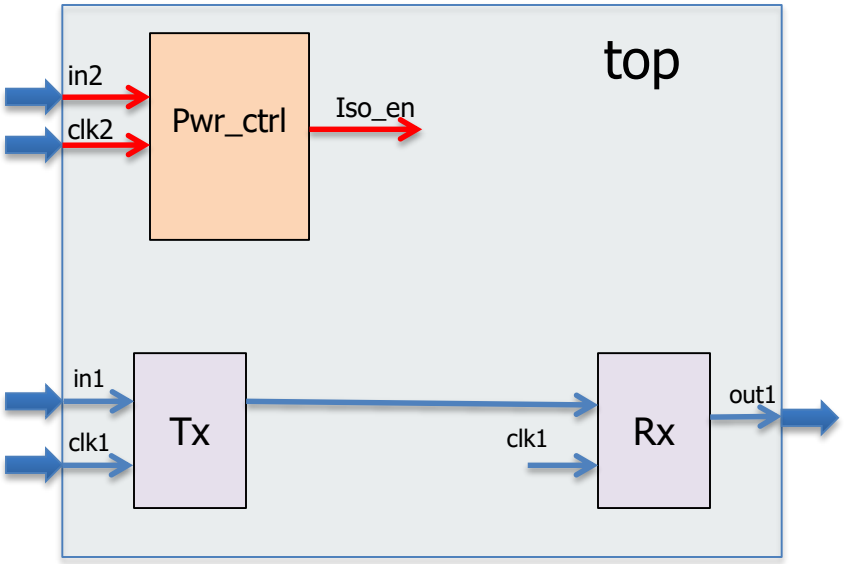
- Infer power cells in RTL
  - Isolation
  - Retention
  - Level shifters
- Infer voltage supply network
  - Power network
  - Power switches



Power Aware CDC Requirement

- Verify interaction between power network and RTL
  - UPF specifies power domains, placement of isolation cells

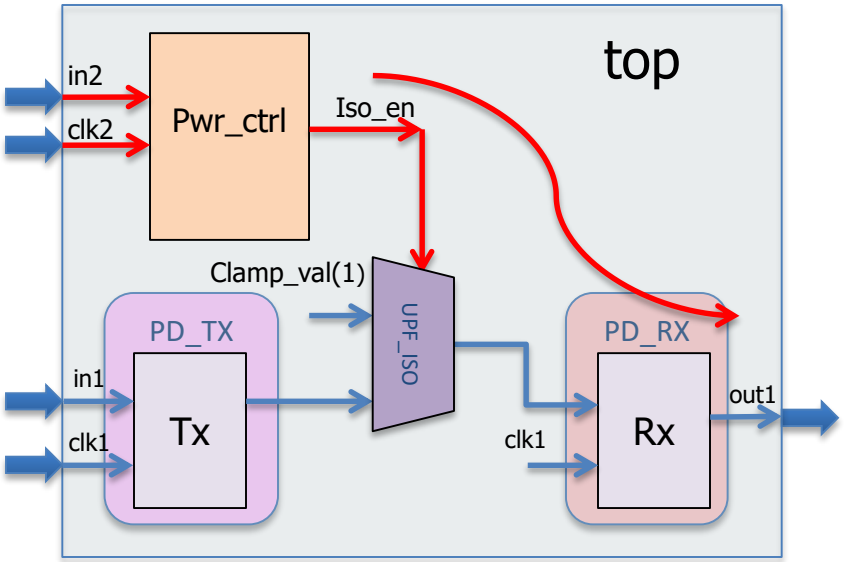
```
set_design_top top
create_power_domain TOP
create_power_domain PD_TX -elements {Tx}
create_power_domain PD_RX -elements {Rx}

create_supply_set PRIMARY1
create_supply_set  PRIMARY2

associate_supply_set PRIMARY1 -handle PD_TX.primary
associate_supply_set PRIMARY2 -handle PD_RX.primary

set_isolation PD_TX_ISO_OUT  -domain PD_TX \
  -clamp_value 1  -applies_to  outputs \
  -isolation_signal iso_en  -isolation_sense low \
  -location parent
```



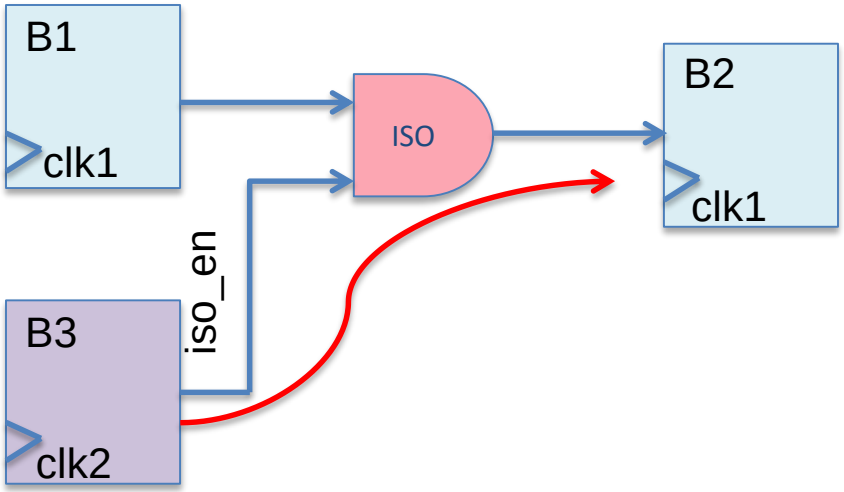
Power Aware CDC Analysis

- Annotated design netlist contains power network
- CDC analysis on RTL + power network

```
Violations
=========================================
Isolation enable signal does not have proper synchronizer.
(iso_en_no_sync)
-----------------------------------------------------------------
clk2 : start : Pwr_ctrl.out1
       clk1 : end : Rx.out1
                    (ID: iso_en_no_sync_40515)
                    via : qspa_iso_1.out1_UPF_ISO.isolation_signal
                    via : qspa_iso_1.out1_UPF_ISO.isolation_output
```

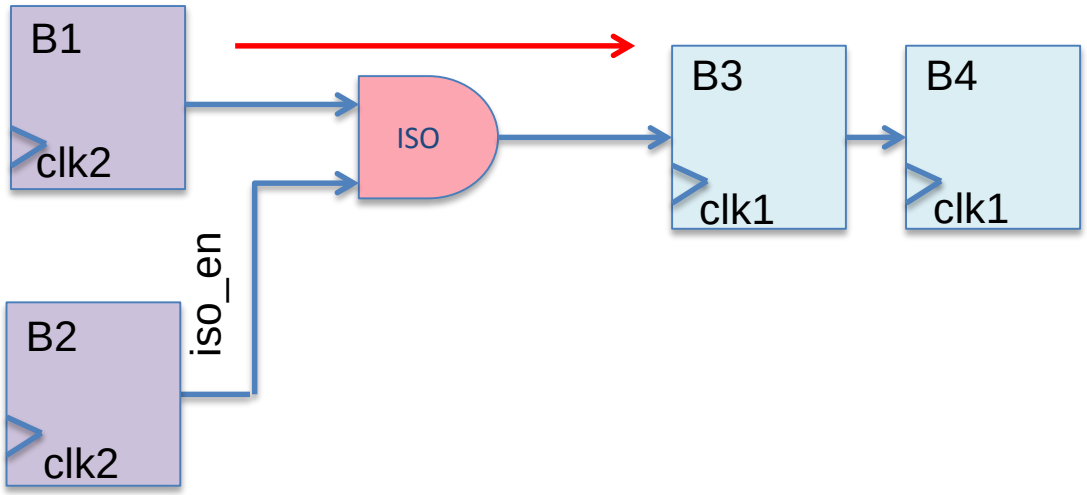


Isolation Enable Missing Synchronizer



- Blocks B1 & B2 are in clock clk1
- iso_en comes from block B3 in clock domain clk2
- Violation for the new CDC path B3->B2

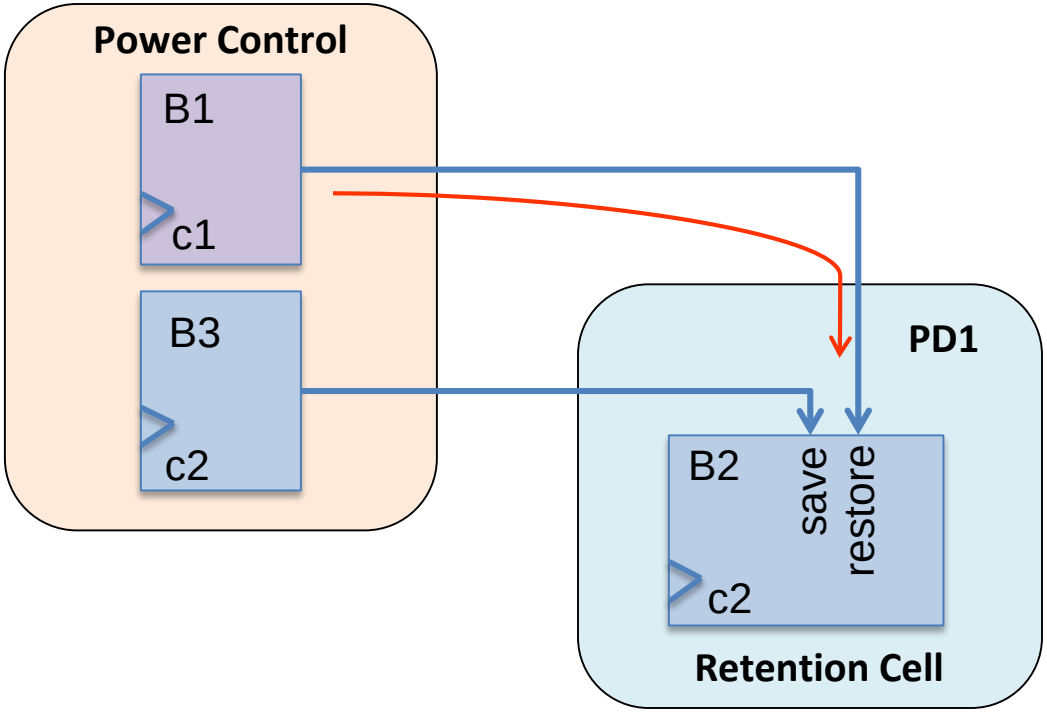
Isolation Cell Combo Logic before Synchronizer



- Block B1 is synchronized via B3/B4
- Isolation cell is placed at input to synchronizer
- Violation for the new CDC path B1->B3

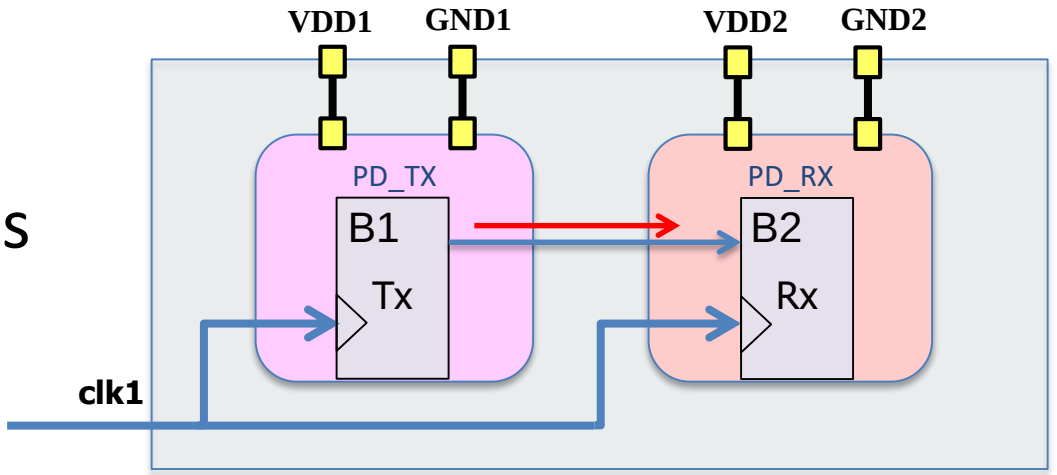
Power Aware Retention Crossing

- Retention cell adds paths to save and restore pins
- New CDC violation B1=>B2



Voltage Domain Crossing

- Identify CDC paths that start or end on DVFS voltage domains
- New CDC violation B1=>B2




```
# Specify Supply Set
create_supply_set PRIMARY1
create_supply_set  PRIMARY2

# Declare primary power and ground nets for the power domains
associate_supply_set PRIMARY1 -handle PD_TX.primary
associate_supply_set PRIMARY2 -handle PD_RX.primary
```

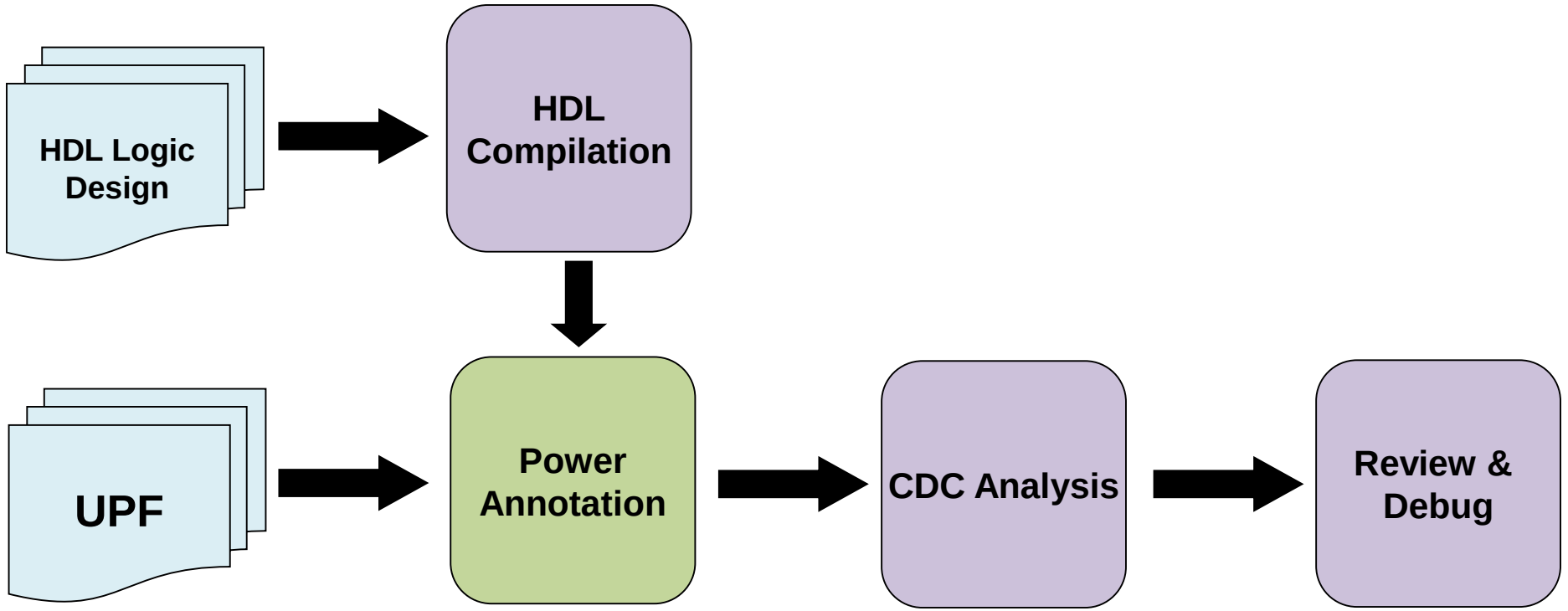
Power Aware CDC with Questa CDC

Power Aware CDC Analysis

- CDC-PA verifies structural CDC paths
  - Power Management functionality verified by simulation/formal

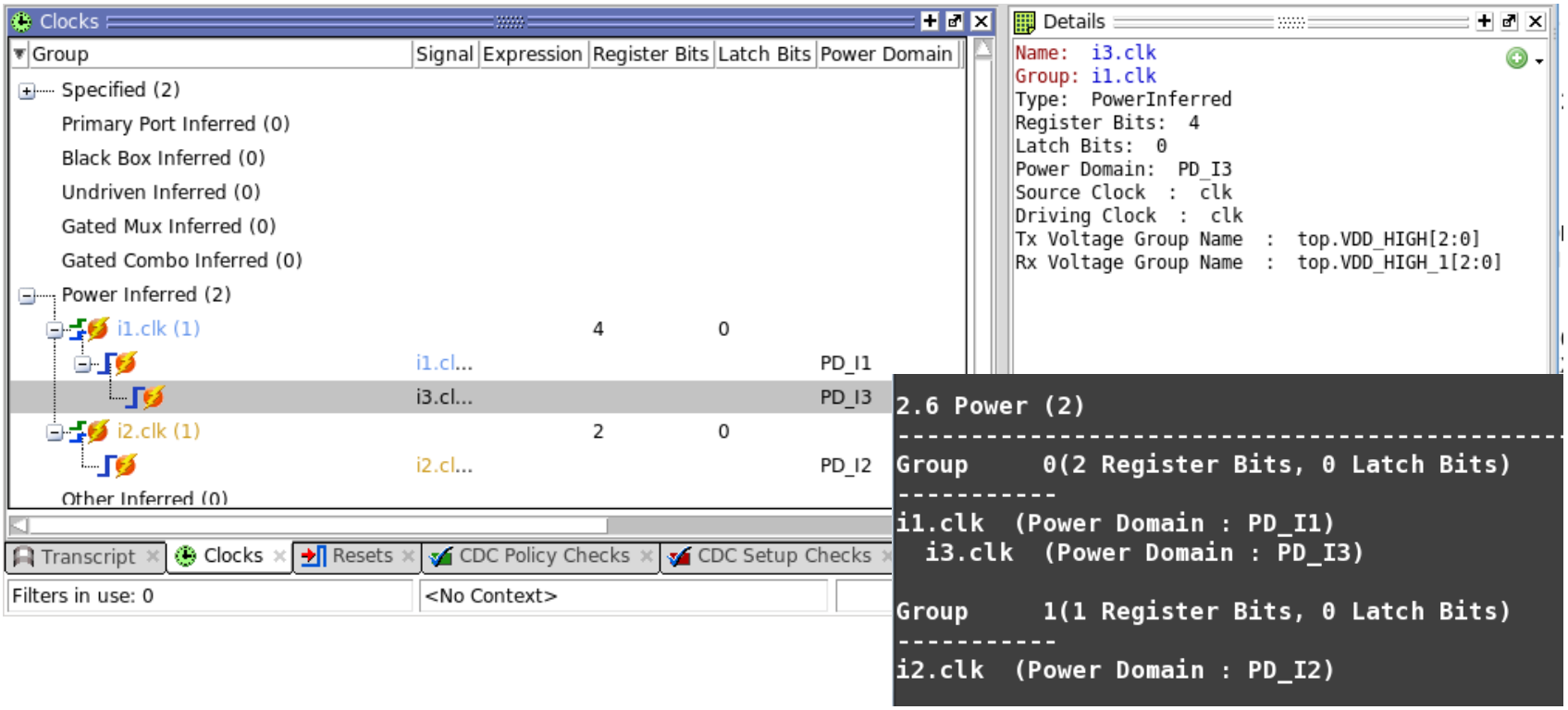
- Identify Power Aware CDC paths
- Detect Power Aware CDC scenarios
  - Isolation enable violation
  - Combinational logic violation
  - Retention cell save/restore violation
- Detect Voltage Domain Crossing schemes
  - Identify all VDC paths
  - Check for VDC synchronizations & violations

Power Aware CDC Flow



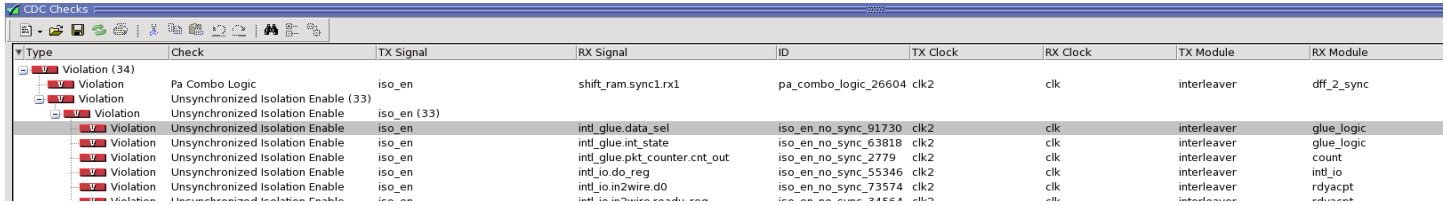
Power Aware CDC Reporting & Debug

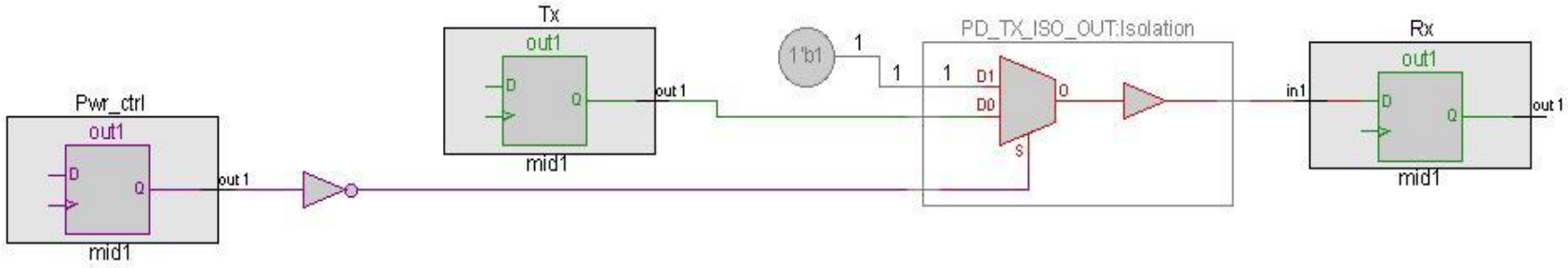
- Report new voltage domain clock groups



Power Aware CDC Reporting & Debug

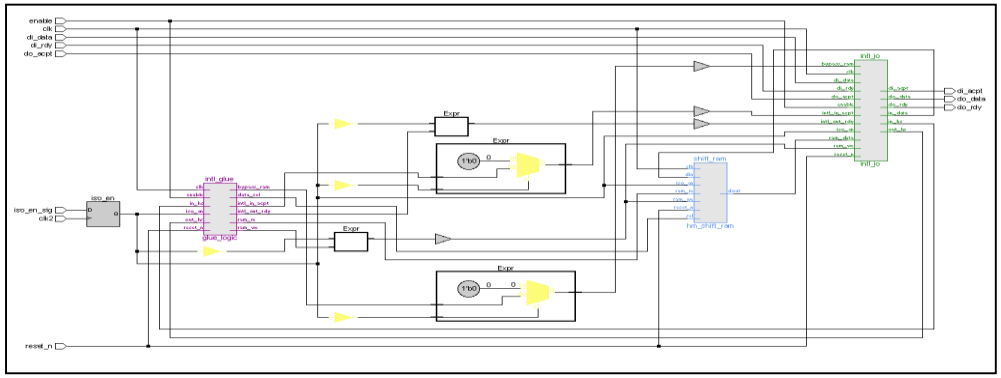
- Report power domain-specific CDC issues
  - Differentiate logic in different power domains



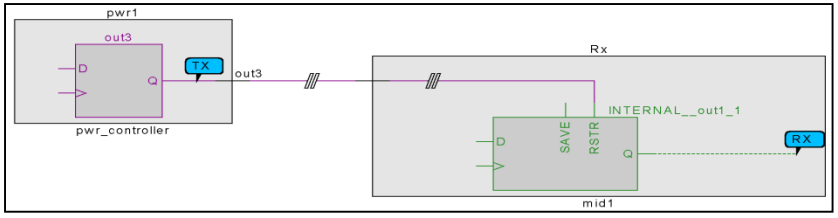


Power Aware CDC Reporting & Debug

- Debug via power domain-specific GUI
  - Visualize power domains and power elements
  - Visualize voltage domain-specific clocks and crossings



Power Domains



Retention Cell

Application of Low Power CDC Verification

	Clocks	Power Domains	Voltage Domains	Asynchronous Clocks	Isolation Cells	Retention Registers	VDC Paths
CPU Core	1	6	6	6	438	134690	4893
Subsystem 1	10	4	4	26	439	0	8404
Subsystem 2	10	5	2	7	142	0	10610

- Potential CDC issues from Isolation and retention cells
- Large number of VDC paths
  - DVFS creates multiple async clocks in a single clock design block
  - Requires verification to ensure reliability

Conclusion

- Low Power issues are missed by traditional CDC methods
- Low Power design introduces
  - New asynchronous clock domains
  - New CDC & VDC paths
- Use Questa Power Aware CDC solution to
  - Improve low power design reliability
  - Avoid low power CDC failures in silicon

Questions