Power Aware CDC Analysis at Top Level Using SOC Abstract Flow

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***Abstract*- Hearable and Wearable devices form a significant part of the internet of things (IOT) market segment. As with any IOT product, meeting ultra-low power needs form the primary requirement of such products. With design teams spread across the globe, the challenges encountered during the design, integration and verification of these products are many from meeting stringent power requirements to quick time to market. This paper focuses on few of these issues seen during the integration and verification phase, mainly dealing with multiple clock domain crossings with low power structures.**

I. Introduction

Generally, a bottom-up clock domain crossing (CDC) analysis at top level is a ***flat-flow*** approach. In ***flat-flow***, complete design is being read along with the constraints for the analysis. With the CDC clean IP's delivered by the IP teams, it still poses a plethora of challenges to the integration team. To name a few,

IP waiver management: The top level team has to work closely with the IP teams to get the IP level constraints and waivers correctly deployed.

Spotting True CDC violations: Once the run is completed, one has to go through the pain of having to find the "true" error, warning within a deluge of unwanted messages that are not under the top level purview.

SoC CDC abstract flow: the IP blocks are replaced by equivalent abstract models, which captures all the relevant CDC details of the IP blocks. This flow eases the setup effort at the top level considerably by doing away with the cumbersome IP level waiver management. More importantly, the flow reduces the number of unwanted warnings, errors that get generated at the top level as compared to the classical flat-flow, without ignoring any rules.

Early verifying of low power structures across different IP's with respect to CDC: The clock and data path's crossings would encounter low power cells implemented via common power format (CPF) / unified power format (UPF) constraints. At the RTL stage however, these cells would not be present. Paths with such crossings may require additional synchronizing schemes to be added. Performing the CDC analysis on the gate level will be too late to catch the bugs in the design Flow. The low power structures across various clock domains paths like isolation and retention logic are specified in the CPF/UPF constraint file. The constraint file is used to identify the possible low power CDC issues by mapping the hierarchy with synchronized domain crossings early in the verification phase.

The presentation captures a case study of the SoC abstraction flow compared with the other approaches like *classical flat-flow, with ip_block option, with blackbox option* and summarizes the benefits seen. And the enhancements being experimented on the SoC abstract flow for power aware and early detection of CDC issues related to power artifacts at RTL stage.

II. Challenges in SoC CDC Analysis

In the typical flat flow SoC CDC analysis, entire SoC is analyzed. Constraints are defined for top and the design is fully elaborated and run flat with all intra and inter block crossings. With the ip_block option the intra –block CDC violations can be filtered and debug is done by SoC integrators with the help of IP owners. In the Flat Flow at SoC top level, block level constraints are validated and mapped accordingly for reuse at top level to eliminate reanalyzing the false CDC violations which are previously analyzed. With the entire SoC being analyzed at top level, the performance increases as the design size increases. As a result runtime for large designs could be in hours to days. New violations gets reported within a verified sub block when run at top level due to wrong or missing information at block level. With more IP's the performance at top level gets deteriorated by large number of block level constraints. Most of the times analysis becomes exactly the same as running a block level but bigger and slower.

A. ip_block

The focus of integration team should be on the inter-block and top level domain crossing. The ip_block option of CDC verification tool ensures that the issues inside the IP's are filtered and not reported. But the disadvantages of using this option are: The qualifiers present inside the IP are not considered for crossing outside the IP. Figure 1 depicts the ip_block and qualifiers which ensures for safe data transfer via synchronizers inside the block are not considered and cause false violations.

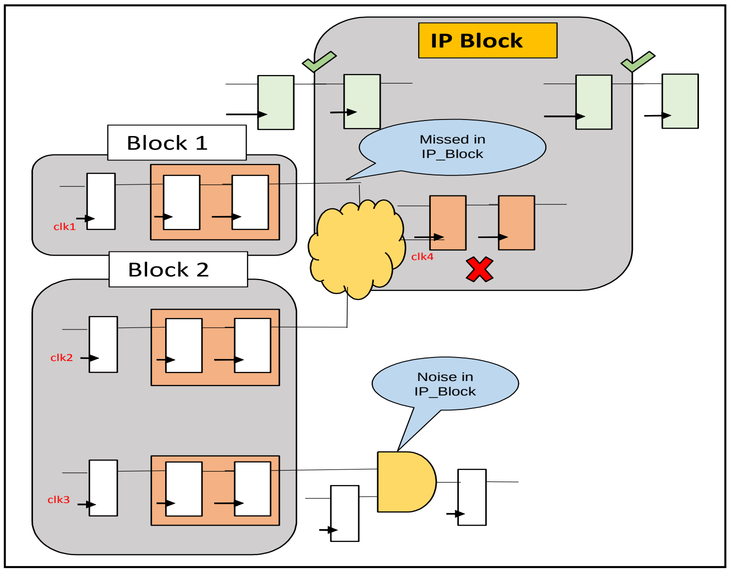

Figure 1. ip_block

B. ip_blackbox

Black-boxing the IP at top level makes the IP and its interface completely invisible to the analysis as shown in Figure 2. The CDC issues will be specific to top level alone. Run times could be better compared to flat flow. But the inter IP analysis is not done. Inter IP block issues and convergence issues are masked.

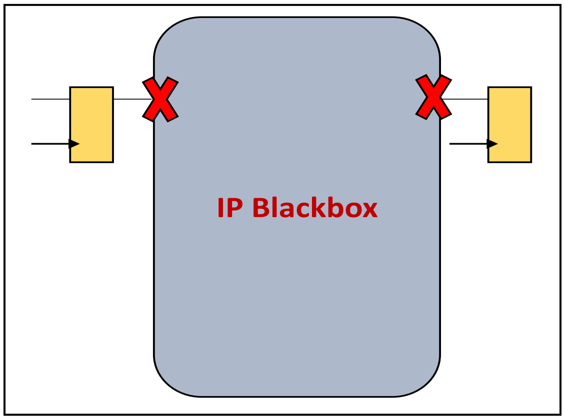

Figure 2. ip_blackbox

III. An Abstraction-Based Bottom Up Spyglass CDC Verification Flow

Abstract models can be generated for the required IP blocks. We generated abstract models for a completely verified and CDC cleaned IP blocks. These abstract models provides sufficient block interface details for chip level analysis that describe the behavior of the block ports as shown in Figure 3. The constraints model the clocks, constants, and qualifiers that control the port. For an input port, they model what drives the port from outside the block while for an output port, they model what drives the port from inside the block. Examples of these constraints are *clock*, *set_case_analysis*, and *abstract port* constraints. The constraint *abstract_port* models the domain of the flops that drive the port, the synchronizers in its fan-in, and synchronizer properties such as the presence/absence of combinational and sequential logic, on the path to the port. The generated abstract model is validated for the consistency in the context of higher-level block. After analyzing the violations, CDC analysis at top level is performed for the desired goals. Figure 4 shows the SoC level abstract flow.

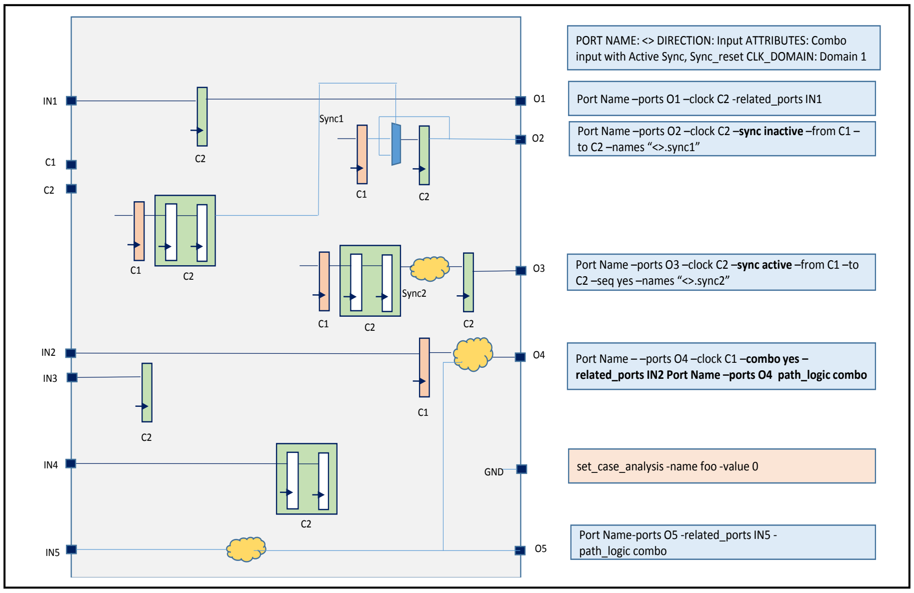
IN1
C1
C2
IN2
IN3
IN4
IN5
C2
C1
C2
Sync1
C1
C2
C1
C2
Sync2
C2
C1
C2
C1
C2
GND
O1
O2
O3
O4
O5
PORT NAME: <> DIRECTION: Input ATTRIBUTES: Combo input with Active Sync, Sync_reset CLK_DOMAIN: Domain 1
Port Name –ports O1 –clock C2 -related_ports IN1
Port Name –ports O2 –clock C2 –**sync inactive** –from C1 –to C2 –names "<>.sync1"
Port Name –ports O3 –clock C2 –**sync active** –from C1 –to C2 –seq yes –names "<>.sync2"
Port Name – –ports O4 –clock C1 –**combo yes –related_ports IN2 Port Name –ports O4 path_logic combo**
set_case_analysis -name foo -value 0
Port Name-ports O5 -related_ports IN5 -path_logic combo

Figure 3. Abstract Model

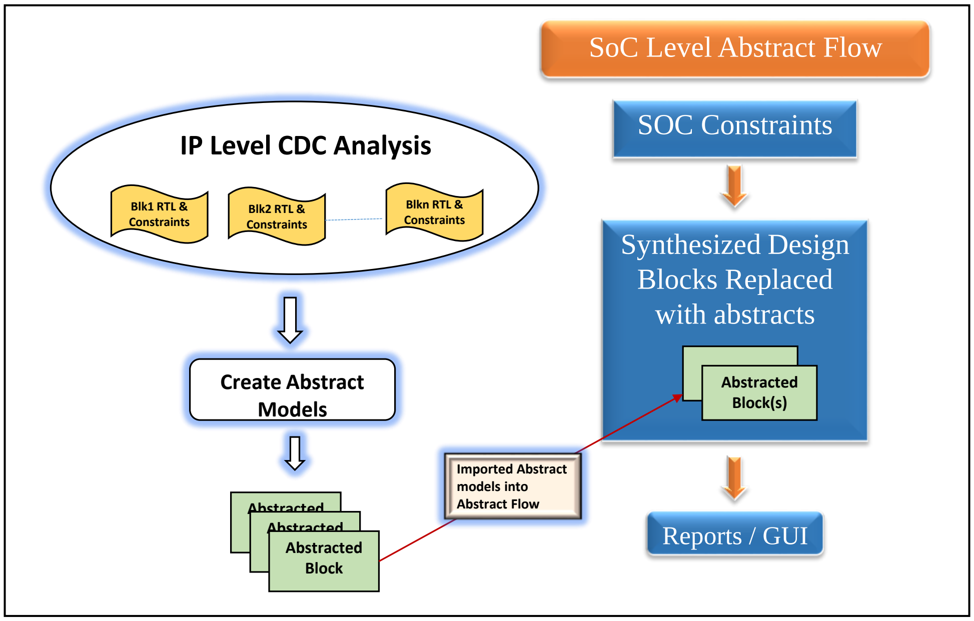

Figure 4. SoC Level Abstract Flow

IV. NEED FOR POWER AWARE CDC ANALYSIS

The clock and data paths crossing would encounter low power artifacts implemented via CPF / UPF constraints during synthesis. During the low power synthesis flow, the isolation and retention cells gets added. These low power artifacts creates new paths to be analyzed for domain crossings at gate level. At the RTL stage however these cells would not be present. Paths with such crossings may require additional synchronizing schemes to be added. The CDC issues introduced as a result of low power synthesis would go unnoticed till the analysis is done at the gate level as shown in Figure 5. In the earlier SoC level abstract flow any issues which may arise as a consequence low power artifact, would not be readily seen at the RTL level.

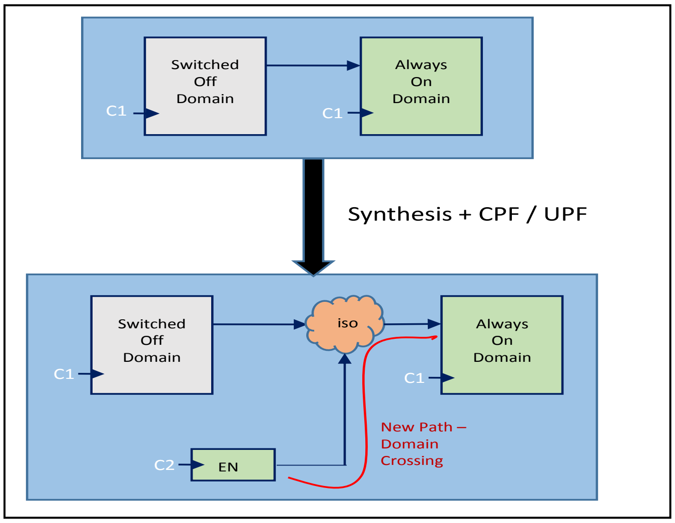

Figure 5. Low Power artifacts after Synthesis

V. EARLY DETECTION OF CDC ISSUES ON THE PATHS OF LOW POWER ARTIFACTS

The low power artifacts across various clock domains paths like isolation and retention logic are specified in the CPF / UPF constraints file. CDC analysis is performed at top level using the SoC abstract flow, to get a list of all the possible crossings. The list is compared with CPF / UPF to obtain the crossings between power domains. Such paths are then analyzed with respect to source and destination clock sources to conclude if the introduction of low power cells would cause an issue. Figure 6 depicts the proposed SoC level abstract flow and power aware.

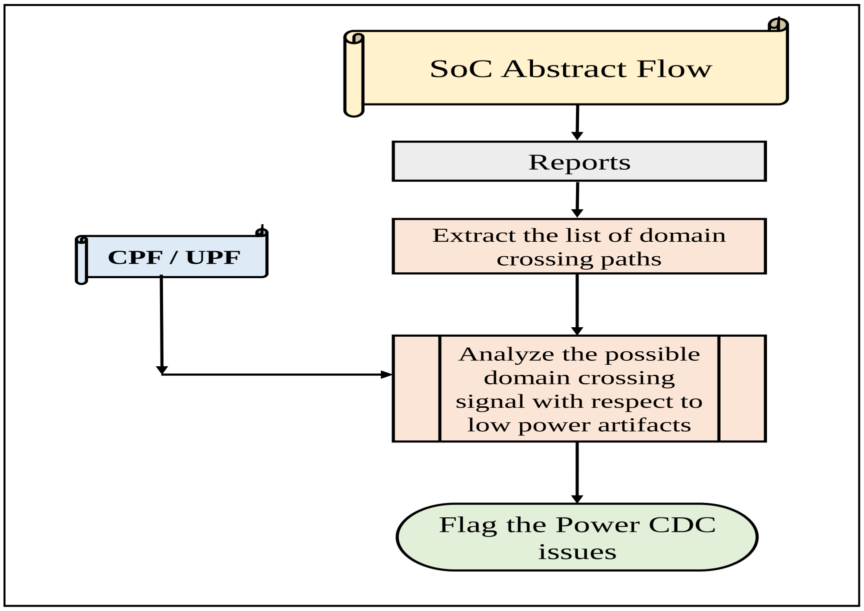
SoC Abstract Flow
Reports
Extract the list of domain crossing paths
CPF / UPF
Analyze the possible domain crossing signal with respect to low power artifacts
Flag the Power CDC issues

Figure 6. Proposed flow for power CDC issues

The different kinds of issues CDC issues which can be detected from the proposed flow at the early stage of RTL are described below:

Isolation logic cells gets added during the low power synthesis. If the enable of isolation cell from clock C2 is asynchronous to destination clock C1, causing for the introduction of new domain path crossing which gets flagged as shown in Figure 7.

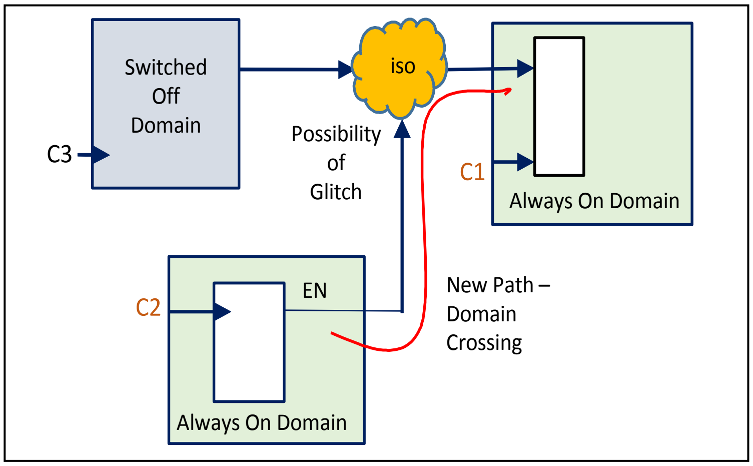

Figure 7. CDC path after synthesis

There are possibilities of glitch occurrences for signals interacting from switched off domain to always on domain, though the enable for the isolation cell is synchronous to the destination domain. In Figure 8, the enable for isolation and the destination registers are clocked to C1. Isolation and Power enable signal working is depicted in Figure 8a.

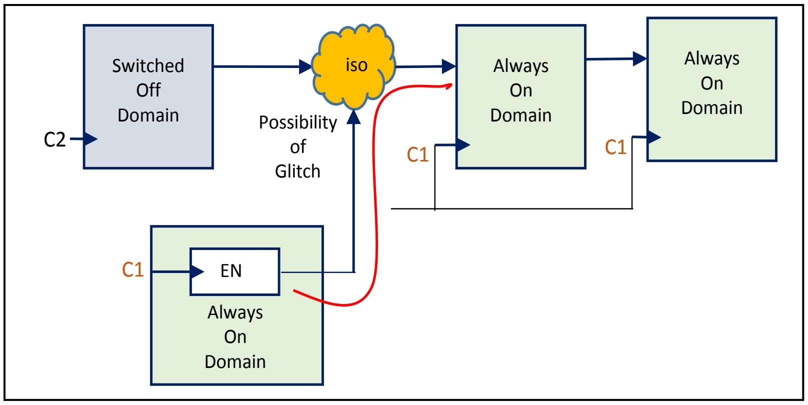

Figure 8. Possibility of Glitch Occurrence at Isolation Cell

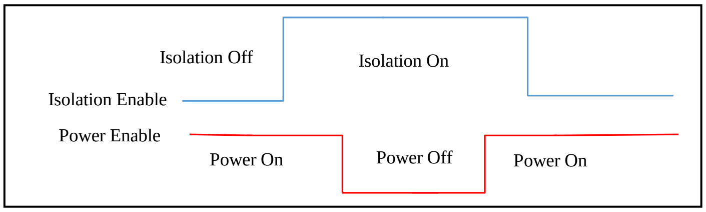

Figure 8a. Isolation & Power Signal

In Figure 9. The isolation cell gets an enable from clock domain C1. The reset comes from the switchable domain via a reset synchronizer on C2 and goes to another power domain of the same clock as synchronized reset. But if there is an isolation cell now on C1, this could cause reset recovery issue.

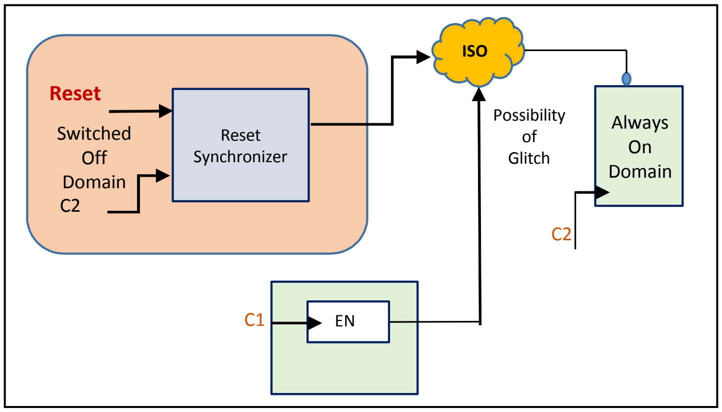

Figure 9. Reset recovery issue

The proposed SoC abstract flow was employed for CDC analysis for Ultra Low Power Mixed Signal IC which consisted of around 50 functional clock domains, gate count of ~600K and multiple power domains. Gains observed with respect to run time and reports crossings are tabulated in Table 1. The issues which gets covered in the abstract flow in comparison with earlier flows are tabulated in Table 2.

Experiments are being carried out for the enhancements made on SoC abstract flow for the proposed flow at top level for the early detection of low power introduced CDC issues.

Table I. Run Time and Reports

	Flat Run	**With ip_block**	**With IP Blackboxed**	**Abstract Flow**
Run Time	~ 10Hrs	~10Hrs	1 min	15min
Unsynchronized Scalar / Vector crossings	7658/355	7378/249	3/0	8/8
Synchronized Scalar / Vector Crossings	8032/256	1411/24	8/0	88/27

Run time and reported crossings comparison are tabulated in Table 1 for the different flows. Table 2 details on the Set up effort required and different kinds of checks which gets covered for the described flow.

Table II. Flow Comparison

	Flat Run	**With ip_block**	**With IP Blackboxed**	**Abstract Flow**
Set up Effort	Single Step	Single Step	Single Step	2/ 3 Steps involved
Interface Checks at top Level	Yes	Yes	Yes	Yes
Inter-Block CDC Checks	Yes	Yes	No	Yes
Convergence Checks	Yes	No	No	Yes
Unwanted Messages to deal with	Maximum	Could be slightly less compared to Flat Runs	Low (Many Crossings were nor considered)	Least compared to the other flows

VI. SUMMARY

The proposed flow helped us close on the CDC issues at top level with tremendous improvements in the run time and reduced considerable effort in filtering out noise.

- Average 10X improvement in run time.
- CDC Analysis scope focused on the top level.
- No need to modify/re-use IP level waivers.
- With the reduced number of warnings / messages, we were able to quickly identify true CDC issues.
- Additional Convergence checks at the top level which are not checked with ip_block and ip_blackbox.
- There are chances of CDC issues can get masked with ip_blackbox for the inter-block analysis and can easily lead to bad silicon, whereas with the abstract flow all such crossing would be considered for the analysis.

- Power Aware CDC analysis helped in analyzing the domain crossing with low power structures quite early in the project cycle.

ACKNOWLEDGMENT

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