Power Aware CDC Analysis at Top Level Using SOC Abstract Flow

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INTRODUCTION

Hearable & Wearable devices form a significant part of Internet of Things (IoT) market segments. As with any IoT product, meeting ultra-low power needs form the primary requirement of such products. With design teams spread across the globe, the challenges encountered during the design, integration and verification of these products are many from meeting stringent power requirements to quick time to market. This paper focuses on few of these issues seen during the integration and verification phase, dealing with multiple clock domain crossings (CDC) with low power structures.

CHALLENGES IN SOC CDC ANALYSIS

In the typical Flat Flow SOC CDC analysis, entire SOC is analyzed.

- Performance and Memory requirements increases with CDC complexity.
- IP Waiver Management.
- Spotting True CDC Violations.

Flat Flow with IP interface details

- Qualifiers which ensures for safe data transfer via synchronizers inside the block are not considered and cause false violations.

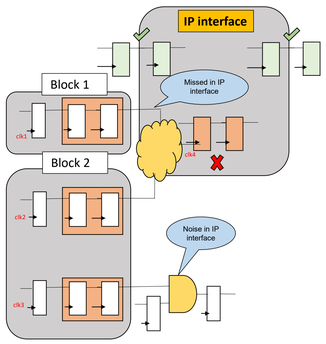

Figure 1: IP interface

Flat Flow with IP blackbox

- Better run times, but inter IP block issues and Convergence issues are masked.

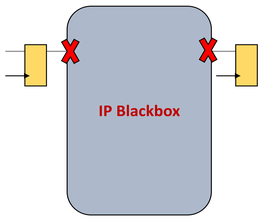

Figure 2: IP blackbox

AN ABSTRACTION BASED BOTTOM UP CDC VERIFICATION FLOW

- Abstract models can be generated for the required IP blocks and provides sufficient block interface details for chip level analysis.
- The constraints model the clocks, constants and qualifiers that control the port.

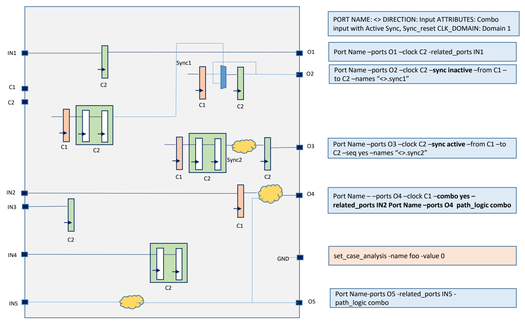

Figure 3: Abstract Model

- The generated abstract model is validated for the consistency in context of higher-level block.
- CDC analysis at top level is performed for the desired goal.

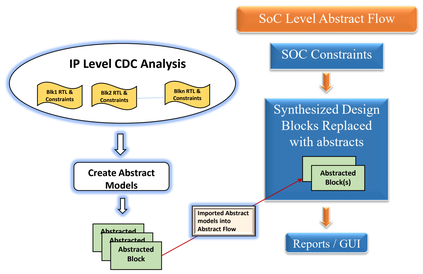

Figure 4: SoC Level Abstract Flow

NEED FOR POWER AWARE CDC ANALYSIS

- Introduction of Low Power structures during synthesis flow creates new paths to be analyzed for domain crossings at gate level.
- Issues which may arise as a consequence of low power structure, would not be readily seen at the RTL level.

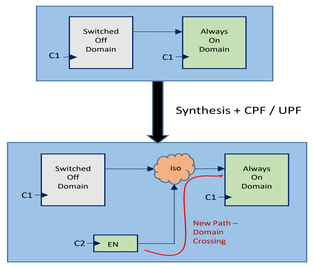

Figure 5: Low Power Structure after Synthesis

EARLY DETECTION OF CDC ISSUES ON THE PATHS OF LOW POWER STRUCTURE

The proposed flow at top level for the early detection of CDC issues arising from low power structures.

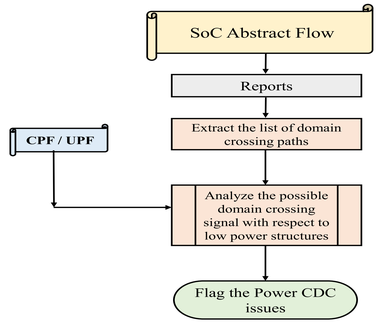

Figure 6: Proposed flow for power CDC issues

Some of the CDC issues that can be detected by the proposed flow at the early stages of RTL are

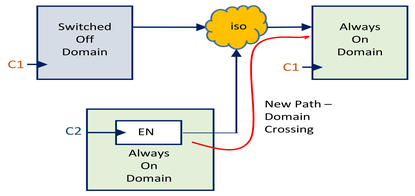

Figure 7: New CDC path introduced after synthesis

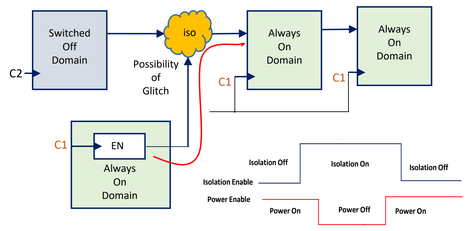

Figure 8: Possibility of Glitch Occurrence at Isolation Cell

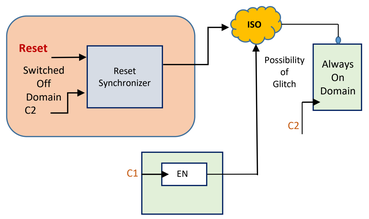

Figure 9: Reset recovery issue

Case Study & Results:

- The SoC Abstract Flow (Non Power Aware) was employed for
  - Ultra Low Power Mixed Signal IC
  - Application: Hearing Aid Device.
    - Gate Count: ~600K
    - Flop Count: ~100K
    - Clock Domains: 50 Functional Clock domains.

Gains observed with respect to run time and reports crossings:

	Flat Run	With ip_block	With IP Blackboxed	Abstract Flow
Set up Effort	Single Step	Single Step	Single Step	2/ 3 Steps involved
Interface Checks at top Level	Yes	Yes	Yes	Yes
Inter-Block CDC Checks	Yes	Yes	No	Yes
Convergence Checks	Yes	No	No	Yes
Unwanted Messages to deal with	Maximum	Could be slightly less compared to Flat Runs	Low (Many Crossings were nor considered)	Least compared to the other flows

Set up effort required and different kinds of checks which gets covered for different flows

	Flat Run	With ip_block	With IP Blackboxed	Abstract Flow
Run Time	~ 10Hrs	~10Hrs	1 min	15min
Unsynchronized Scalar / Vector crossings	7658/355	7378/249	3/0	8/8
Synchronized Scalar / Vector Crossings	8032/256	1411/24	8/0	88/27

- The SoC Abstract Flow with Power Aware
  - Work on the proposed flow to identify CDC issues in low power designs is in progress.

SUMMARY

- Average 10X improvement in run time.
- CDC Analysis scope focused on the top level.
- No need to modify/re-use IP level waivers.
- With the reduce number of warnings / messages, we were able to quickly identify the CDC issues.
- Additional Convergence checks at the top level which are not checked with ip interface and ip blackbox.
- There are chances of CDC issues getting masked with ip blackbox for the inter-block analysis and can easily lead to bad silicon, whereas with the abstract flow all such crossing would be considered for the analysis.
- Power Aware CDC analysis helps in analyzing the domain crossing with low power structures quite early in project cycle.

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