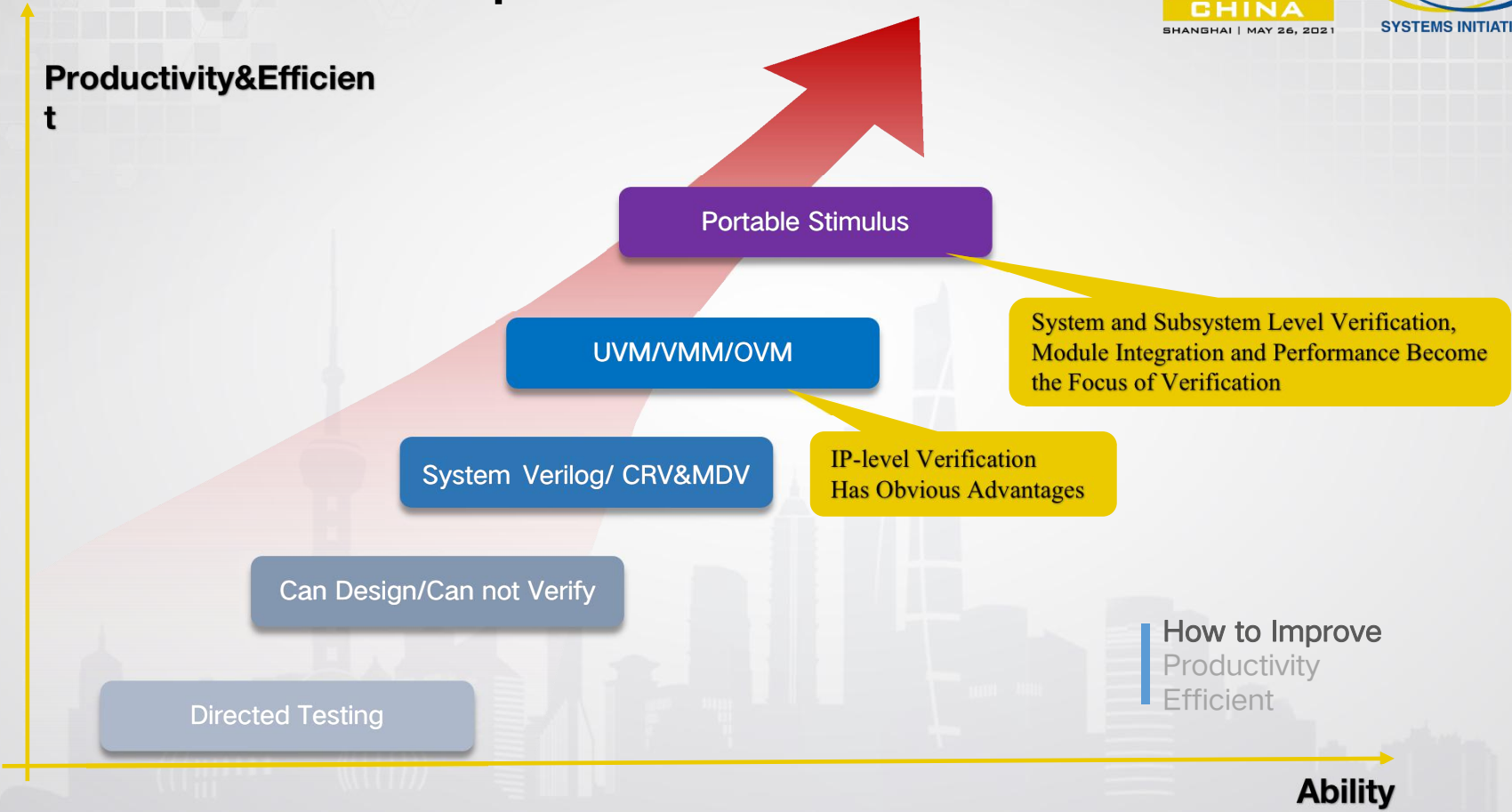


# Cache Coherency Verification for CMP Based on the PSS

Yang Yang



# PSS / SLN / Perspec



# PSS / SLN / Perspec

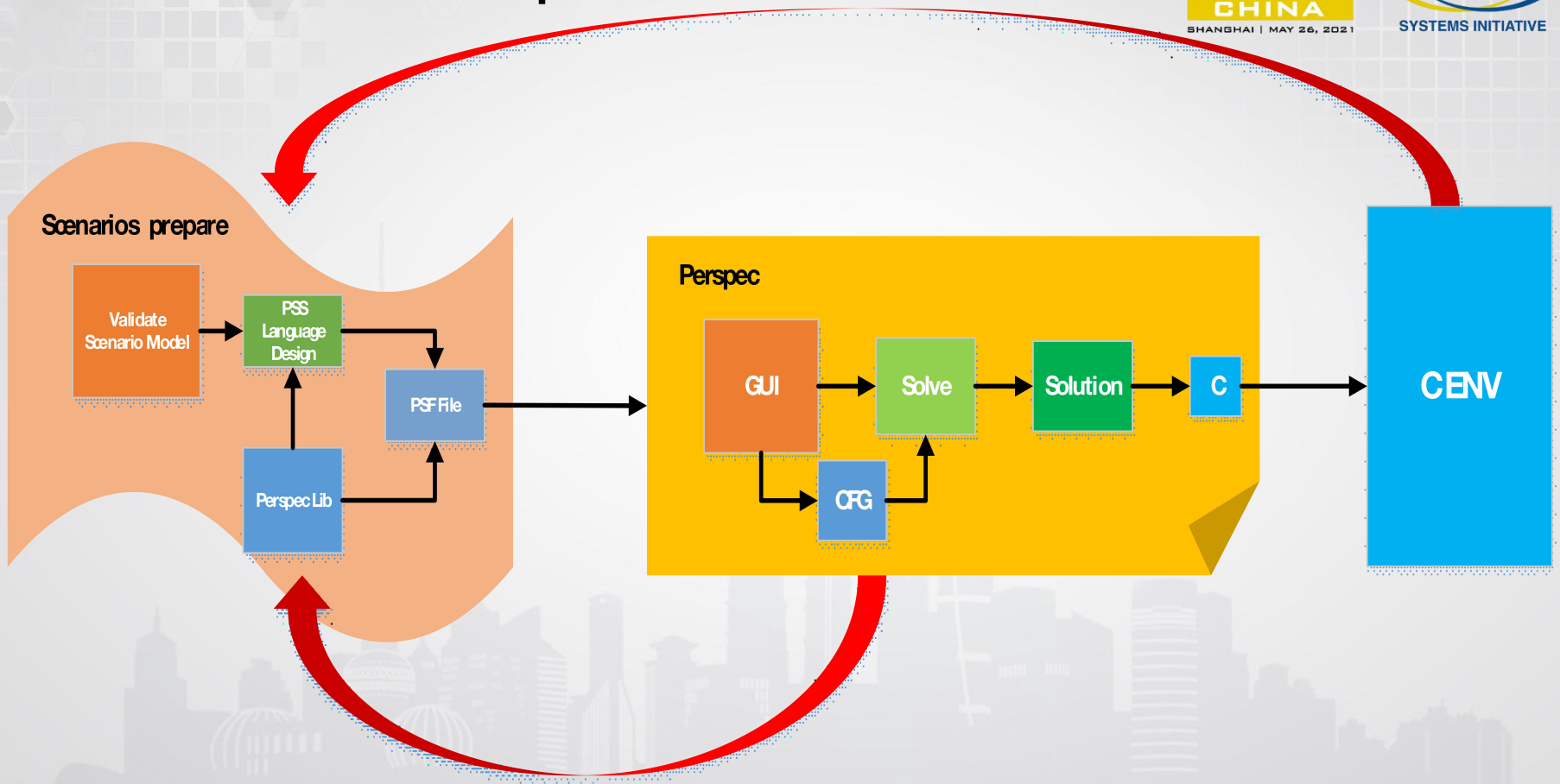


Early Scenario Portable  
Scenario Language  
Specification  
Library scenarios for the ARM  
architecture

PSS parsing tool  
EX : Mentor InFact

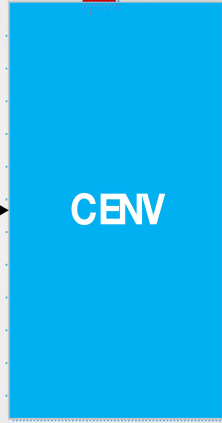
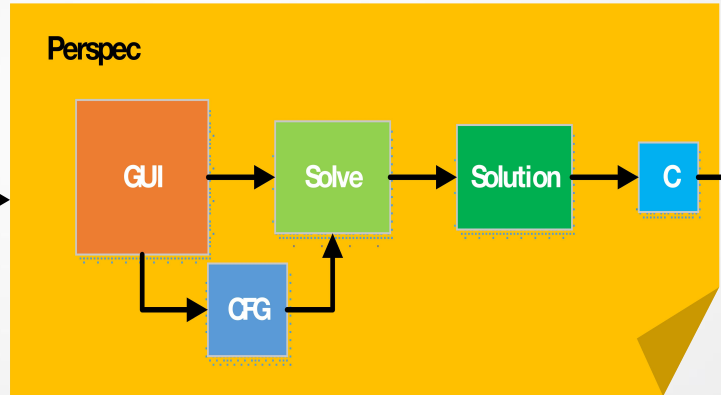
Language syntax standard  
based on scene description  
Reuse SLN syntax rules

# PSS / SLN / Perspec

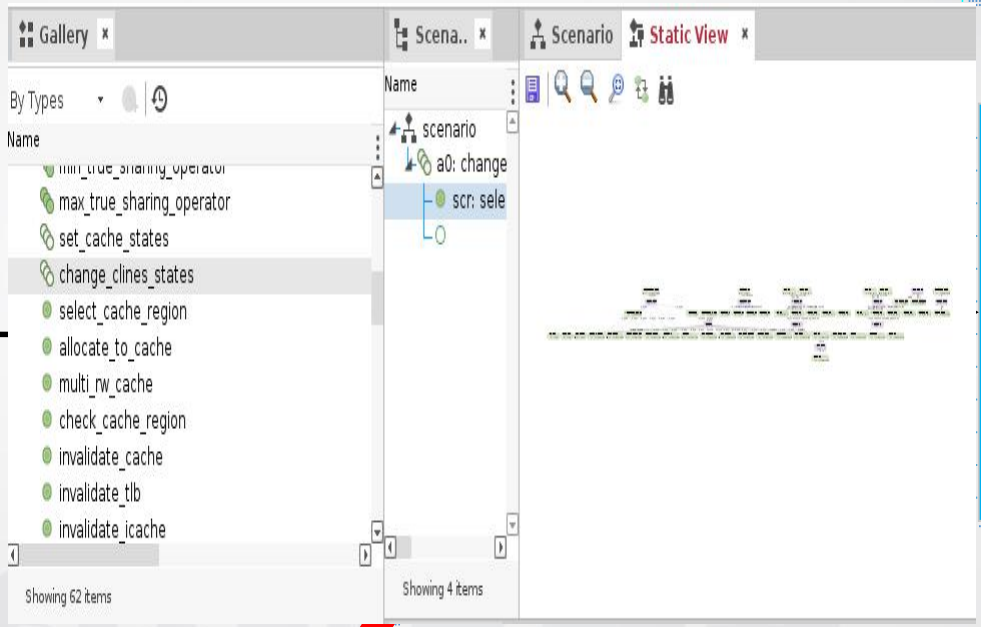
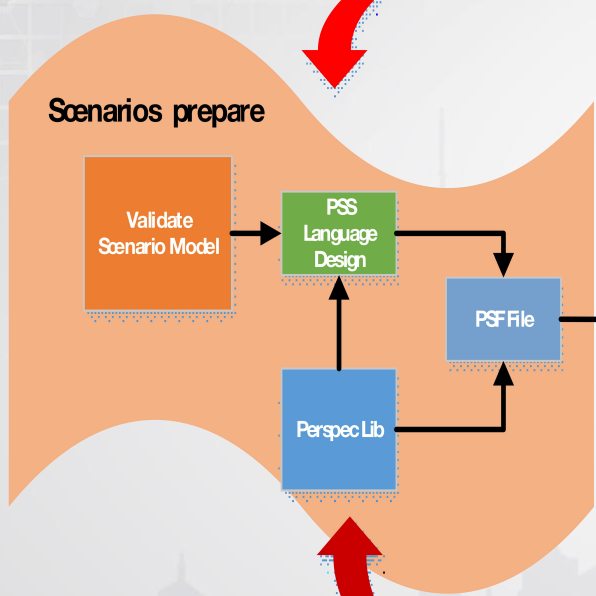


# PSS / SLN / Perspec

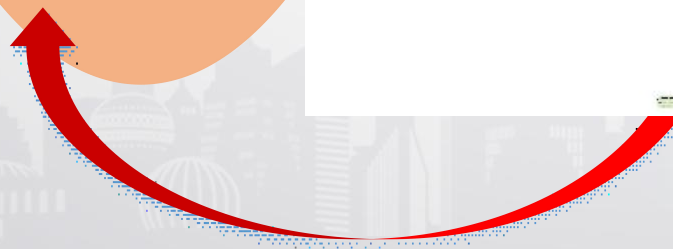
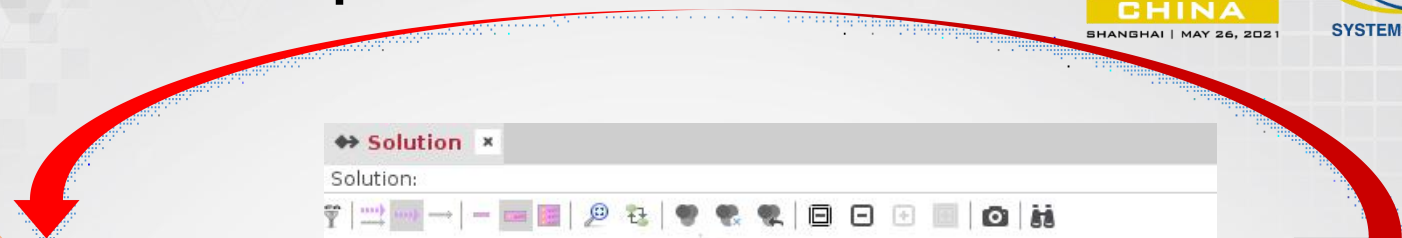
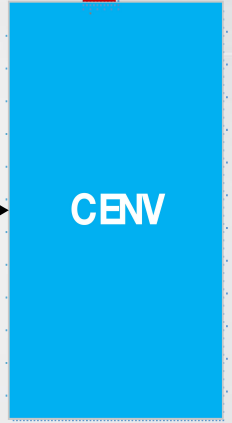
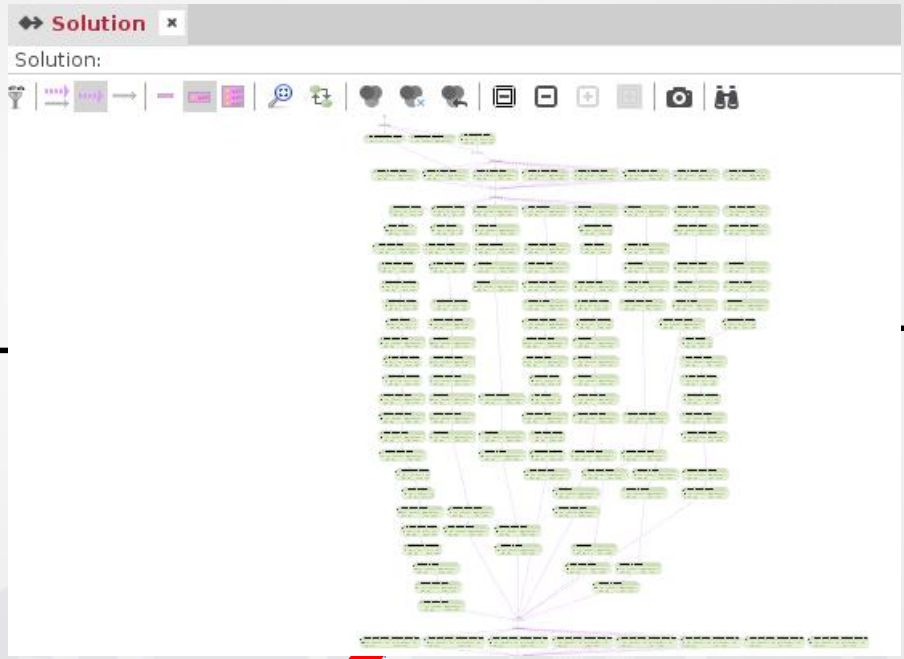
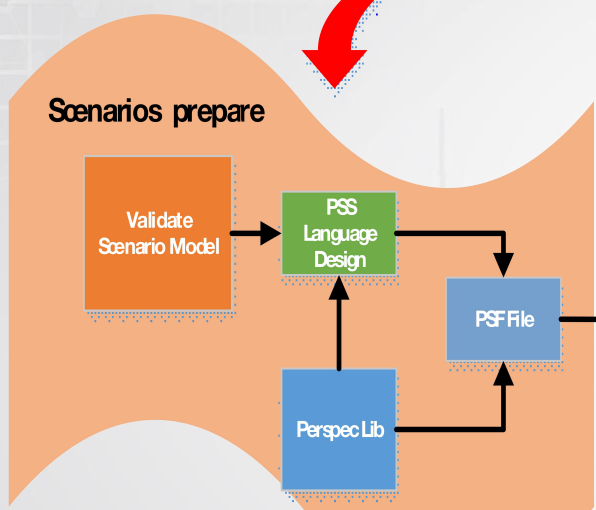
```
false_sharing_random_operator: false_sharing_random_operator
[?] cdn_coherency_ops_c ?
[?] ^num_of_clines ?
[?] ^count ?
[?] external_alloc FALSE
[?] ^procs_subset.selected[]
[?] ^procs_subset.size ?
[?] ^procs_subset.cpu0_core0_selected ?
[?] ^procs_subset.cpu0_core1_selected ?
[?] ^procs_subset.cpu0_core2_selected ?
[?] ^procs_subset.cpu0_core3_selected ?
[?] ^procs_subset.cpu1_core0_selected ?
[?] ^procs_subset.cpu1_core1_selected ?
[?] ^procs_subset.cpu1_core2_selected ?
[?] ^procs_subset.cpu1_core3_selected ?
[?] ^procs_subset.num_clusters ?
[?] ^procs_subset.num_cpu0 ?
[?] ^procs_subset.use_max_cores_cpu0 ?
[?] ^procs_subset.num_cpu1 ?
[?] ^procs_subset.use_max_cores_cpu1 ?
[?] ^procs_subset.minimize_size ?
[?] ^procs_subset.num_coherent ?
[?] ^procs_subset.num_iocoherent ?
[?] ^procs_subset.num_noncoherent ?
procs_subset.apply_power_constraints TRUE
[?] ^exclusive_access ?
[?] ^exclusive_mem_size ?
[?] ^start_with_rw ?
[?] ^use_msgs ?
[?] ^cohfull_procs_alloc_only ?
[?] ^do_allocate_to_cache ?
```



# PSS / SLN / Perspec



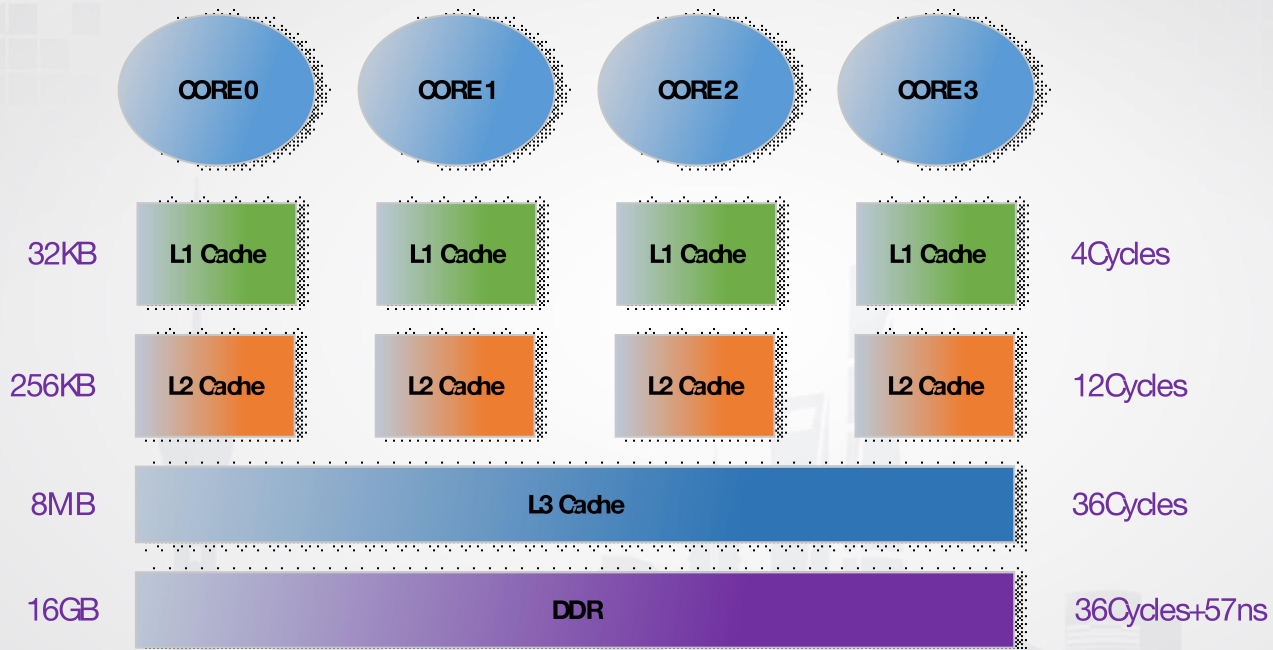
# PSS / SLN / Perspec



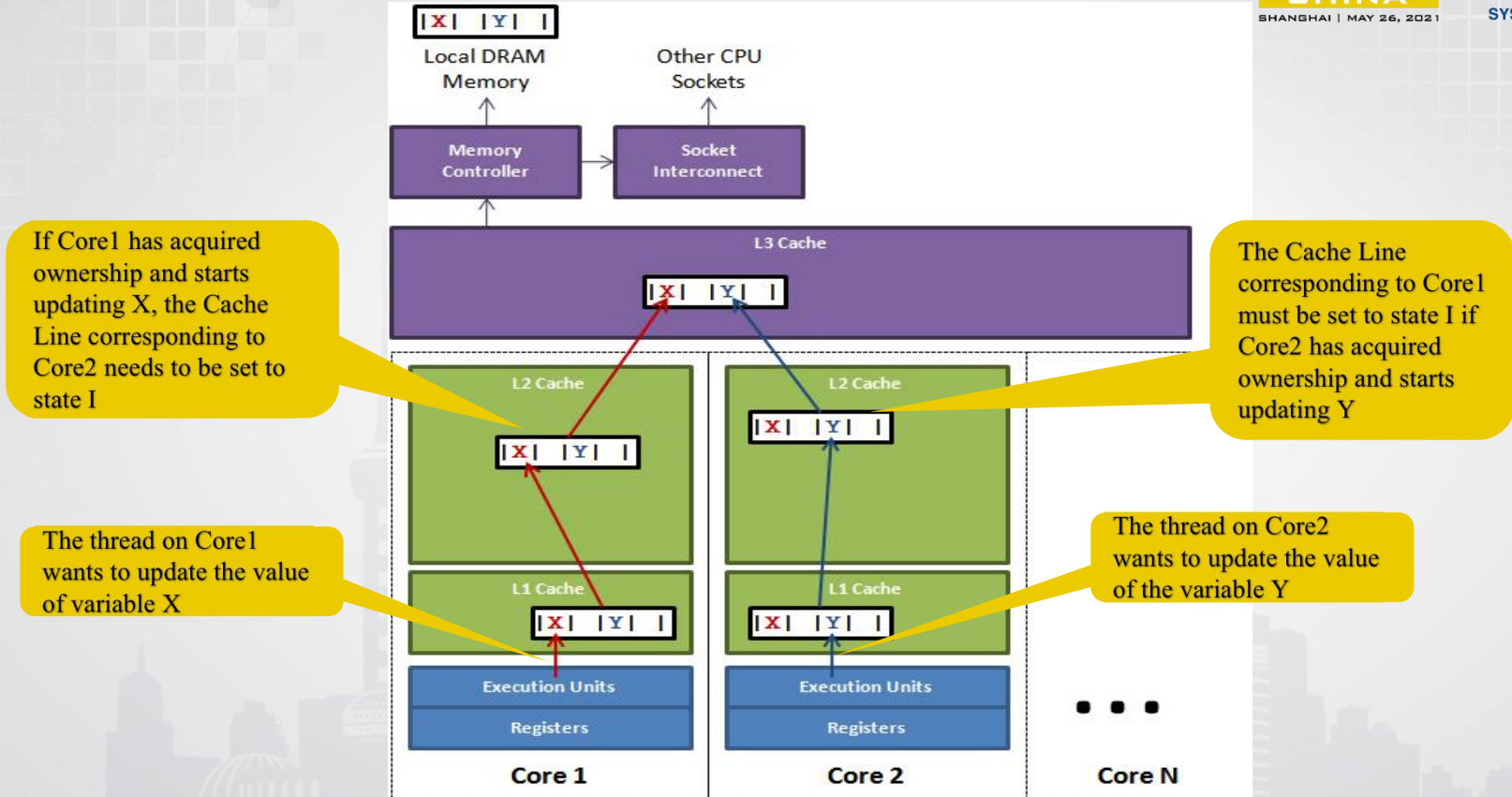




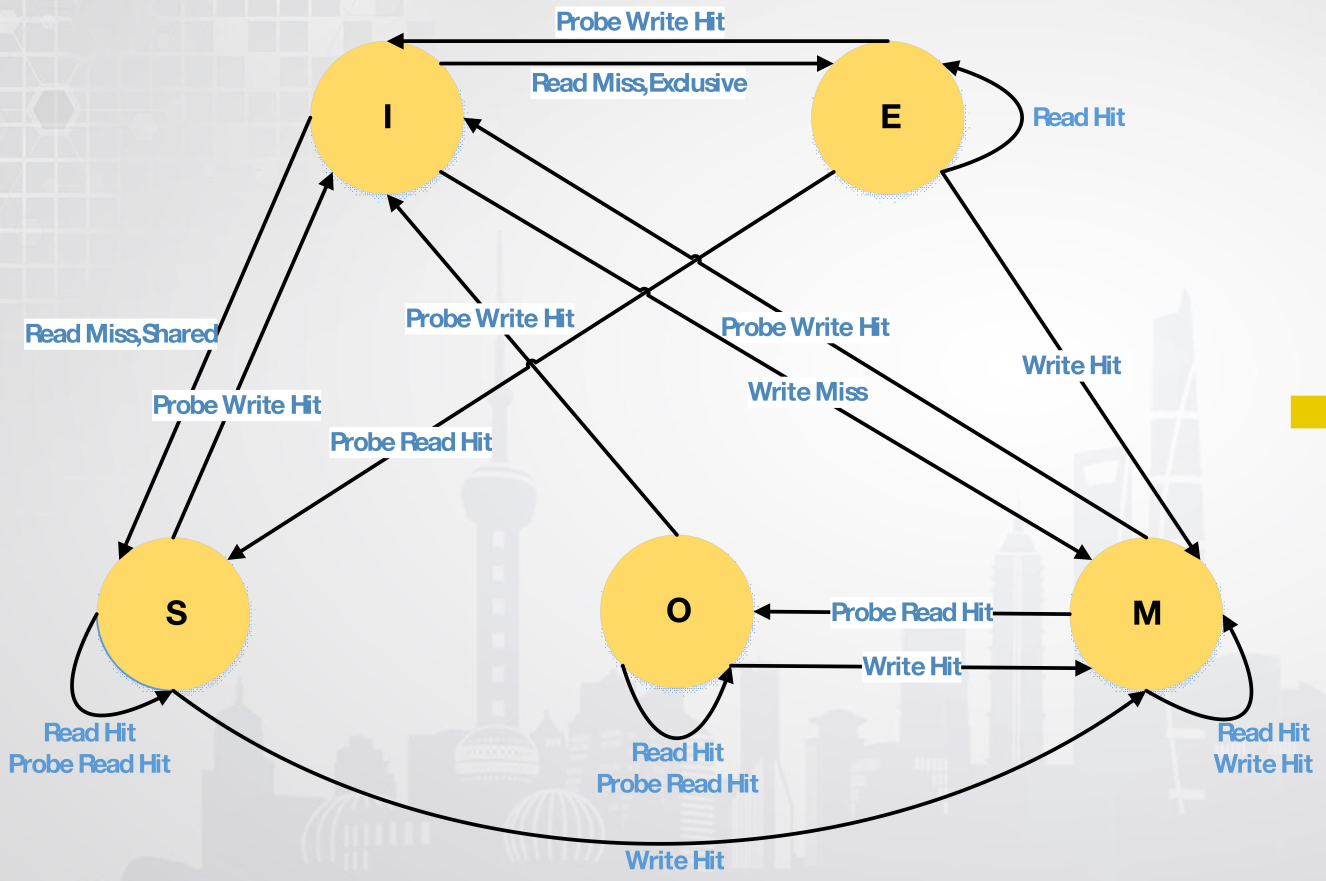
# Cache Coherency



# Cache Coherency

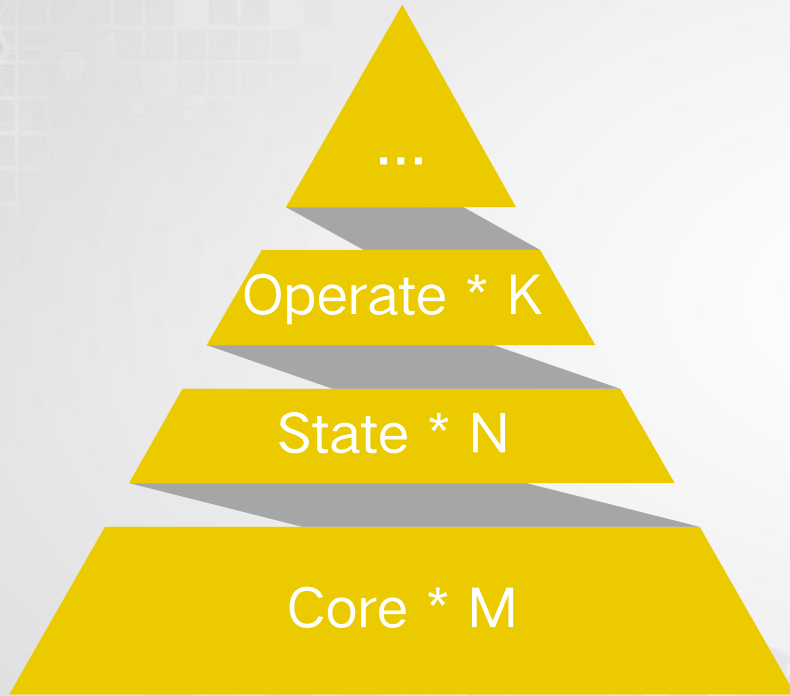


# Verification Model



**State enumeration verification**

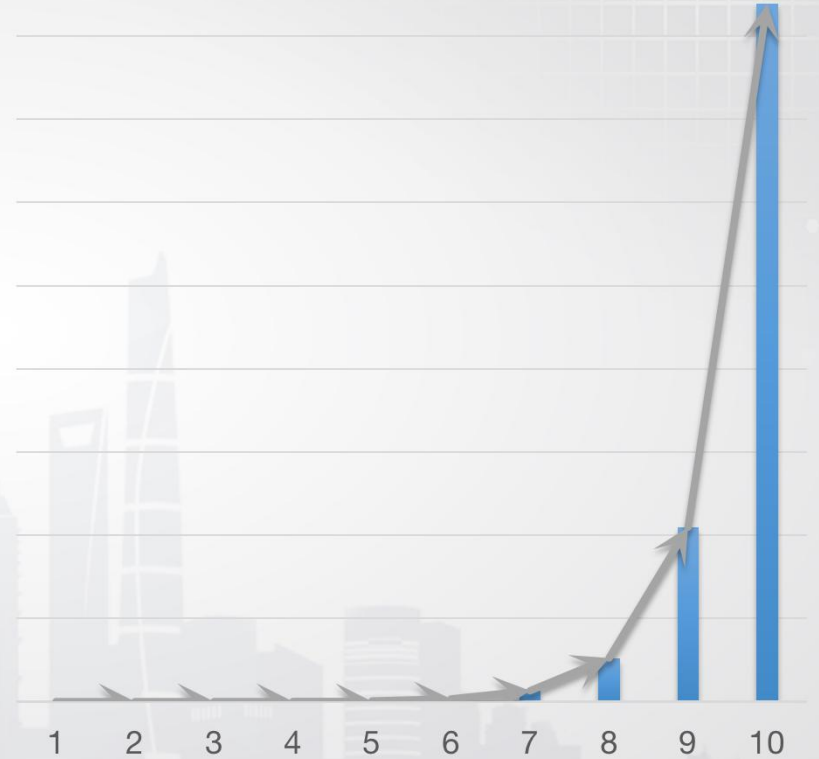
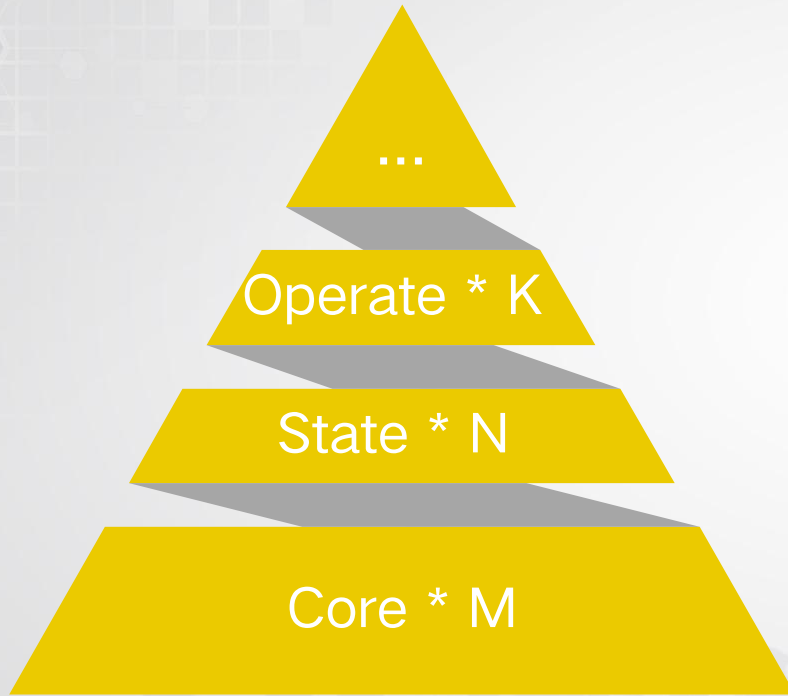
# Verification Model



$$C = K \times N^M$$

$$4 \times 5^8 = 1,562,500$$

# Verification Model



# Verification Model

## Cache Level

L1

L2

L3

## Cache Ability

Device Mem

Non-Cacheable

Cacheable

## Cache Share

Non-Shareable

Outer-Shareable

Inner-Shareable

## Cache Replacement

Random

Prandom

LRU

## Cache Protocol

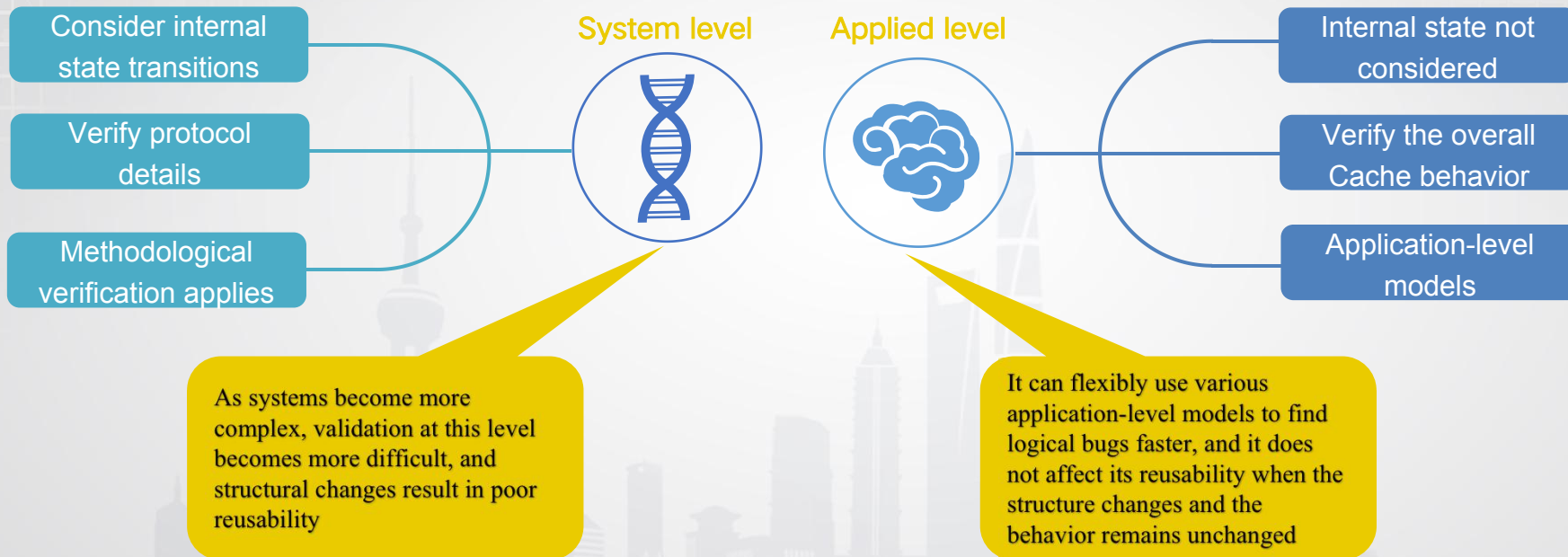
None

MOESI

MESI

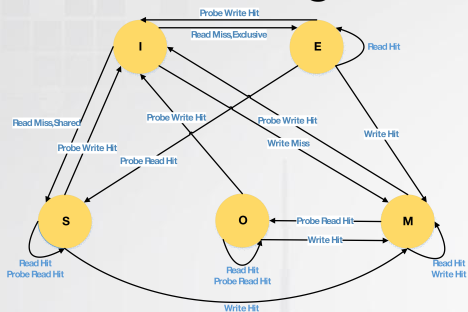


# Verification Model

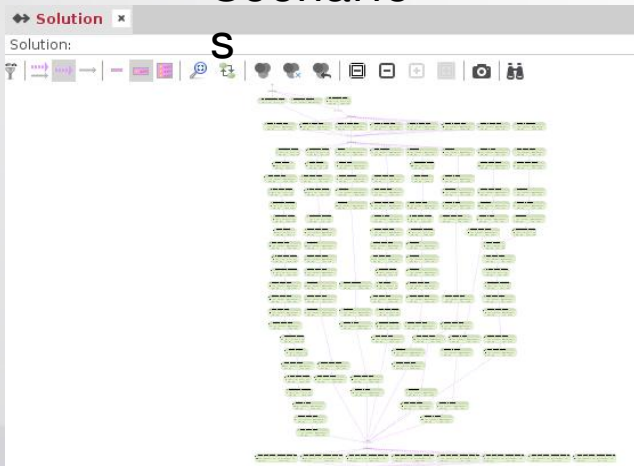


# Verification Model

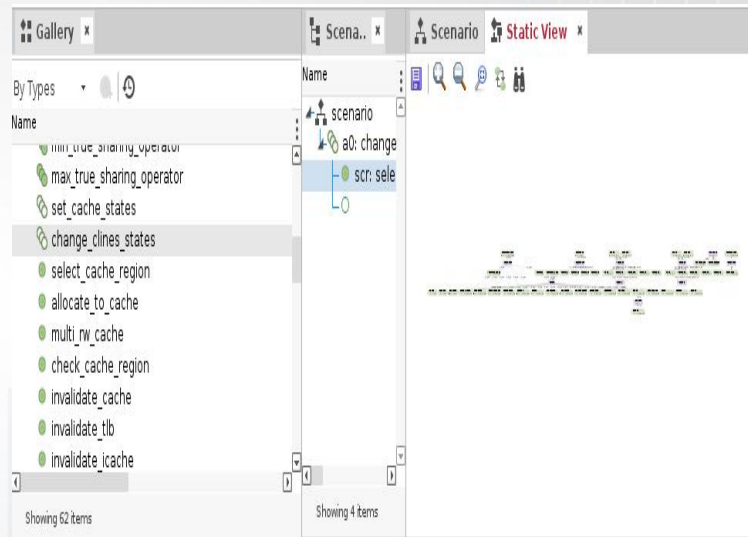
## State Diagram



## Scenario



## Model



## Test Case



# Verification Model



# Plan

## False Sharing

Min False Sharing coherency  
Multi False Sharing coherency  
Max False Sharing coherency

## True Sharing

Min True Sharing coherency  
Multi True Sharing coherency  
Max True Sharing coherency

## Cache State

Debug Cadence Scenarios

## Analyze

Research New Model to Cover State Transition  
Symbol state model method .....

Min is a random 2 cores  
Multi is a random 4 cores  
Max has 8 cores at once  
A Cache Line that accesses the same address

PSS can also be used to test the new model for Cache consistency (Symbolic State Model)

*Thank You !*



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