2021 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION CHINA
SHANGHAI | MAY 26, 2021

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Co-simualtion platform of SystemC and System-Verilog for algorithm verification

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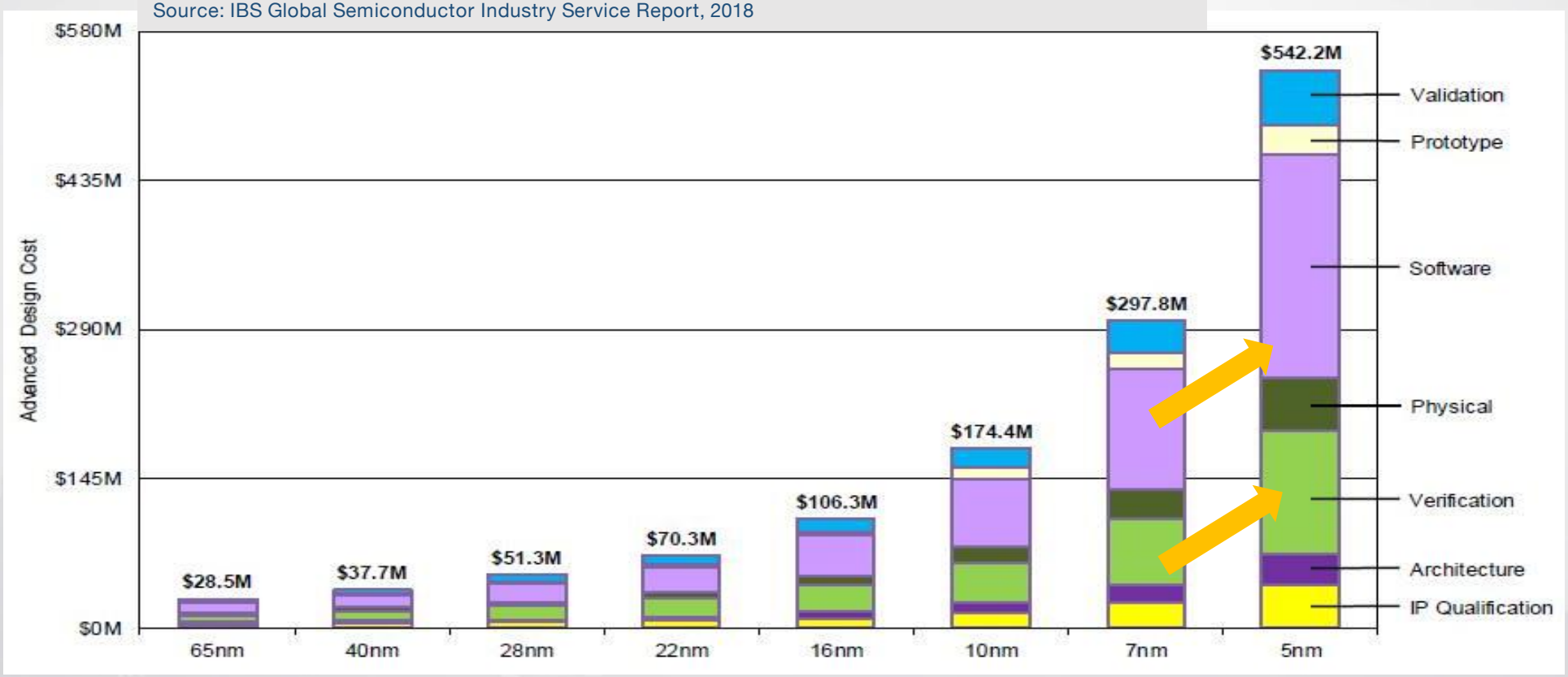
Agenda

- Current Verification Challenges
- Why SystemC
- The SystemC model of compression algorithm
- Verification with SystemC
- C/C++ vs. SystemC model for Verification
- Advantages of Co-sim Platform of SystemC and System-Verilog

Current Verification Challenges

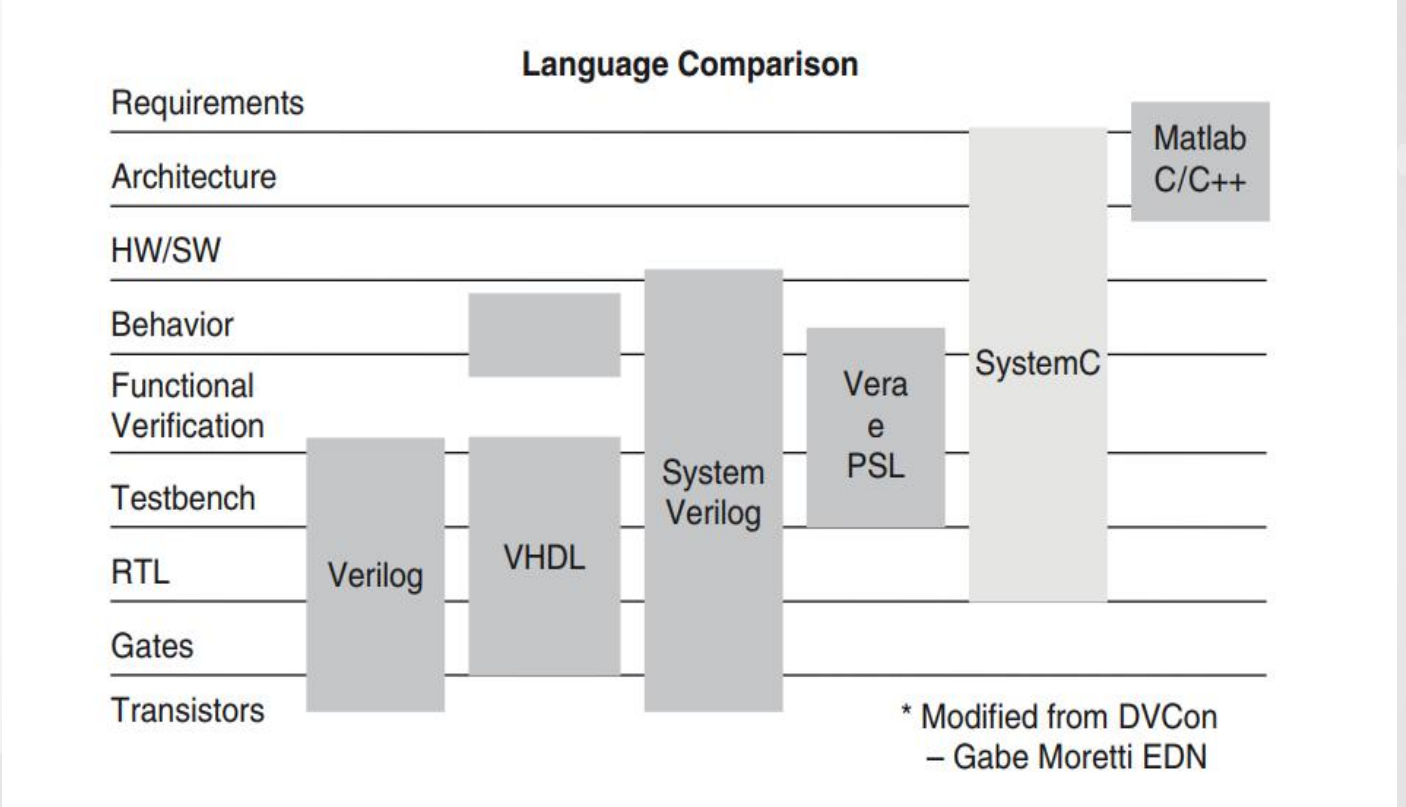
- increasing complexity of SoC design
- time to market is getting shorter and shorter
- verification growth in cost and schedules

Source: IBS Global Semiconductor Industry Service Report, 2018



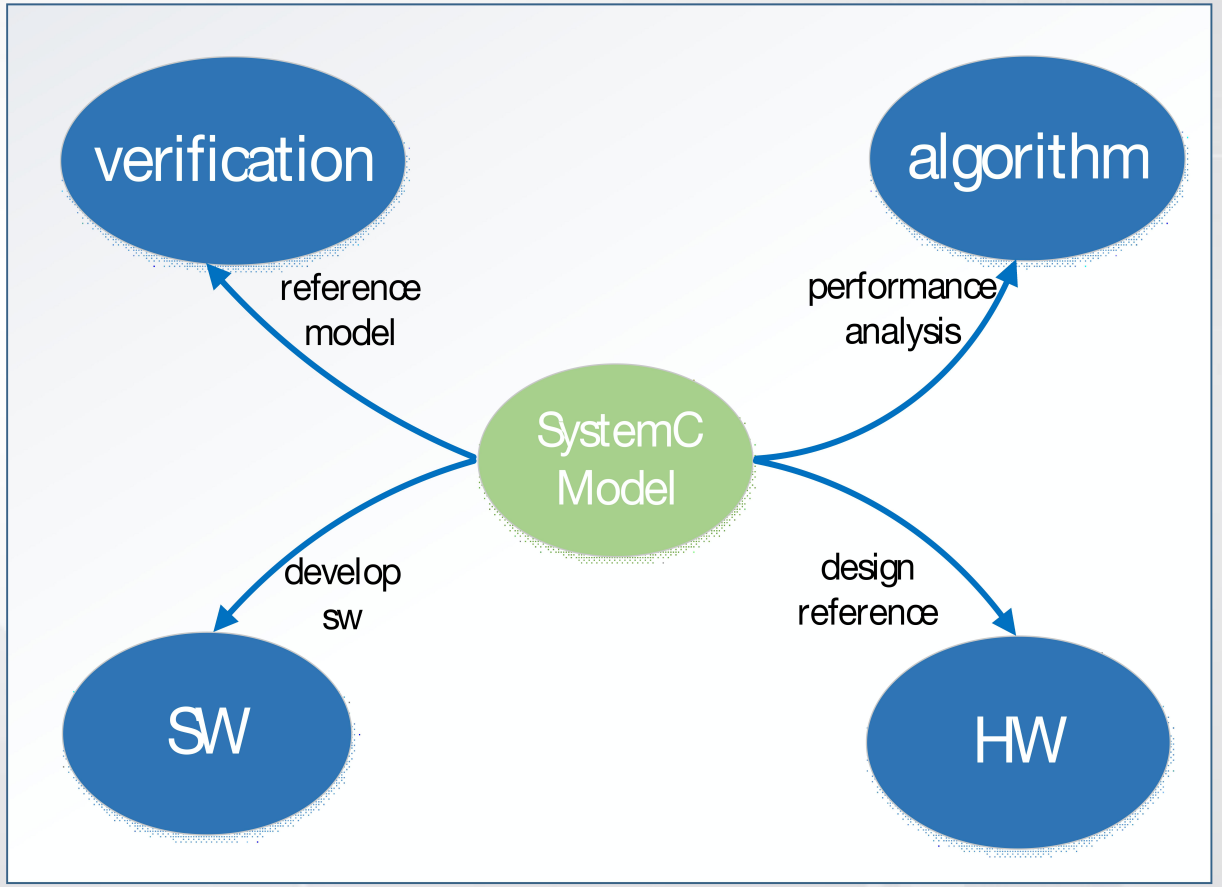
Why SystemC

- extended library of C++
- hardware-oriented features
  - Time model
  - Hardware data types
  - Module hierarchy to manage structure and connectivity
  - Concurrency model
  - Communications management between concurrent units of execution



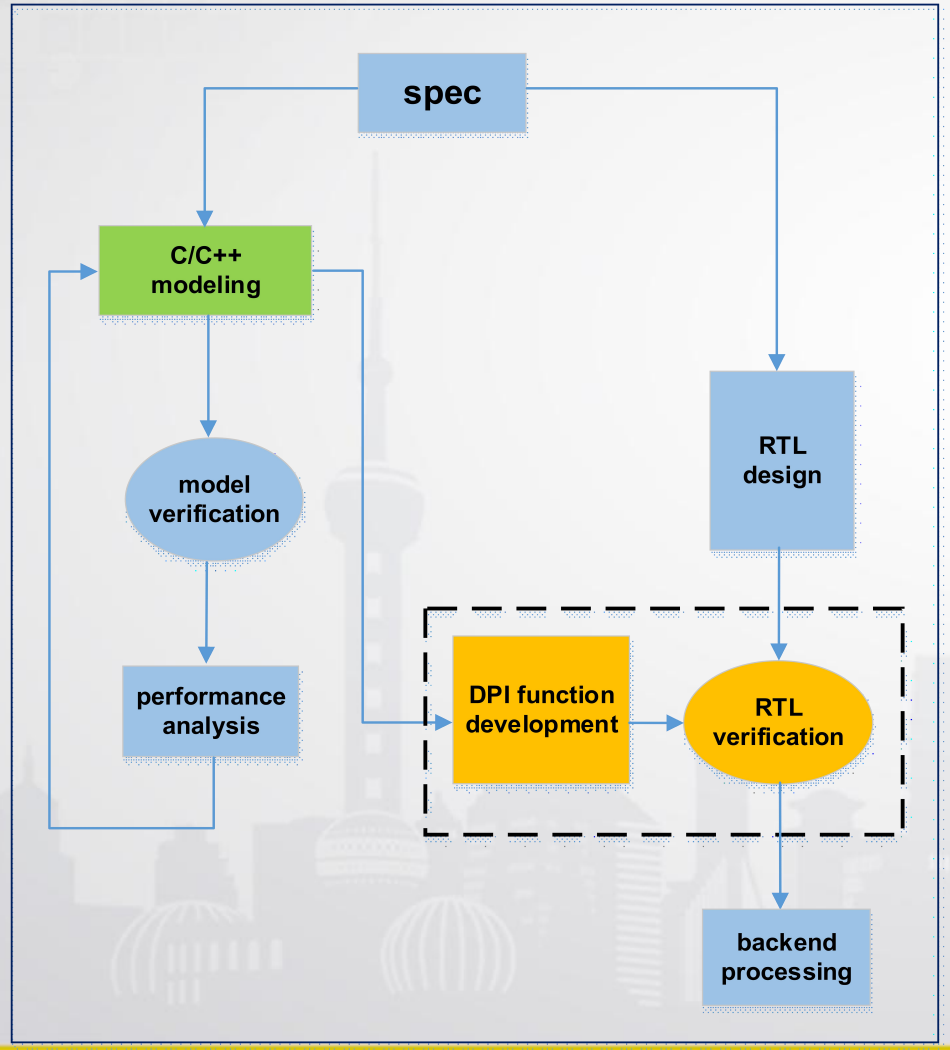
Why SystemC

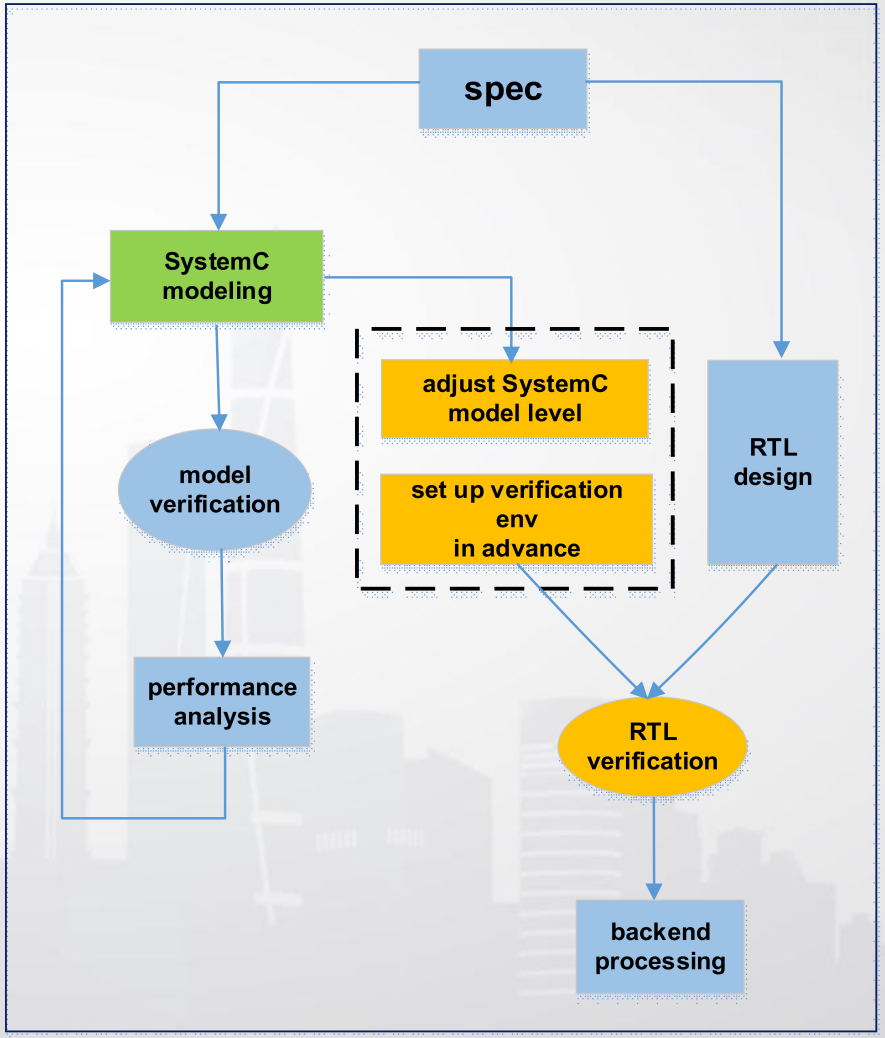
- Support modeling at different levels of abstraction
  - ALM
  - SAM
  - TLM
  - RTL
- highly reused in the development of SoC
- as a bridge between various departments



Why SystemC

- C/C++ vs. SystemC for development processes

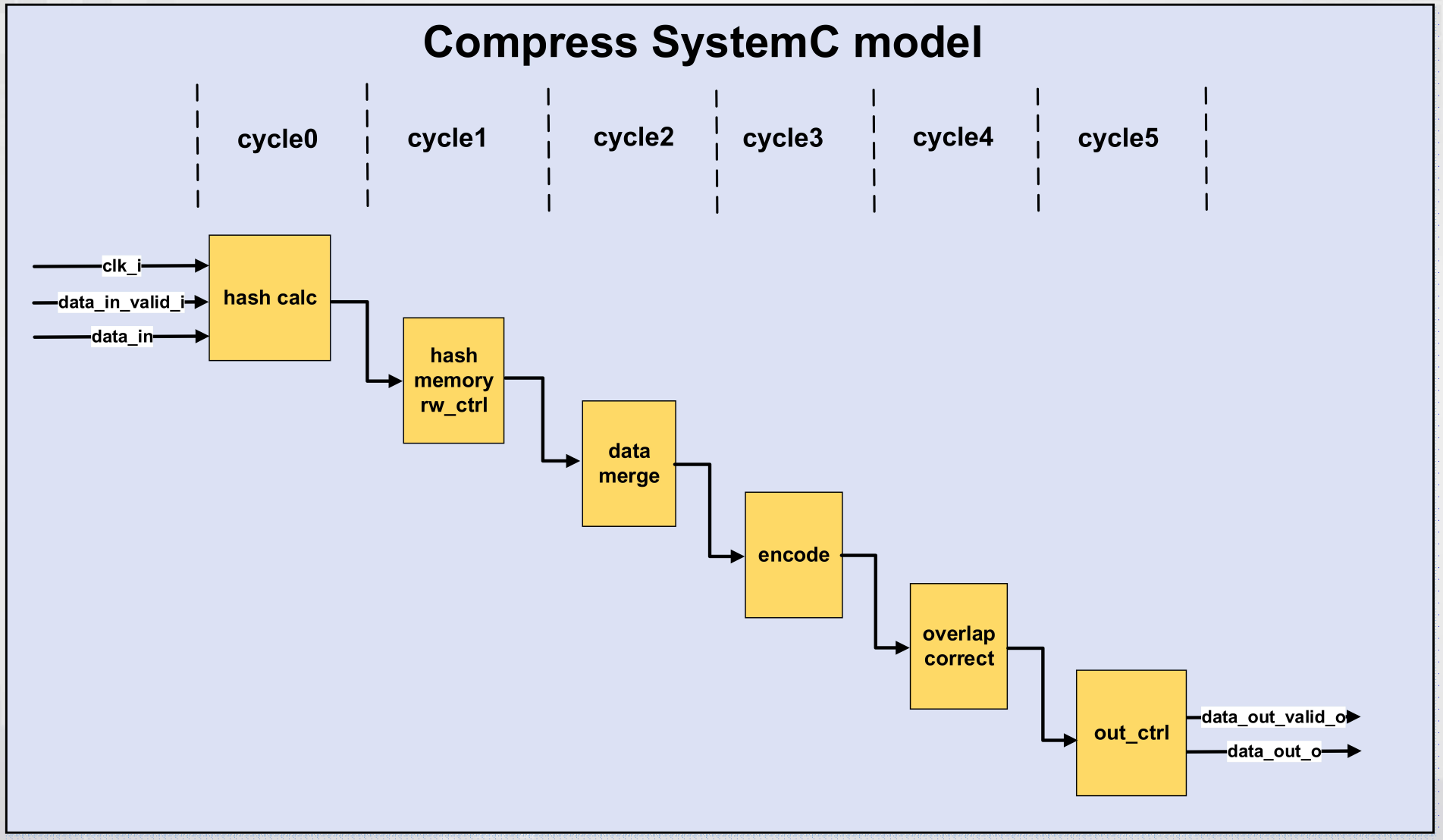




The SystemC model for compression algorithm

- **algorithm requirements**
  - Original algorithm is to find a possible matching character byte by byte, can only process one byte of input data per cycle
  - Need to increase the data throughput rate, explore the parallelization of hardware implementation, process more data in one cycle
  - Limited memory resources, HW architecture has no input buffer
  - Pipelined processing methods are used to implement a forward and branch-free algorithm

The SystemC model for compression algorithm



The SystemC model for compression algorithm

performance analysis					
File	QAT	initial arch	updated arch		
		SRAM 240KB	SRAM 1152KB	SRAM 576KB	SRAM 288KB
		ratio	ratio BW12_C12	ratio BW11_C12	ratio BW10_C12
dickens	1.659	1.449	1.58	1.652	1.592
mozilla	2.188	1.853	1.966	1.953	1.922
mr	1.992	1.754	1.91	1.905	1.875
nci	5.765	2.681	4.36	4.356	4.34
ooffice	1.618	1.453	1.53	1.521	1.489
osdb	1.89	1.710	2.22	2.131	1.86
reymont	2.207	1.736	1.96	1.941	1.902
samba	2.889	2.079	2.73	2.696	2.61
sao	1.158	1.188	1.18	1.173	1.162
webster	2.165	1.808	2.18	2.154	2.092
x-ray	1.136	1.057	1.124	1.107	1.072
xml	3.714	2.641	3.73	3.875	3.772
average	2.247249	1.823031	2.131843	2.119311	2.061693

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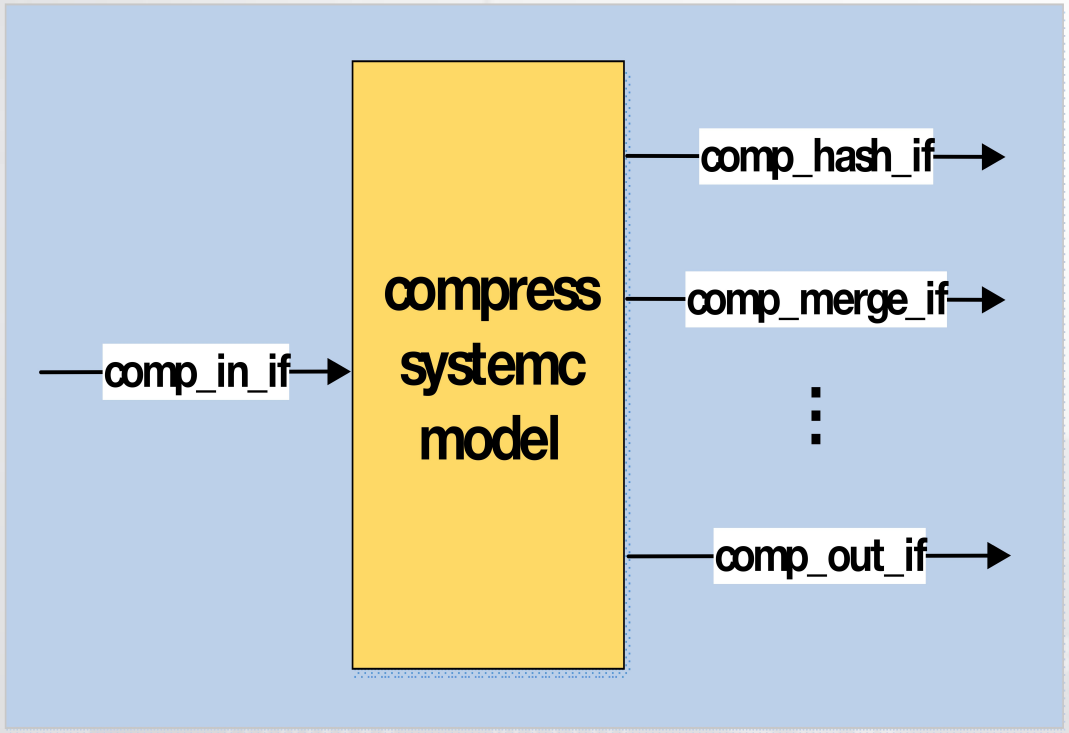
Verification with SystemC

Verification with SystemC

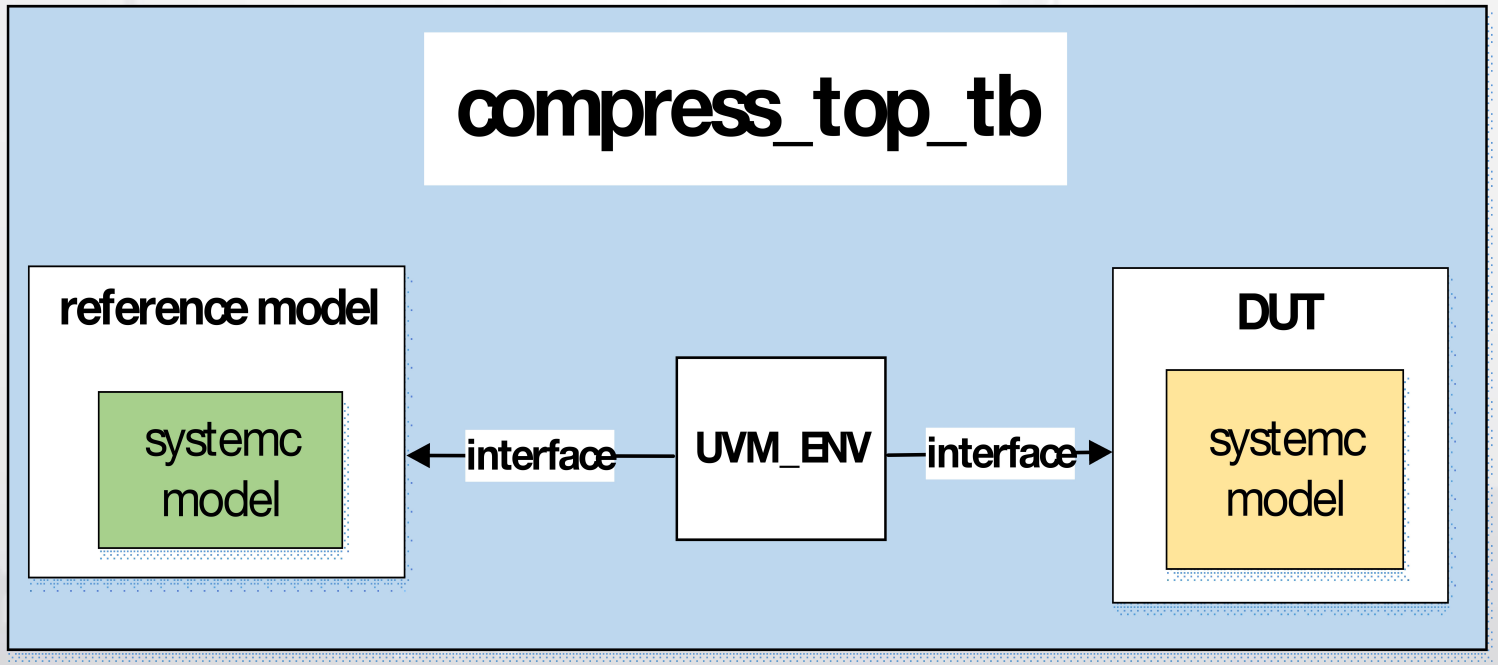
- Build a pin-level algorithm model



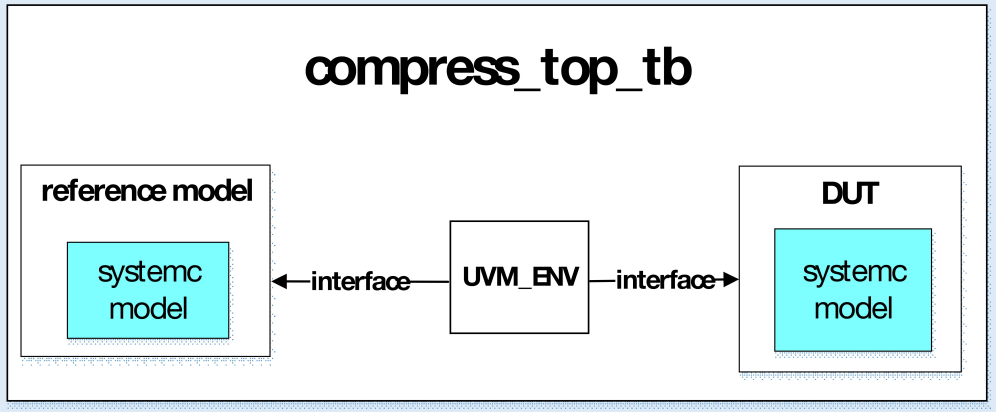
  - The interface timing of the model is exactly the same as the RTL ;
  - Output intermediate results through the SystemC out port for debugging

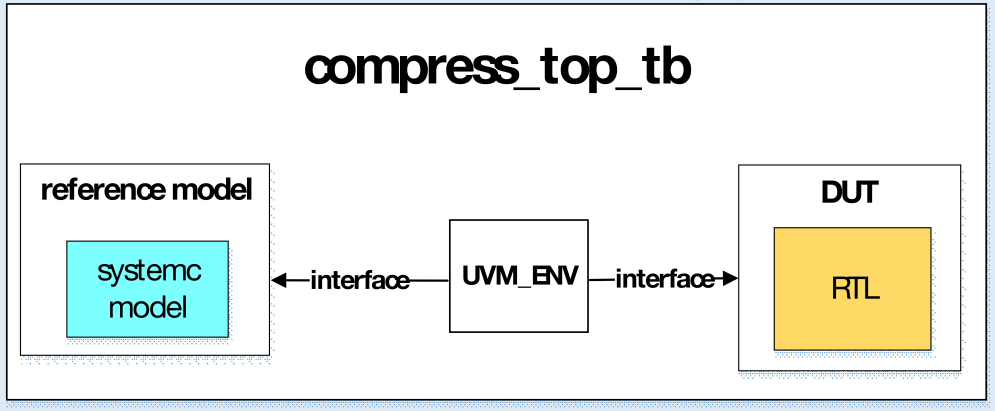
Verification with SystemC

- Use the SystemC model to build UVM TB in advance
  - Before RTL is available, the SystemC model can be used as a DUT to build TB for preliminary verification



Verification with SystemC





- Verify the real RTL
- Upgrade the verification environment

Verification with SystemC

- EDA tools such as VCS has built-in support for SystemC.
- When integrating the SystemC model into the System-Verilog environment, just instantiate the model like an RTL module

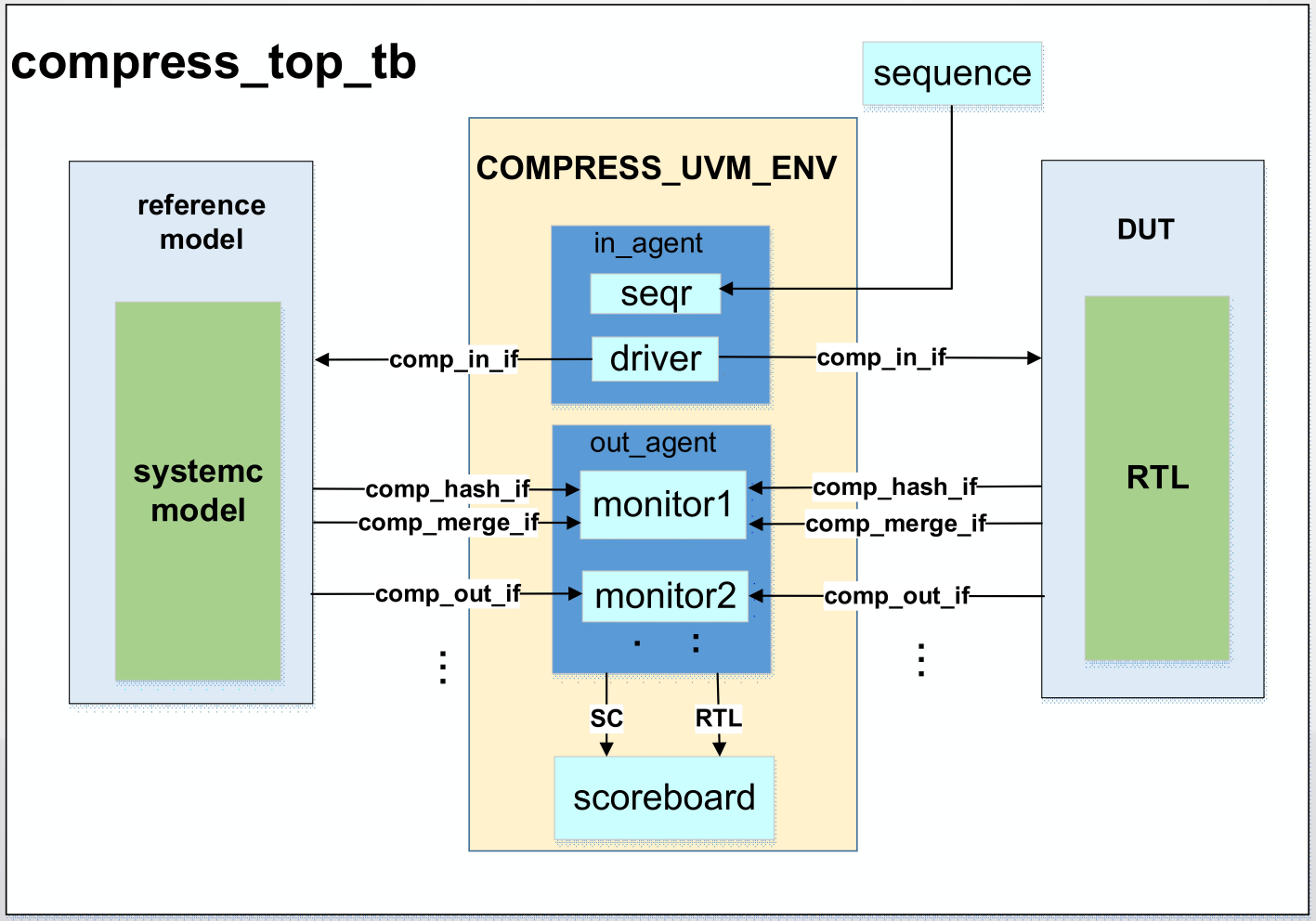
```
//compress_top_tb.sv
//DUT
compress_top_dut compress_top_rtl (
.clk_i            (clock)
.block_in_size_i   (comp_in_if.block_size)
.block_in_type_i   (comp_in_if.block_type)
…
.data_out_type_o   (comp_out_if.rtl_data_type)
.data_out_o        (comp_out_if.rtl_data)
…
);

//SC reference model
compress_top_sc compress_top_sc (
.clk_i            (clock)
.block_in_size_i   (comp_in_if.block_size)
.block_in_type_i   (comp_in_if.block_type)
…
.data_out_type_o   (comp_out_if.sc_data_type)
.data_out_o        (comp_out_if.sc_data)
…
);
```

instantiate RTL

instantiate SystemC model

Verification with SystemC

- Co-sim platform of SystemC and System-Verilog



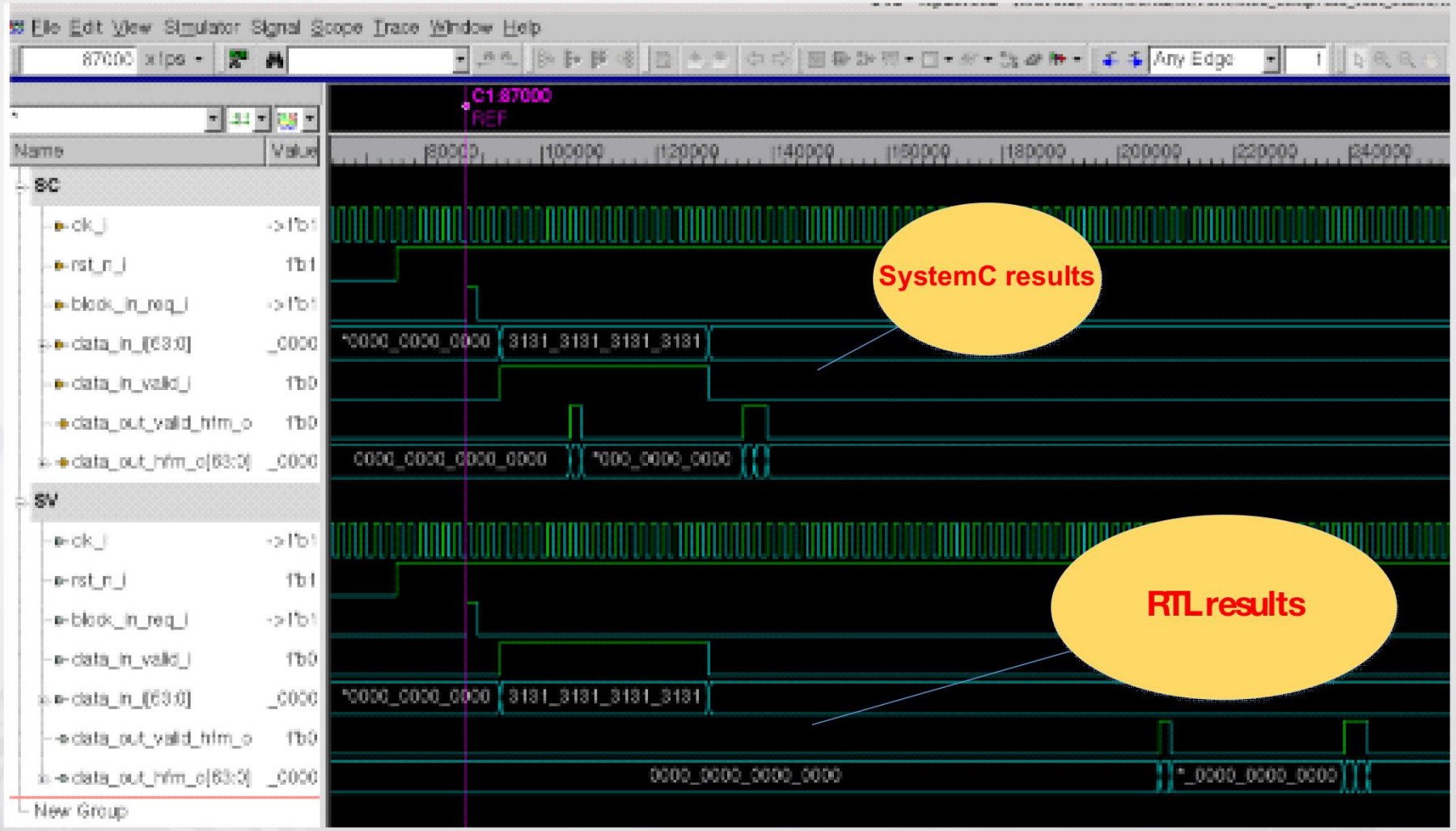
Verification with SystemC

- simulation command with VCS

```
//Compile Systemc:
syscan –cpp g++ -cc gcc –cflags –g –full64 $(SC_SRC)

//Compile System-Verilog:
vlogan –full64 –sverilog $(SV_SRC)

//elaboration
vcs –full64 –cpp g++ -cc gcc -sverilog –sysc SV_TOP_TB
```

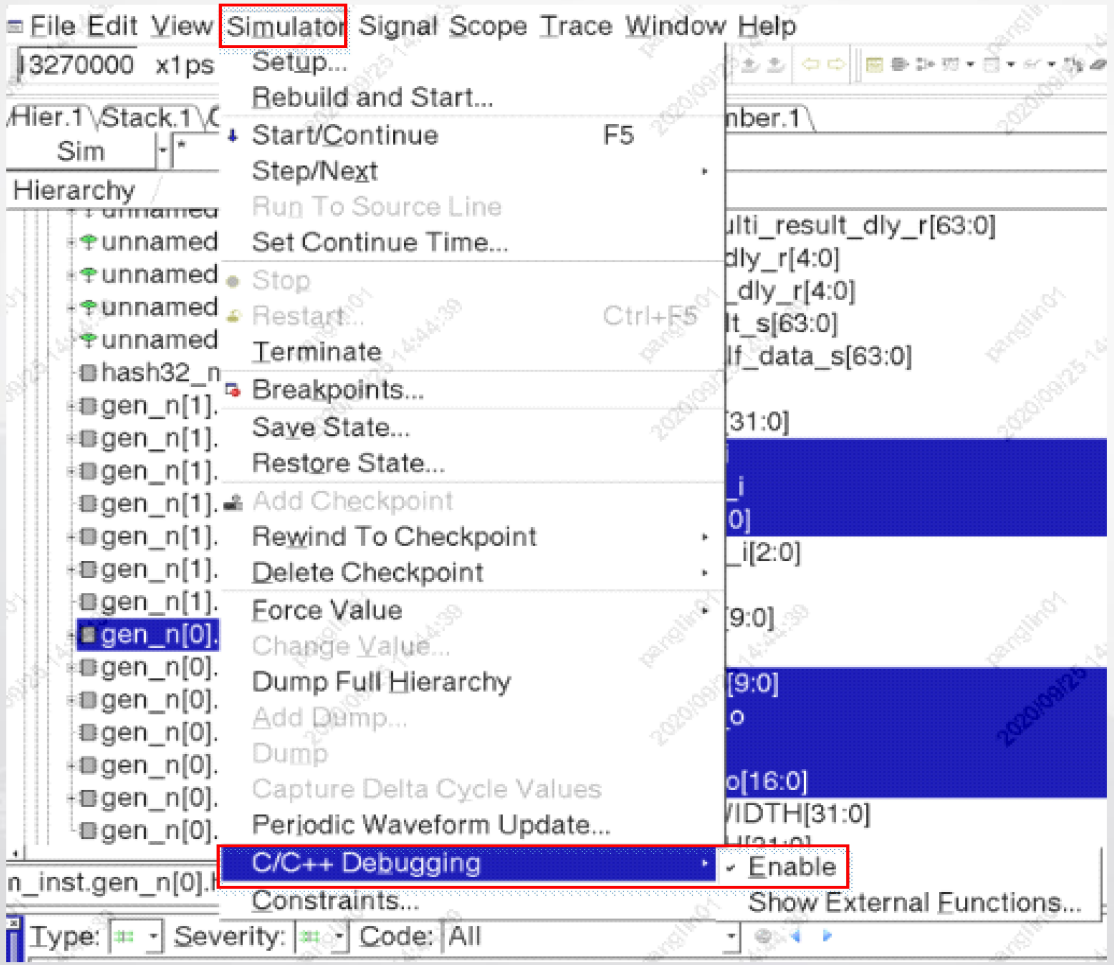
Verification with SystemC

- simulation results



Verification with SystemC

- debug SystemC model with VCS Cbug

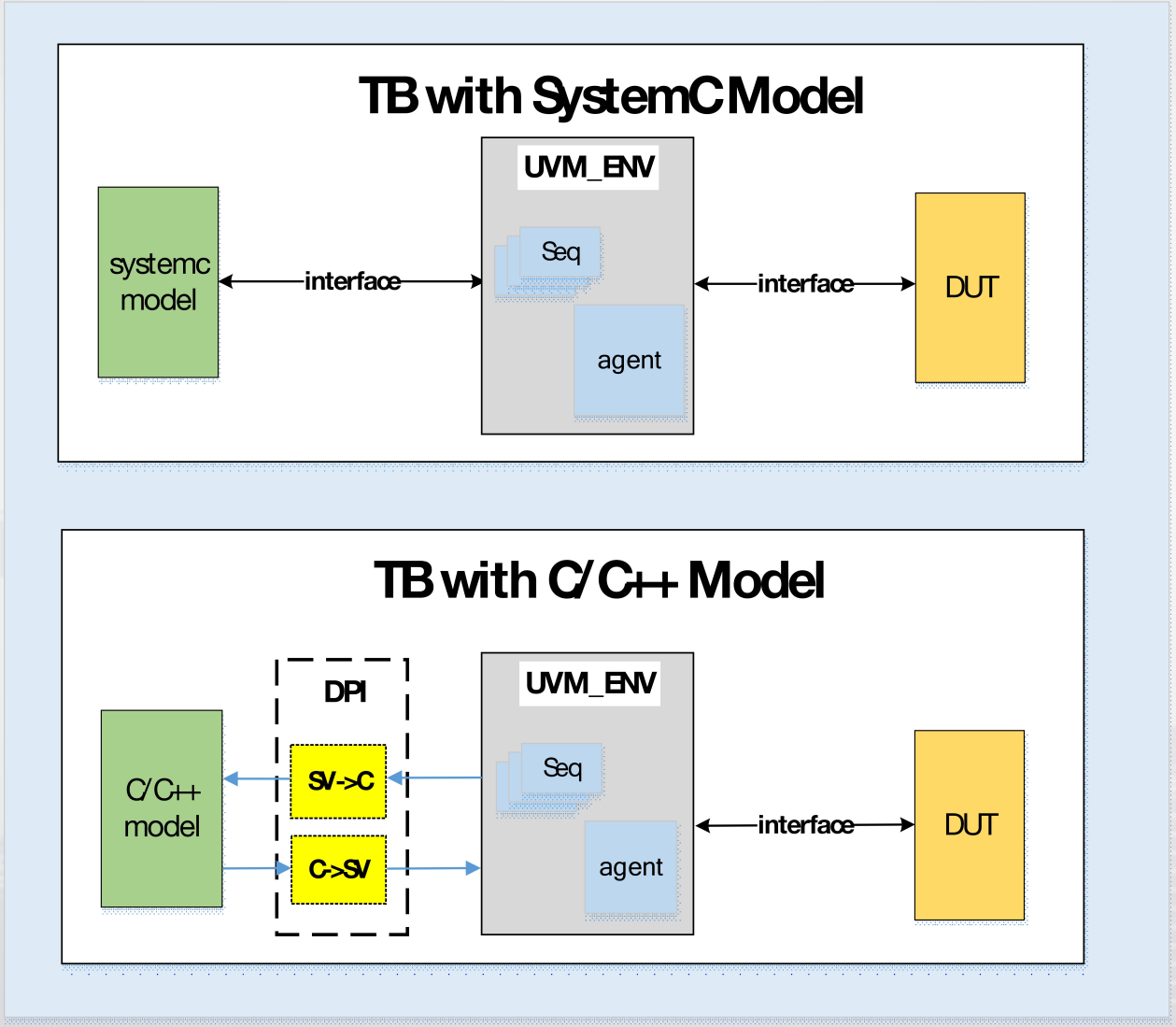


Verification with SystemC

- VCS SystemC co-simulation interface
  - Enables Verilog,VHDL and SystemC modeling to work together
  - Supports for Verilog-top/SystemC-top/multiple-top topology
  - VCS Extensions to SystemC Library, such as get_full_name()…
  - Unified compilation/simulation/debug flow
  - Transaction Level Interface (TLI) enables integrating transaction level SystemC models into a SystemVerilog environment seamlessly and efficiently

Advantages of Co-sim Platform

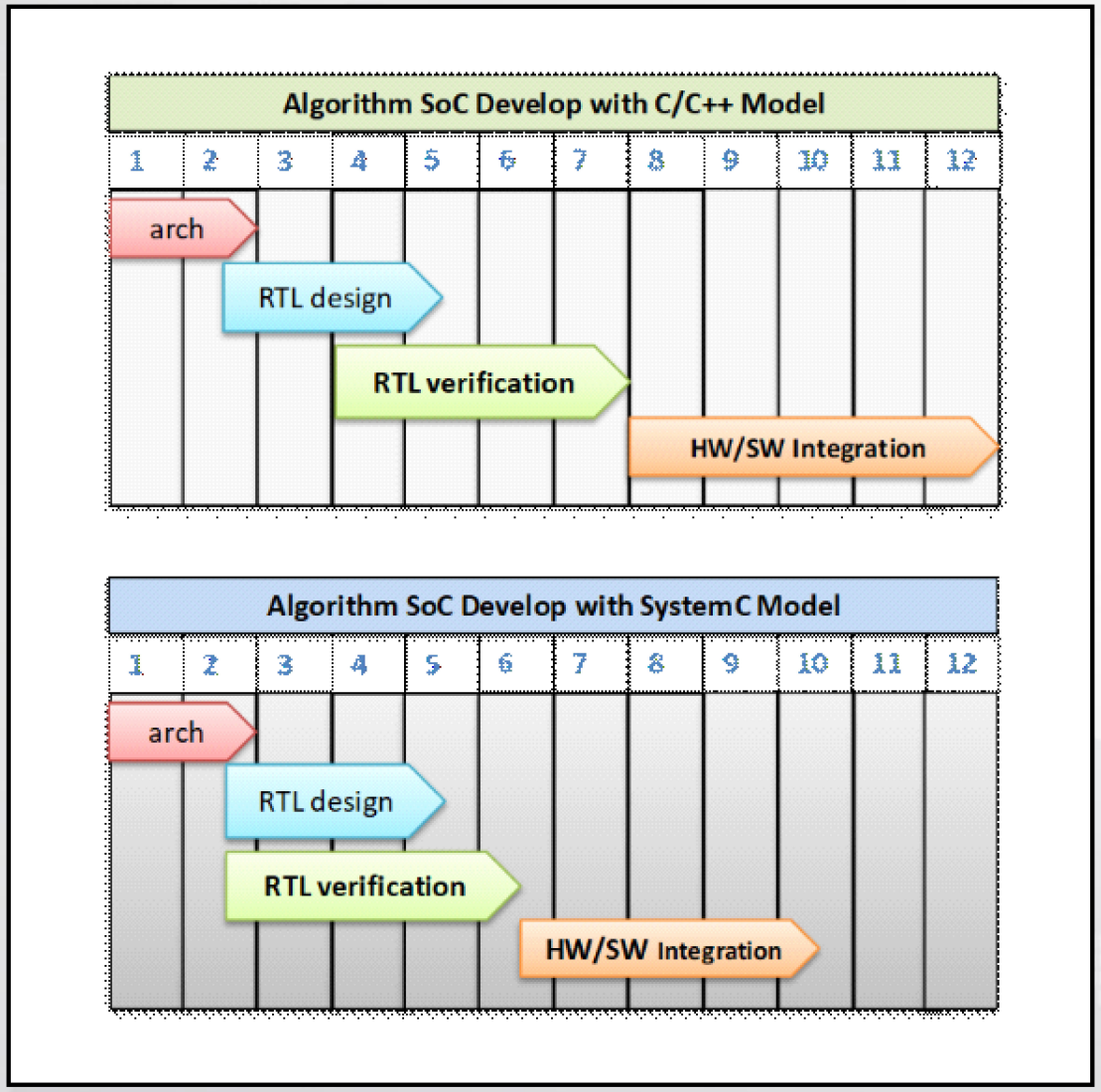
C/C++ vs. SystemC model for Verification



C/C++ vs. SystemC for Verification

items	C++	SystemC
integration	Develop DPI-C function	As simple as instantiating RTL
driver	Call the DPI function in the test case	Driven by the same driver of RTL
checker	Need to store the results of C/C++ model Take up additional storage space	Monitor the results through interface
debugging	Internal variables are difficult to debug Dump variables to files or use breakpoints	Output key variables through SystemC ports or signals

Verification start earlier



Verification can start at least 1 month in advance

The reusability of SystemC model is high

Be reused by Arch/HW/SW team

Be easily reused for module/sub-system/SOC verification

When the RTL of some modules has not been delivered, SystemC model can be used to start sub-system or SOC level verification

Summary

items	C/C++ Model	SystemC Model
Model integration time	About 3 days	Less than 1 day
Debug	difficult	easier
Verification start earlier	No	Yes
Verification reusability	low	high

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