Justin Refice,

Version: Final 1.0

## **OVM** TO **UVM** DEFINITIVE **G**UIDE **P**ART **1**

*Abstract-* The Universal Verification Methodology (UVM) is an industry standard maintained and developed by the Accellera technical subcommittee for verification intellectual property (TSC-VIP). The UVM standard consists of SystemVerilog IEEE 1800 compliant reference library along with a technical reference manual and a VIP engineer's user guide.

UVM is constantly maturing and as OVM based projects come to end everyone is asking how they should move to use UVM for the next project. At AMD there is a long term strategy to migrate all projects using OVM code to UVM. Based on the knowledge within the methodology team there has been several successful SoC code-upgrades each containing numerous subsystems with dozens of IP block projects.

During OVM's short life span, it went through a multitude of revisions and lots of bug fixes. Many other issues and bugs were never resolved in OVM which created divergence in the user community as verification teams created their own solutions. UVM not only fixes several open bugs from OVM but also draws from VMM to address many of the basic features required for verification that were left unanswered by OVM.

The definitive guide is split over two parts. This paper is part one, a practical aid for the users who are upgrading from OVM to UVM. There will be a subsequent paper namely "Part Two" which addresses methodological modifications required to upgrade from OVM to UVM.

### I. INTRODUCTION

When upgrading from OVM to UVM there is more than just syntax and semantics that need to be modified. In this paper we will discuss for each major section of the UVM's base classes how to upgrade syntax from OVM to UVM, covering explanations as how to move forward with UVM.

The starting point of UVM code base was created by an automation script that performed a renaming of keywords, from the OVM base class library. The script was the first OVM to UVM renaming technology developed and was donated to Accellera. Subsequently, Accellera members have enhanced, modified, rewritten and renamed the original script, OVM UVM Rename.pl to ovm2uvm.pl. Unfortunately, these scripts quickly became outdated as UVM moved forward and they cannot take code from OVM to UVM-1.X version. There are other scripts and technologies in the industry that can automate much of the process. However, automation is not a substitute for knowing what and why changes are occurring. It is not the purpose of this paper to provide an automated script, but instead to provide the user with the knowledge as to what such an automated script might be doing.

The UVM library proved a switch to the user to ensure that users have not accidently overlooked an area which is deprecated or targeted for deprecation. +define+UVM\_NO\_DEPRECATED is a compilation option that enables error messages if deprecated features are used.

## II. PRIOR TO OVM-2.1.2

The OVM-2.1.2 release notes list deprecated features in OVM. These need to be resolved before converting to UVM. Any items marked as deprecated prior to OVM-2.1.2 will not be available in UVM. As OVM went through rapid churning, not all projects were able to keep up to date and not all changes were easily identifiable as deprecated features or required code modification. Whilst many of the OVM deprecated features were indicated at runtime by a specific OVM DEPRECATED warning message there were some that were not so easily identifiable by the end users. To ensure OVM migration to UVM was as smooth as possible AMD methodology team created OVM 2.1.2 TRANS version which was OVM-2.1.2 but with all deprecated features removed. This enabled project teams to identify areas where their code was using features not available in UVM.

#### A. Typical deprecation issues not enforced in OVM

For completeness this section outlines some of the more prevalent issues a user would need to resolve prior to upgrading from OVM to UVM. The issues include modification to the phasing API, the removal of semicolons to macros and the replacement of ovm\_threaded\_component objects along with vendor specific classes.

#### 1) Threaded Classes

In older versions of OVM library there was an ovm\_threaded\_component object that could be used by people to derive their own custom VIP components. The ovm\_threaded\_component was originally the class that held run() mechanism. By the time of UVM and OVM-2.1.2 the ovm\_threaded\_component had been completely deprecated and functionality merged into ovm\_component.

## 2) Reporting

An area that inevitably touches every part of a verification environment is the standard output text API. It has been well discussed about the limitations of using \$display() within your code as it can add overhead for regression and lacks the controllability for different users. So, it was guite natural for users to want to adopt a better reporting system as provided by OVM. Most users got caught between different version of OVM having slightly different API to use as an alternative to \$display(). i.e. message(), `OVM REPORT INFO, ovm report info `ovm info. Also note, or `message() was not part of OVM and will be discussed in vendor specific section.

### a. Messages with Severities

By the time of OVM-2.1.2 users were expected to be using `ovm\_info(), `ovm\_warning(), `ovm\_error() and `ovm\_fatal() macros for reporting information. The capitalized variants were deprecated prior to OVM-2.1.2;

`OVM\_REPORT\_[info\_WARNING|ERROR|FATAL]

#### This in UVM now becomes:

`uvm [info warning|error|fatal]

### b. Message Macros with semi-colon

The semi-colon is a line terminator in Verilog and can cause functional differences in the code if not used correctly. For instance a semi-colon placed at the end of an already terminated line after an if-else clause will cause the "if" to be terminated unless it is followed by a "begin" block. Therefore, it is important to understand whether or not a semi-colon is included as part of the macro expanded code. Here is the code in question:

- if (enter)
  - if (somevar)

```
`ovm error(...);
```

```
else ...
```

The issue in the above code is that the "if (somevar)" clause may be terminated by the semi-colon after the ovm\_macro call.

Let us rewrite the above as some classic Verilog code.

```
if (enter)
    if (somevar)
        $display("ERROR Message output");
//`ovm_error(...)
        ; //bad semi-colon after `ovm_error
    else ... //Else is associated with "enter"
and not with "somevar"
```

#### Therefore,

```
`ovm_[info|warning|error|fatal](...);
becomes:
```

```
`ovm_[info|warning|error|fatal](...) `ifndef
BAD_semi ; `endif
```

### 3) Sequence and Sequence\_item Constructor

The sequence and sequence\_item constructor in OVM had 3 parameters passed in 2 of which were deprecated i.e.:

```
ovm_sequence::new(arg1, arg2, arg3);
ovm sequence item::new(arg1, arg2, arg3);
```

#### Sample code is:

```
ovm_sequence::new(name, sequencer=null,
parent sequence=null);
```

In UVM the constructor now only has the one supported parameter so the code becomes:

```
uvm_sequence::new(name);
```

## 4) Phasing

#### a. Terminating the Simulation

In OVM each component had a global\_stop\_request() method which has been removed from UVM. In UVM a global level (not component level) global\_stop\_request() method is present but marked as deprecated. The preferred mechanism in UVM is for components to participate in phasing and object to the current phase being executed from ending until the component no longer requires that phase to be executing. More on this topic in the methodology improvements section later in this paper.

i.e. OVM syntax:

```
mycomp::global_stop_request() or mycomp_inst.
global_stop_request();
Making the UVM syntax:
```

global\_stop\_request(); // to be deprecated Component level global\_stop\_request() was deprecated prior to ovm-2.1.2 and removed in UVM from component into root space. In turn global\_stop\_request() in the root space is marked for deprecation.

## b. Deprecated Phases

As OVM matured and learned what users needs were, several phases got deprecated along the way. Most notable post\_new(), configure() and pre\_run() phases should not be used in OVM-2.1.2 and are completely removed in UVM-1.X. The expectation is that the functionality executed in these deprecated phases can be moved into a supported phase in UVM. For instance, post\_new() functionality can often be moved into UVM's build\_phase(). Similarly, configure() functionality can be collapsed backward into connect\_phase() or it can pushed forward into end\_of\_elaboration\_phase(). Lastly, procedural code executed in pre\_run() can be mapped into start\_of\_simulation\_phase().

#### B. Vendor Specific code in OVM

There were numerous parts of users usage of OVM library that relied on code from vendor specific solutions. These have been removed so that UVM is vendor neutral and doesn't contain legacy non-agreed code in the standard. You may have some leftover pieces from a vendor specific library or vendor specific debug facility.

In UVM the transaction recording has been abstracted away from the base-class library and EDA vendors have an API which allows them to provide tool-specific transaction recording without affecting the UVM library code. Historically, many OVM users migrated from the now defunct URM or AVM methodologies.

As noted previously you may have unknowingly been using reporting features like `message() and 'dut error() which were never actually part of OVM. `message() and `dut error() should be replaced with `ovm info() and `ovm error() respectively. It is important that your code be clean of all urm \* and avm \* code before attempting to upgrade to UVM. In a similar but much more subtle vain there was a macro that had the ovm prefix but clearly leveraged the urm code infrastructure, although it may not have been guite so clearly stated as deprecated in OVM it definitely had no place in UVM. The macro in question is

`ovm msg define(<verbosity arg>) which users performing the upgrade are expected to replace with ovm report enabled (<verbosity arg>) prior to moving to UVM. The main functionality is to test what level the verbosity has been set to and the result will return "1" if the configured verbosity is greater than the verbosity arg supplied. Another popular method that is should be kept upto date with OVM advancements to reduce issues in miaratina to UVM is set global verbosity() which in OVM-2.1.2 becomes set report verbosity level hier().

#### III. OVM TO UVM

One could imagine since UVM was derived from an OVM code base that by performing an "O" to "U" translation on all scripts and code should suffice to enable UVM compilation rather than OVM. This is not true as OVM had some files and members that were not prefixed with ovm. Many of these discrepancies have been addressed in UVM. However, this does mean that the user needs to upgrade their scripts and top-to-bottom code usage appropriately.

In the following section let us review what is required to have correct UVM functionality for each of the major building blocks within the UVM library. This covers the general base class usage, the infamous configuration and factory schemes, a review of the reporting structure, what is involved in switching to UVM phasing, leveraging the new UVM sequence infrastructure and lastly modification in the TLM domain.

#### A. Base Classes

 temporary workarounds, how access to the top level arrays have been modified, discrepancies in macros that have been fixed, and modification to the comparator operations that could catch you out.

#### 1) Class Inclusion Scheme

The first place to start with the OVM is how users were accessing it from their verification code. A large portion of users were using `include "ovm.svh". Well in UVM there is no uvm.svh and if you pull in uvm.sv then there will be duplicate entries of the uvm library compiled. The correct mechanism is to use import uvm\_pkg::\*; which also enables users to pre-compile the library into its own precompiled library for all teams to use. Of course package imports do not bring in macro definitions therefore `include "uvm\_macro.svh" is expected where macro usage occurs.

#### 2) Parameter Class Workaround

The file ovm\_template.svh was used to workaround simulator deficiencies. OVM usage of this file should have been restricted to simulators which did not fully support template types in separate scopes. The file enabled template objects to be available in multiple scopes where the definitions and specializations did not need to be shared between the scopes. For UVM this file does not exist and all references in the users code must be removed.

#### 3) Top\_levels Array

The Top\_levels array is very useful for viewing all the classes that are used in your UVM testbench. If a uvm class has been constructed and not passed a "parent" hierarchy handle then it will be a top\_level component. The access to the top\_levels array is now contained within the uvm\_root object as a static element. Whereas

in OVM one could access using <code>uvm\_toplevels</code>, now in UVM the access is <code>uvm root::top levels</code>.

### 4) Field macro usage

OVM, unintentionally, supported the declaration of an enumeration as int within the field automation macros.

ie:

```
typedef enum {FOO, BAR} foo_e;foo_e my_foo;
`ovm_object_utils_begin(my_object_type)
    `ovm_field_int(my_foo, OVM_ALL_ON)
`ovm_object_utils_end
```

UVM has specializations within `uvm\_field\_int which makes this code erroneous. The corrected code becomes:

```
typedef enum {FOO, BAR} foo_e;foo_e my_foo;
`uvm_object_utils_begin(my_object_type)
`uvm_field_enum(foo_e, my_foo, UVM_ALL_ON)
`uvm object utils end
```

## 5) Comparator

It is generally accepted that the actionable methods in UVM users need to override should be  $do_*()$ . In OVM there was a comp() method that users could override for performing the compare functionality. With UVM one should override  $do_compare()$  rather than comp() when using uvm\_class\_comparator.

i.e: ovm\_class\_comparator::comp();

is now: uvm\_class\_comparator::do\_compare();

#### B. Configuration and Factories

The OVM mechanism for applying configurations has been significantly revamped and improved in UVM. At the time of writing the OVM set/get\*() API had been requested to be deprecated. Hence in the later section of upgrading methodological usage we will discuss how to move from the old OVM API to the improved UVM API. In this section we will cover the minimal subset of changes required to make OVM configuration and factory API's operate with UVM code.

### 1) Set/get config\_object()

There was an ambiguity that required clarification between OVM documentation versus OVM code versus UVM documentation versus UVM code implementations of set/get\_config\_object() API. The following is an amended extract from Accellera's UVM bug tracking system Mantis with reference bug number 3731.

http://eda.org/svdb/view.php?id=3731

OVM-2.1.2, occur In clonina would on а get config object() only if the clone bit for and the corresponding set config object() were set to 1. This prevented inadvertent cloning when get config object() was called without specifying the clone argument, which defaults to 1. One could argue the default for clone should have been 0.

Set	Get	affect
0	0	no cloning at all
0	1	no cloning at all
1	0	cloning on set
1	1	cloning on set (useful for multi- gets)

1	0	cloning on set	
0	1	cloning on get	
0	0	no cloning at all	
Set	Get	affect	
truth table is unerent, and not backward compatible.			

In UVM-1.0, the clone bit for the set is not saved, so the

Thus discussion of Mantis 3731 ensued. Resulting in, auto-configuration method, <code>apply\_config\_settings()</code> being fixed in UVM-1.1b to honor the clone bit provided with the <code>set\_config\_object()</code> method per the Accellera standard specification. The <code>get\_config\_object()</code> has intentionally been left as implemented in UVM-1.0 (not following the Accellera standard specification) in order to preserve current library implementation semantics.

cloning on set,

cloning on get

#### 2) Printing Factory & Override

1

1

Code modifications that were performed in other areas of OVM were also applied to the factory section. Some areas are high likely to affect users such as the modification in how to print the factory and how to print all the overrides in the factory. Previously, an OVM user would have called ovm\_factory::print() and to output all the override, ovm\_factory::print\_all\_overrides(). Whereas now in UVM the code becomes uvm\_factory::get.print().

To perform override calls to enable the factory to replace objects the API has gone from ovm\_factory::set\_type\_override[\_by\_type|\_by\_name ]

Thus in UVM becomes:

my\_obj::type\_id::set\_type\_override[\_by\_type|\_ by\_name];

#### C. Reporting and Controlling Messages

#### 1) Command line message control

Converting OVM Command line options cause UVM warnings. The format of the example below is an incorrect translation from " $\circ$ "vm to " $\cup$ "vm. The verbosity options are reordered under UVM.

i.e:

```
+uvm_set_verbosity=start_of_simulation,uvm_te
st_top.t0.ioe_s.slave[0].*,UVM_HIGH
becomes:
```

+uvm\_set\_verbosity=uvm\_test\_top.t0.ioe\_s.sla
ve[0].\*,\_ALL\_,UVM\_HIGH,start\_of\_simulation

#### 2) 'uvm\_info inside of sequence static methods

In OVM, sequences did not have implementations of the report methods, and as such relied soley on the ovm\_pkg scope functions.

In UVM, sequences do implement these methods, allowing for `uvm\_info() (et al.) to be called from within the sequence without needing to point to the sequence's parent sequencer. These implementations are not static however, which means that any static methods defined inside of a sequence must not use`uvm info calls.

### 3) Reporting Classes

The ovm\_reporter has been superseded by uvm\_report\_object and the ovm\_report\_global\_server class is replaced with a proper implementation of a singleton in the uvm\_report\_server class. The following statements

```
ovm_report_server srvr;
ovm_report_global_server glbl= new();
srvr = glbl.get_server();
GLBL.SET_SERVER(MY_SRVR);
should be modified as follows:
```

```
uvm_report_server srvr;
srvr = uvm_report_server::get_server();
uvm_report_server::set_server(my_srvr);
```

## 4) Topology Printing

The printing of the topology is now scoped to the uvm\_root object constructed as uvm\_top. Therefore, ovm\_print\_topology() now becomes uvm\_top.print(). The same modification needs to be performed for ovm\_enable\_print\_topology() for it to become in UVM uvm\_top.enable\_print\_topology().

Based on component context this should be reviewed by user to ensure valid modification is performed during upgrade.

#### 5) Printer API's

Several printer knobs are deprecated and no longer have any effects.

In OVM the printer knobs were located in:

ovm\_default\_printer.knobs
these in UVM 1.0 became:

uvm\_printer\_knobs

subsequently in UVM 1.1 the printer knobs were reviewed and many where removed, such as:

uvm\_printer\_knobs::max\_width uvm\_printer\_knobs::truncation uvm\_printer\_knobs::name\_width uvm\_printer\_knobs::type\_width uvm\_printer\_knobs::value\_width
uvm\_printer\_knobs::sprint
uvm\_component::print\_config\_settings

#### One of the knob members was renamed from:

ovm\_printer\_knobs::global\_indent
to

uvm\_printer\_knobs::indent

The uvm\_component::print\_config\_settings() method is deprecated in favor of the method uvm\_component::print\_config().

#### The following statement:

```
comp.print_config_settings("", null, 1);
print_config_settings("", comp, 0);
Hence, should be modified as follows:
```

```
comp.print_config(1);
comp.print config(0);
```

The other notable point with printers is that in OVM the down() method had two arguments whereas in UVM there is only one argument. See the following example:

```
printer.m_scope.down(get_name(), null);
Is now in UVM as:
```

```
printer.m_scope.down(get_name());
```

#### D. Phasing

UVM provides a run time switch allowing the phasing to use the scheduling as ordained by the OVM run\_phase() , the switch is +uvm use ovm run semantic. Usage of

this switch should be temporary to ease the migration process, once fully conversant in UVM the phasing should be implemented correctly and remove usage of the switch. An obvious change that you will notice is that the phase names have been enhanced to explicitly state <method>\_phase and pass the phase\_name as an argument to the method. By doing so it give easy access to phase methods such as objection interactions. This correlates with how various timeouts have been modified.

1) Phase names, calls and super accesses.

Even though the same OVM phase methods are in the UVM library they are marked for deprecation and it is strong advised that all users implement using the new phase names and API.

This means OVM code

<phase\_name>();

#### Becomes:

<phase name> phase (uvm phase phase);

The signature of all pre-defined phase implementation methods are modified, build, connect, end\_of\_elaboration, start\_of\_simulation, run, stop, extract, check and report.

Due to the change in UVM if there was code in the environment that was directly calling a phase method such as <mycomp>.build()this will now cause an error condition to be signified. Direct calls to <anyusercomponent>.build() are illegal and should be removed from the code.

Similarly, the phase name modifications need to be applied to all super.<pname>() where there are intermediate classes used for derivation functionality

containment these now need to use super.<phase\_name>\_phase (phase).

#### 2) Timeouts and Termination Criteria

Timeouts were implemented in OVM and in UVM to prevent endless runaway simulations. They were never intended to be used as functional mechanisms to determine when a users verification of a design was complete. Moving from OVM to UVM the timeouts were streamlined, the OVM set global timeout and ovm top.stop timeout were removed from UVM in preference for the objection mechanism. Also, the `UVM DEFAULT TIMEOUT which in OVM was typically used as "`UVM DEFAULT TIMEOUT - \$time" still exists although the usage now is simply `UVM DEFAULT TIMEOUT and it will issue a UVM FATAL message when reached from UVM-1.1c onwards.

Users wishing to prolong or terminate their testbenches must use the objection mechanism to determine when the simulation should end. There has been a change in the syntax which for OVM use to be: ovm\_test\_done.[raise|drop]\_objection(args1)

Now with UVM-1.X the syntax, specifically when within a phase method context has become:

#### phase.[raise|drop]\_objection(args1);

The *hammer* approach of global\_stop\_request() has been deprecated as it was not reusable and caused many issues when integrating code that incorrectly and ungracefully terminated the simulation. Later, in the methodology section we will cover a full example of how to properly terminate the simulation.

#### E. Sequence Control and Data Objects

The sequence API in UVM has been improved by adding more debug features and aligned the methods with other

parts of UVM also removed unnecessary variables such as count. The OVM sequence library had several problems and in UVM-1.1 there is a new sequence library that solves many of the use and reuse factos faced previously.

#### 1) Sequence Raise Objection with debug

UVM add a description field to the raise and drop objections functions. This provides a convenient way to view and debug when there are multiple interleaved objections within the simulation. The OVM syntax was:

raise\_objection(object, count);

drop\_objection(object, count);

#### Whereas UVM uses:

raise\_objection(object, description, count);

drop\_objection(object, description, count);

#### 2) Sequence Objections

To correctly upgrade the syntactical usage of objections within sequences one must also address how they are used. In OVM the policy was to leverage the ovm\_test\_done object and use that as a container to raise and drop the objections controlling the end proloning or termination of the simulation. That is in OVM syntax one would have coded :

uvm\_test\_done.[raise|drop]\_objection(<args>)
Whereas in UVM the policy is to raise and drop objections
per phase which makes the syntax usage within a
sequence as follows:

#### if (starting\_phase !=null)

starting\_phase.[raise|drop]\_objection(<args>)
This direct translation between what is expected syntax
previously to what is UVM syntax does not address the

complete usage. Most users had implemented a style of objection usage that one can call pessimistic mode. In many verification environments the objection usage is per-sequence placed, at worst within the sequence or more common within pre/post body() for raising then dropping objections. It is probably overkill and engineering paranoia wanting to ensure each sequence can prolong or protect against simulation terminating during sequence execution. The code can be optimized by refactoring for an optimistic mode, whereby only the highest level sequences need to raise/drop objections from within pre/post start(). For the pedantic, prior to UVM-1.1 it would have been within pre/post body(). See section on body() callbacks in the methodology upgrade chapter to learn about how pre/post body() are now callbacks for every sequence and pre/post start() are only root sequence activated.

#### 3) Sequence Item Port Connections

The pseudo TLM-1 OVM sequence API has been cleaned to align more closely with other API's within UVM. Namely the \* if has been dropped meaning OVM API's:

```
seq_item_prod_if, seq_item_cons_if,
seq_item_port.connect_if
Translates to::
```

seq\_item\_port, seq\_item\_export,
seq\_item\_port.connect

# 4) Data objects for constrained random verification

Some parts of OVM were more trial and error than driven by definitive users criterion. One such area was the creation of ovm\_transaction class, it was considered useful at one point to have a lower level object that did not have the overhead of sequence item members yet could be used for transaction recording and derived from for monitoring purposes. At the time of UVM review it was noted that overhead of using sequence\_item object rather than transaction was minimal and created less divergent code as most users would anyway derive from sequence\_item to add in their object members required for constrained random and coverage driven verification. The ovm\_transaction class is deprecated and should be replaced with uvm\_sequence\_item. The following statement

class my\_trans extends ovm\_transaction; should be modified as follows:

class my\_trans extends uvm\_sequence\_item;

Some advanced users had been accessing non-public API's of the OVM library. The area that seemed most common was the usage of `OVM\_FIELD\_DATA within data objects. This macro is deprecated from UVM however with some reviews of the macro usage it is normally possible to use `M\_UVM\_FIELD\_DATA instead

## 5) Sequence, Sequencer Automation and Relationship

As part of the review and improvement process when creating UVM the sequence utility macros were enhanced for a more flexible and complete usage model. Fristly, the sequence and sequencer automation macros now align with their internal base-class types of uvm\_object and uvm\_component respectively. Secondly, the sequence data automation gives the sequence the freedom to not be tightly coupled with a single sequencer. In OVM for the sequence one would have written the syntax: `ovm\_sequence\_utils(arg1, arg2)
Now with UVM-1.X the syntax becomes:

`uvm\_object\_utils()
`uvm\_declare\_p\_sequencer(arg2)
Similarly, for the sequencer the OVM syntax was:

`ovm\_sequencer\_utils
This in UVM becomes:

`uvm\_component\_utils

# 6) Default Sequence, counting and the sequence library

OVM had a default sequence which was set to ovm random sequence as default. This allowed users to use the internal count variable to control how many sequence items were generated. UVM has enhanced the usage of default sequence to be per runtime phase aware and it no longer defaults to ovm random sequence. Therefore, there is no longer a requirement to have the count variable within the library. If users require a count variable it would belong in their sequences outside of the summary code librarv code. In such as set config int(<sqcnr>, "count", 0)is no longer valid and should be removed.

To configure the default\_sequence per phase there are a variety of techniques available within UVM. If a user in the OVM code had the following:

set\_config\_string("<hier\_to\_sqncr>",
default\_sequence, "<seq\_type>");
They could use the UVM configuration database:

```
uvm_config_db#(uvm_object_wrapper)::set(this,
"<hier to sqncr>.run phase",
```

``default\_sequence, <seq\_type>::type\_id::get()); Alternatively use the factory to find the type:

```
myseq_type my_seq=new("my_seq");
uvm_config_db#(uvm_sequence_base)::set(this,
"<hier_to_sqncr>.run_phase",
"default_sequence", "my_seq").
```

Occasionally, it is better reuse and readability to have seq.start() in each of your testcases to start different sequences per test:

```
myseq_type my_seq= new("my_seq");
my_seq.start(my_sqcnr, null);
```

This leads directly onto how to categorize sequences into a library for reuse. In OVM there were many caveats and tight coupling between objects preventing arbitrary reuse of sequences and sequence libraries across arbitrary sequencer. The OVM sequencer based sequence library is deprecated and replaced with a more reusable implementation. As shown above sequences can be spawned by simply calling start(). Also, see the methodology section on using UVM-1.x sequence library. The main code that affects users is the removal of the sequence library macros in OVM, which means the code must be removed to work with UVM

```
`ovm_update_sequence_lib() and
`ovm_update_sequence_lib_and_item(<arg>)
```

#### F. TLM API inclusion and usage

The TLM directories and files were an area where OVM did not use ovm\_ or OVM\_ nomenclature. This was addressed by UVM therefore OVM syntax tlm\_\* or TLM\_\* has been fixed in UVM to become uvm\_tlm\_\* or UVM\_TLM\_\*. User including, importing or using the TLM files and features of OVM would need to modify their code to use the corrected UVM prefix nomenclature with TLM.

The UVM library also addressed the OVM export\_connections\* and import\_connections\* by deprecating these and replacing them by having calls within connect().

#### IV. CONCLUSION

Knowledge of what, how and where modification are required de-risks the migration process from OVM to UVM. At AMD and within Synopsys there are technologies and resources that make the OVM to UVM transition painless and can even be done unbeknown to the user. For AMD the UVM upgrade is a long term strategy that needs to coincide with project specific needs and requirements. The process has been proven and well understood thereby enabling users to take advantage of the OVM bugs addressed by UVM and the new features UVM brings for advanced verification.

### V. ACKNOWLEDGEMENTS

The authors would like to acknowledge the contributions of John Fowler, who architected and implemented much of the AMD transition kit. Also, Janick Bergeron provided significant material for the definitive guide. Numerous AMD, Synopsys colleagues and various companies aided by qualifying the scripts developed preceding this paper. The scripts were coupled with the OVM to UVM upgrade guide and with the UVMKit, to all of those users involved we owe much appreciation as they drove the requirement for creating this paper. Also a huge thank you must go out to all Accellera members whom are continuing to strive for a better UVM that can fulfill many users verification needs.

## VI. REFERENCES

- 1. UVM-1.1.c User guide by Accellera
- 2. UVM-1.1.c Accellera source code
- 3. OVM-2.1.2 Release notes by OVM team
- 4. OVM-2.1.2 VCS source
- 5. AMD internal TWiki by John Fowler & Justin Refice
- 6. OVM to UVM Upgrade guide by Adiel Khan
- 7. http://eda.org/svdb UVM Mantis by Accellera