NVVM: A Netlist-based Verilog Verification Methodology for Mixed-Signal Design

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Agenda

• Why is verifying mixed-signal IP a great challenge?

• NVVM compares to traditional methods?

• Examples of NVVM

• Limitations
The Complexity of Mixed-Signal Design is Growing Rapidly.

- # of transistors increase
- More complex blocks
- Contain digital control logic
- FastSPICE + Blackbox is still commonly used.
Traditional Verification Method

Design Specification

Analog designer

Analog Schematic

Continuous simulation with Spice/Spectre

Consistency? Feedback?

Verification engineer

Digital Model

Digital-centric regression runs
NVVM Flow

Design Specification

Analog designer

Verification engineer

Scripts, Database, Assertions

Analog Schematic

netlist

Digital Model

Consistency Timely feedback

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NVVM strikes a balance among speed, accuracy and modeling efforts.
Example of NVVM

Spectre Netlist:

MP1 (VDDH OUTB OUT VDDH VSS) PCH_3P3V_ESF3  wFinger=0.6 l=0.4
MP2 (VDDH OUT OUTB VDDH VSS) PCH_3P3V_ESF3  wFinger=0.6 l=0.4
MN2 (GND net49 INB GND) NCH_1P2V  wFinger=1  l=0.07
MN1 (GND net53 IN GND) NCH_1P2V  wFinger=1  l=0.07
INV1 (IN VDDL VDDL GND INB) INV_F1
MNA (GND OUTB VBias net53) NCH_3P3V_ESF3  wFinger=1  l=0.4
MNB (GND OUT VBias net49) NCH_3P3V_ESF3  wFinger=1  l=0.4
Example of NVVM - 2

Verilog Netlist:

PCH_3P3V_ESF3  MP1  (.D(OUTB), .B(VDDH), .G(OUT), .S(VDDH));
PCH_3P3V_ESF3  MP2  (.D(OUT), .B(VDDH), .G(OUTB), .S(VDDH));
NCH_1P2V  MN2  (.D(net49), .B(GND), .G(INB), .S(GND));
NCH_1P2V  MN1  (.D(net53), .B(GND), .G(IN), .S(GND));
INV_F1  INV1  (.Y(INB), .A(IN));
NCH_3P3V_ESF3  MNA  (.S(net53), .G(VBias), .B(GND), .D(OUTB));
NCH_3P3V_ESF3  MNB  (.S(net49), .G(VBias), .B(GND), .D(OUT));
Example of NVVM - 3

Original Netlist:

PCH_3P3V_ESF3 MP1
PCH_3P3V_ESF3 MP2
NCH_1P2V MN2
NCH_1P2V MN1

Modified Netlist:

PCH_3P3V_ESF3_r MP1
PCH_3P3V_ESF3_r MP2
NCH_1P2V MN2
NCH_1P2V MN1

Database:

<table>
<thead>
<tr>
<th>Module</th>
<th>Instance</th>
<th>Cell</th>
<th>Mod</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>LS_test</td>
<td>MP1</td>
<td>PCH_3P3V_ESF3</td>
<td>r</td>
<td>weak PMOS load in LS</td>
</tr>
<tr>
<td>LS_test</td>
<td>MP2</td>
<td>PCH_3P3V_ESF3</td>
<td>r</td>
<td>weak PMOS load in LS</td>
</tr>
</tbody>
</table>

Primitive Library:

module PCH_3P3V_ESF3_r ( B, D, S, G );
    inout B, D, S;
    input G;
    rpmos(D,S,G);
endmodule
Limitations

Is

- Node-accurate structural model
- As fast as a black box
- Supports assertions and coverage analysis
- A powerful tool for designers

Is not

- The input and output signal can only be 0/1/x/z
- Not suitable for small complex analog blocks

XX out of 295 tests failed.
Questions