Sequential Equivalence Check beyond Clock Gating Verification

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Different Types of Equivalence Checking

Boolean Equivalence (Formality)

- Design A
  - Matched Compare Points
  - Compare Boolean Fan-in Logic

- Design B
  - Matched Compare Points

Sequential Equivalence (SEQ)

- RTL Model A
  - Assume Equal Inputs & Start State
  - Compare Outputs, Every Cycle, Unbounded ...

- RTL Model B
  - Assume Equal Inputs & Start State
  - Compare Outputs, Every Cycle, Unbounded ...

Transaction Equivalence (DPV)

- Untimed Transaction Model A
  - Assume Equal Inputs
  - Compare Outputs at End of Transaction(s)

- Cycle Accurate Model B
  - Assume Equal Inputs
  - Compare Outputs at End of Transaction(s)
Two designs that produce same output on every clock cycle from valid initial states given the same inputs are sequentially equivalent.
Clock-Gating Verification

Clock gated design

Task: Ensure no output mismatch for all possible legal input combinations

Instance spec of DUT
slog clocks always running

Instance impl of DUT
slog clocks can be disabled based on internal state

SEQ for Outputs
SEQ Applications beyond Clock Gating

1. Verify RTL de-feature

```verilog
input feature_foo_input_vld;
...
`ifdef enable_feature_foo
assign foo = ....;
...
`else
assign foo = 0;
...
`endif
```

SPEC:
+define+enable_feature_foo
fvassume feature_foo_input_vld==0

2. Verify RTL add-feature

```verilog
...
`ifdef new_feature_foo
assign foo = ....;
`endif
...
```

SPEC:
Without define+new_feature_foo

IMPL
SEQ Applications beyond Clock Gating

3. Verify parameterized design changes

4. Verify design changes due to power

5. Verify designs with timing changes

- Swap building cells, memory cells, clock gating cells
- Shorten pipeline stages
- Move logic across flop boundaries for timing
Convergence Techniques

- Redefine equivalence for accuracy

- Partial word mapping
Orchestration view

- Convergence Debug Aid – Orchestration View
  - Highlights progress for ongoing refinement steps
  - Failures in the child proofs do not automatically mean failure in any of its parent-proof’s
Report and Control Register Mappings

- “report_seq_mappings” provide information on
  - All the mapping points
  - All the points not mapped
- Internal mappings have significant impact on the convergence
Results

4 inconclusive after 3 days

Partial word mapping
seqmap internal mapping

Full proof within 2 hours