Next-generation Power Aware CDC Verification – What have we learned?

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Abstract

Reducing power consumption is essential to mobile and handheld application chips where reduced power contributes to longer battery life while minimally impacting performance. Reduced power consumption is achieved by partitioning an ASIC into multiple power domains, then controlling the power of these domains by switching off power or reducing voltage levels. Reduction of power consumption is further complicated by the interdependence of logic between power domains. This logic interdependence requires designers to add isolation, retention, and voltage shifter components at the power domain interfaces.

The addition of power control logic introduces new challenges to both design and verification efforts. The Unified Power Format (UPF) [1] is the IEEE standard format for specifying power domains and power control logic that is added to the RTL design. UPF support is required for all tools in the design and verification process, including simulation, synthesis and physical design. Traditional low power verification only validates the functional correctness of power control logic but does not validate the impact of power logic on multi-clock logic. Designers must additionally validate that power control logic does not introduce new multi-clock issues into their designs.

Today, designers understand the clock domain crossing (CDC) design and verification [2], but leading-edge design teams must incorporate low power techniques to detect CDC issues in low power designs. First generation low power CDC analysis techniques [3] have been successful in identifying problems resulting from incorrect power control logic insertion, but the evolution of low power design techniques has resulted in new challenges for low power design and requires new design practices and new verification techniques. In this paper, we will discuss the effects of advanced low power design on CDC design and verification. Specifically, we will describe the new CDC issues caused by the addition of power control logic including isolation cells, retention cells, level shifters, and dynamic voltage scaling:

- **Metastability introduced by isolation and retention cells**
- **New asynchronous clock relationships created by voltage domains and power switches**

We will describe the resolution of these CDC issues by employing netlist analysis, assertions, and formal verification:

- **Low power-based clock and reset analysis**
- **Identification of low-power CDC paths and synchronization structures**
- **Formal analysis for protocol assertions on low-power CDC paths**
- **Metastability delay modeling on low-power CDC paths in simulation**

Finally, we will illustrate these issues and solutions with real life UPF and designs.

Keywords – Design Verification, Verification, Clock Domain Crossing, CDC, Voltage Domain Crossing, VDC, Low Power, UPF, Isolation, Retention, Level Shifter, Voltage Domain, Successive Refinement, DVFS, Dynamic Voltage Frequency Scaling, Formal Analysis

I. INTRODUCTION

Advances in low power design and verification have been driven by both the technology as well as the tools. Often, the evolution of the tools is inspired by the needs of the designers based on their challenges during design implementation or the design issues found in the silicon.

Clock verification is a great example of this evolution. Initially, CDC verification was run on the gate-level representation of the low power design. As the designs have grown, designers achieve greater efficiencies through abstraction. Here, the abstraction involves running CDC analysis at the RTL instead of the gate-level. CDC verification at the RTL increases productivity by allowing designers to run the CDC analysis and fix CDC problems earlier in the design cycle to achieve time and resource savings. When designers run CDC verification at the gate-level, the CDC violations identified would require expensive, late-stage design modifications.

In this paper, we begin by discussing the current methods for verifying CDC paths for low power designs. The following section describes the latest problems found on low power designs and the methods for verifying these problems. Finally, we discuss how the latest generation of UPF (UPF 2.0 and UPF 2.1) has evolved to improve the CDC design and verification methods for low power design.

II. First Generation Low Power CDC Design Challenges

The Unified Power Format (UPF) is the universal standard for specifying the power control logic and its design connections. When the power logic is not instantiated in the design, the power intent is absent in the RTL and extracted from the UPF file during synthesis. This late implementation of the power intent information into the gate-level design may delay the start of power verification until after the gate-level representation is available and the power verification may create a critical path late in the design flow.

Most design teams are aware of possible design problems that can be introduced by the power control logic implementation. Clock and CDC errors can occur when the power elements are incorrectly inserted in the clock tree, the reset tree or the CDC paths. These errors may result in incorrect functionality such as data loss or data corruption. In other cases, these errors may result in intermittent errors that may not be reproduced in simulation and are extremely difficult to debug in silicon. These intermittent errors may appear or disappear when the operating conditions such as temperature, voltage, or frequency change.

III. First Generation Low Power CDC Verification

Design teams have implemented "power aware" methods and tools to address these low power design problems. Power aware CDC verification is such a method for identifying CDC errors introduced by the power control implementation.

CDC verification involves understanding the clocks, clock trees, and CDC paths in a design. Power aware CDC verification involves understanding how the power domains and power control logic affect the clocks, clock trees, and CDC paths. First generation power aware CDC analysis compiles the UPF and adds the power elements to the RTL design. Initially, only paths involving isolation cells were analyzed for CDC errors. The isolation cells are modeled as combinational logic and may create combinational logic or missing synchronizer violations. An isolation cell will introduce a new path from the enable signal to the destination register and in doing so, may introduce a missing synchronizer violation between the isolation enable signal and the destination register (see Fig. 1). If the isolation enable signal is in a clock domain that is asynchronous to the destination register's clock domain, the assertion and deassertion of the isolation cell enable may cause an asynchronous edge at the output register. When a missing synchronizer is detected, designers will correct the power control logic by synchronizing the isolation enable signal to the destination register's clock domain.

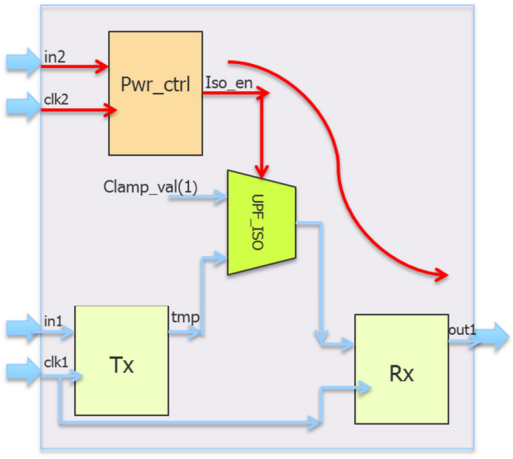

Figure 1: Isolation cell introduces a CDC path between synchronous registers

On properly synchronized CDC paths, isolation cells may introduce glitches and increase the occurrence of metastability that would reduce the reliability and mean-time-between-failures (MTBF) of these CDC paths (see Fig. 2). Power aware CDC tools operate on the RTL design and UPF and would detect combinational logic violations and new CDC paths created between the isolation cell enable and the destination register. With power aware verification tools, designers detect and fix these power-related CDC errors early in the design flow.

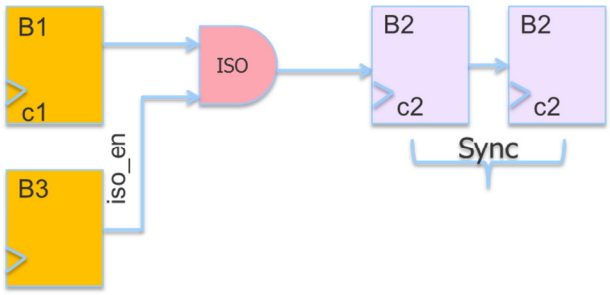

Figure 2: Power element on synchronized CDC path

IV. ADVANCED LOW POWER CDC DESIGN CHALLENGES

Design teams are becoming aware of new ways that low power design can adversely affect design logic. One such case that has affected CDC design is the presence of multiple voltage domains.

Advanced low power design has taken advantage of dynamic voltage frequency scaling (DVFS) to further improve power savings. By reducing the voltage and/or frequency, designs can reduce power consumption and heat dissipation when functionality or performance is not needed.

Initially, designers were not aware of the effects of DVFS on clocks and clock trees. Design teams have found new metastability issues in designs that implement DVFS techniques. After long and painful debug sessions in the lab, designers have found metastability issues between registers in the same synchronous clock group. Further exploration has found that registers between synchronous clocks on different voltage groups behave the same way as registers on asynchronous clock domains. The conclusion is that synchronous clocks on different voltage domains do not have a deterministic phase relationship and should be treated as asynchronous clocks. As the voltage level for a specific voltage group changes, the clock in that voltage group does not maintain a synchronous relationship to synchronous clocks in other voltage groups. Every control and data signal that runs between voltage domains must now be considered CDC paths including signals between synchronous registers (See Fig. 3).

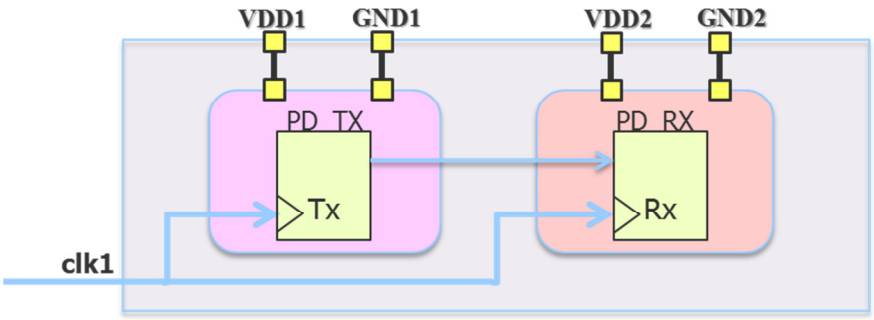

Figure 3: Synchronous registers on different voltage domains considered CDC path

Previously, design teams only inserted level shifters on paths between voltage domains. The realization that the synchronous clocks behave asynchronously between voltage domains means that CDC synchronizers must be added on the receiver side of the data transfer between voltage domains. Additionally, design teams were not previously concerned about CDC crossings to and from retention cells, because they believed that the save and restore protocol protected the retention logic from adverse effects due to metastability. Now, design teams are also concerned about

CDC crossing involving both isolation and retention cells. Designers are using synchronizers with retention registers to synchronize paths that traverse voltage domains (Fig. 4).

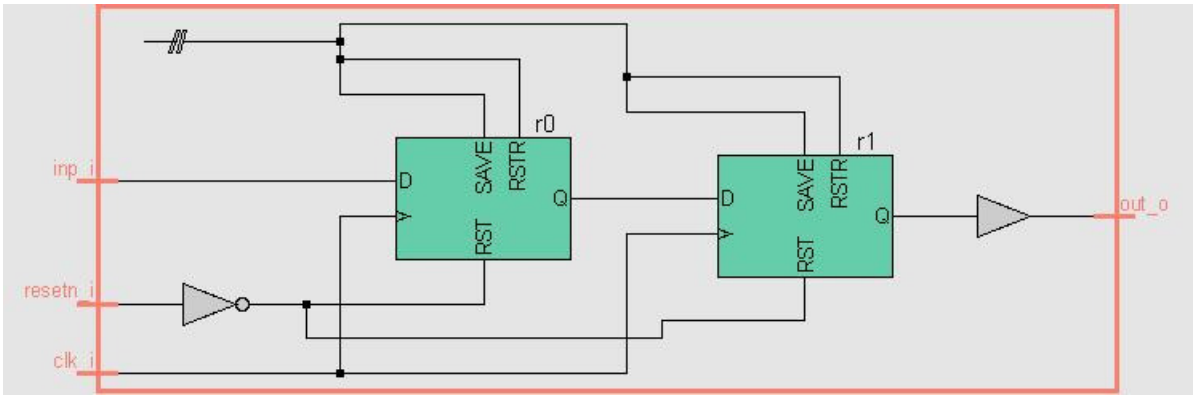

Figure 4: Retention-enabled synchronizer

V. APPLYING ADVANCED CDC VERIFICATION TO LOW POWER DESIGNS

Advanced low power designs are taking advantage of common CDC verification techniques to ensure that data transfer between power and voltage domains are not corrupted by metastability. These CDC verification techniques include both static and dynamic verification of CDC paths. The static techniques include the identification of low power CDC paths and synchronization structures as well as support for both isolation and retention cells. The dynamic techniques leverage both simulation and formal model checking technologies on CDC protocol assertions and metastability delay models.

Advanced CDC solutions such as Questa CDC have the capability to more accurately model the asynchronous low power clock domains. Questa CDC has implemented a capability to partition synchronous clock groups on different voltage domains into asynchronous clock groups. The addition of voltage domains to low power designs requires that designers add synchronizers on paths between voltage domains and the CDC analysis will flag CDC violations on any voltage domain crossing (VDC) paths that do not contain synchronizers.

This CPU core design demonstrates the effect of voltage domains on a single clock design (Table 1). Without the consideration of voltage domains, there are no CDC paths in this single clock design. When voltage domains are taken into consideration, this core is considered to have 6 asynchronous clocks and 4893 VDC paths. For Block 1 and Block 2 designs, these blocks have not been fully instrumented with power management logic, so the designers are reviewing the VDC paths to determine the appropriate power management strategies.

	Clocks	Power Domains	Voltage Domains	Asynchonrous Clocks	Isolation Cells	Retention Registers	VDC Paths
CPU Core	1	6	6	6	438	134690	4893
Block 1	10	4	4	26	439	0	8404
Block 2	10	5	2	7	142	0	10610

Table 1: CPU core design with power control logic

Once the design clocks have been accurately grouped, static structural analysis is used to identify both correct and incorrect CDC and VDC synchronization structures. For low power designs, both isolation and retention cells must be reviewed to ensure that incorrect CDC paths are corrected. Isolation and retention cells should not disrupt correct CDC structures and should not introduce new CDC paths. As mentioned earlier, VDC violations must be flagged on voltage domain crossing signals that do not contain synchronization structures and designers should add CDC synchronizers to these paths. Also, designers are also extending the power aware CDC verification to retention cells.

With the power aware CDC analysis, designers are able to verify CDC paths between voltage domains. In typical CDC analysis, paths between synchronous clock logic are not analyzed, but power aware CDC analysis detects VDC errors between these synchronous paths (See Fig. 5). In the illustrated case, the left and right power

domains are on different voltages, so a synchronizer is required for this path. This path also demonstrates a case where combinational logic in the fan-in of a synchronizer would reduce the reliability of the synchronizer. This VDC violation would not have been detected with typical CDC analysis, since this design has only 1 clock domain. Similar to CDC combinational logic violations, designers must ensure that design logic must first be registered before driving a VDC synchronizer.

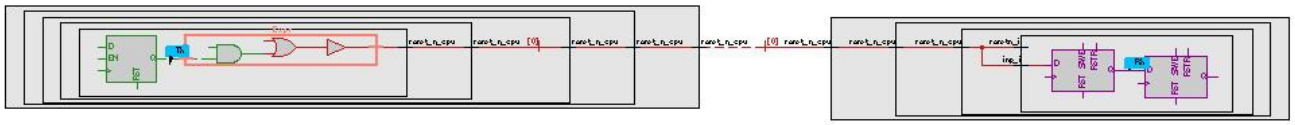

Figure 5. Combinational logic violation on synchronous voltage domain crossing

In addition to incorrect structures, it is important to identify correct synchronization structures, so CDC protocol assertions and metastability delay models can be generated for use with the dynamic CDC verification techniques. Dynamic CDC verification involves verifying both CDC protocols and reconvergence logic. Each CDC synchronization structure type requires that the design logic adhere to a structure-specific set of protocols. A simple example of a CDC protocol is the stability requirement for 2DFF synchronizers to avoid data loss or data corruption. For more complex synchronizers, adherence to the CDC protocol is needed to avoid metastability on the CDC transfer path. Additionally, we can expect certain CDC and VDC synchronization structures to have probabilistic delays due to metastability that is not modeled in traditional RTL simulation. The fan-in of reconvergence logic must be verified to ensure that there are no timing dependencies between synchronized CDC or VDC paths. Any timing dependencies between synchronized paths would result in functional errors in silicon.

During the static structural CDC analysis, both CDC protocol assertions and metastability delay models can be generated for each type of synchronization structure. The CDC protocol assertions can be used to check the synchronizer-specific rules in simulation or static timing analysis.

Metastability delay models can also be generated for each CDC path including VDC paths. The metastability delays occur in silicon, but this silicon-accurate metastability behavior does not occur in RTL simulation. Automatically generated, metastability delay models can be added to the RTL simulation. These models monitor the CDC path for conditions that would cause metastability in silicon and when metastability conditions are witnessed, the delay model randomly adds a cycle of delay at the RX register for setup violations or subtracts a cycle of delay at the RX register for hold violations. Using metastability models will ensure that each design is able to tolerate the metastability delays found in the design silicon.

VI. UPF 2.1 - SUCCESSIVE REFINEMENT

The latest UPF standards, UPF 2.0 and UPF 2.1, introduce successive refinement which is a new concept for low power design and verification. Successive refinement supports the System-on-Chip (SoC) design and verification flow by allowing the UPF file to be refined and updated as it travels from IP design to SoC design to SoC place and route. The UPF will also be refined as it is updated to support both front-end tools such as verification tools as well as back-end tools such as physical implementation tools.

The power distribution network is a physical implementation feature that is added to the design late in the project cycle. In UPF 1.0, the power distribution network is defined by the power supply ports, nets, and switches and the power domains are connected directly to the power supply nets (See Fig. 6). In this case, the design and verification teams must wait to verify the effects of the voltage domains on their design until after the implementation team has specified the power distribution network architecture.

```
# Specify Supply Ports
create_supply_port  VDD1 -domain PD1
create_supply_port  VDD2 -domain PD2
create_supply_port  VSS -domain PD1

# Specify Supply Nets
create_supply_net  VDD1 -domain PD1
create_supply_net  VDD2 -domain PD2
create_supply_net  VSS -domain PD1
create_supply_net  VSS -domain PD2

# Connect Supply Nets to Ports
connect_supply_net VDD1 -ports VDD1
connect_supply_net VDD2 -ports VDD2
connect_supply_net VSS -ports VSS

# Declare primary power and ground nets for the power domains
set_domain_supply_net PD1 -primary_power_net VDD1 -primary_ground_net VSS
set_domain_supply_net PD2 -primary_power_net VDD2 -primary_ground_net VSS
```

Figure 6: UPF 1.0 for Power Distribution Network

In UPF 2.0 and UPF 2.1, a new power network grouping option, the power supply set, has been introduced. The new power grouping option allows design teams to specify power groups without defining the voltage group's power and ground ports and nets [8]. The power supply set does not require the definition of the power ports, nets, and switches and their connection to the power domains. The power supply set allows designers to define and test the power distribution network earlier in the project cycle before the power distribution network has been implemented (See Fig. 7).

```
# Specify Supply Set
create_supply_set PRIMARY1 –function {power VDD1} –function {ground VSS}
create_supply_set  PRIMARY2 –function {power VDD2} –function {ground VSS}

# Declare primary power and ground nets for the power domains
associate_supply_set PRIMARY1 -handle PD1.primary
associate_supply_set PRIMARY2 -handle PD2.primary
```

Figure 7: UPF 2.1 for Power Distribution Network

The new power distribution network in UPF 2.1 is an example of the successive refinement methodology where the power network can be incrementally built over the duration of the project cycle by the different teams on design projects. The block and system designers can begin to verify the power management logic before the power distribution network has been implemented, then the final power management logic verification will occur later in the design flow when the physical designers add the power distribution network.

VII. SUMMARY

Power management continues to be a critical need for mobile systems. With the advances in low power design, the low power design and verification methodologies and techniques continue to evolve. The successive refinement features in IEEE 1801 allow designers to begin the design and verification of power distribution networks earlier in the design flow and continue to refine the power networks throughout the design cycle. Designers can start CDC verification for the power distribution networks at the RTL level and avoid detection of CDC errors late in the design flow at the gate-level.

In addition to the CDC verification for paths with isolation and retention cells, we have learned that voltage domain crossings are analogous to CDC paths and synchronizers are required on these paths. The Mentor Graphics Questa CDC solution verifies paths between power and voltage domains.

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