Next-generation Power Aware CDC Verification
What have we learned?
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### Power Control Logic
- Specified by Unified Power Format (UPF)
- Power intent not implemented in RTL
- Simulation verifies functional correctness
- Power logic may cause multi-clock issues

### Low Power Design Challenges
- Ensure isolation and retention cells do not introduce new CDC paths
- Ensure isolation cells do not introduce combinational logic violations
- Synchronize VDC paths between DVFS voltage domains

### Dynamic Frequency and Voltage Scaling (DVFS)
- Synchronous clocks in different voltage domains now asynchronous!
- In addition to level shifter, synchronizers are now needed at the receiver side of voltage domain boundaries

### Power Aware CDC Verification
- Low-power clock and reset analysis early in the design flow (before synthesis)
- Identification of low-power CDC paths and synchronization structures
- Formal analysis and simulation for protocol assertions on low-power CDC paths
- Metastability delay modeling on low-power CDC paths in simulation

### Advanced Low Power CDC Verification

#### 1. Static CDC verification
- Identify low power CDC paths and synchronization
- Low power CDC paths include isolation and retention cells

#### 2. Dynamic CDC verification
- Verify CDC protocol assertions with simulation and formal verification
- Verify reconvergence with metastability delay models in simulation

#### 3. Verify DVFS voltage domains
- Model asynchronous clock behavior induced by DVFS voltage domains
- Verify synchronization on voltage domain crossing (VDC) paths

### Unified Power Format (UPF)
- IEEE standard 1801
- UPF adds isolation cells, retention cells, level shifters
- Specifies power domains and power control logic
- Power intent extracted during synthesis
- Support required for all tools

### UPF 2.1 – Successive Refinement
- Successive refinement introduced with UPF 2.0 and UPF 2.1
- Supports System-on-Chip (SoC) design and verification flows
- UPF evolves as it travels from IP design to SoC integration
- UPF updated with additional detail as it travels from front-end design (design and verification) to back-end design (physical implementation)
- UPF power distribution network is available earlier and allows voltage domain-related CDC verification

### UPF Power Distribution Network
- UPF 1.0 voltage domains require power distribution network
- UPF 2.0 voltage domains require only power supply sets

#### CPU Core Design
- Single clock design
- No CDC paths
- Voltage domains induce 6 asynchronous clock domains
- 4893 VDC paths analyzed

#### Clocks
- Voltage Domains: Asynchronous Clocks
- Isolation Cells: Retention Registers
- VDC Paths

#### Results
- 4893 VDC paths analyzed
- 10 asynchronous clocks
- 438 isolation cells
- 438 retention cells
- 0 leakage power

#### Summary
- Advanced low power design introduces new CDC risks for SoCs
- Aggressive low power techniques such as DVFS, create new design and verification challenges
- Advanced CDC techniques enable the verification of low power designs
- Successive refinement in UPF 2.1 allows early verification of voltage domain crossing (VDC) paths

#### UPF Analysis Requirements
- Identify asynchronous voltage domain clocks
- Verify VDC synchronization
- Verify VDC protocol assertions
- Verify VDC reconvergence using metastability delay models

#### UPF Power Distribution Network
- Connect Supply Ports
- Connect Supply Nets
- Declare power and ground nets for power domains

#### UPF 1.0 voltage domains require power distribution network
- Specify Supply Ports
- Specify Supply Nets

#### UPF 2.0 voltage domains require only power supply sets
- Specify Supply Sets
- Declare power and ground nets for SoC design

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**Table:**

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<th>Block</th>
<th>Clocks</th>
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<th>Asynchronous Clocks</th>
<th>Isolation Cells</th>
<th>Retention Registers</th>
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**Diagram:**

- Instantiation of isolation cells may introduce new CDC paths and CDC errors
- Instantiation of isolation cells may cause combinational logic violations