Next-generation Power Aware CDC Verification
What have we learned?

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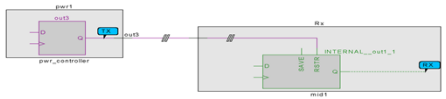
Power Control Logic

- Specified by Unified Power Format (UPF)
- Power intent not implemented in RTL
- Simulation verifies functional correctness
- Power logic may cause multi-clock issues

Low Power Design Challenges

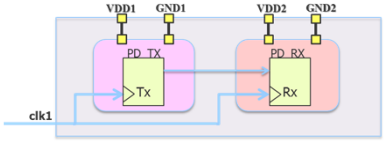
- Ensure isolation and retention cells do not introduce new CDC paths
- Ensure isolation cells do not introduce combinational logic violations
- Synchronize VDC paths between DVFS voltage domains



CDC paths may occur at the destination retention cell's save and restore pins

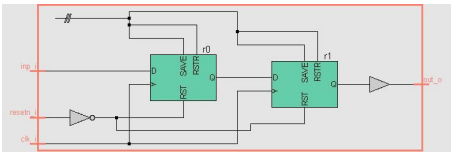
Dynamic Frequency and Voltage Scaling (DVFS)

- Synchronous clocks in different voltage domains now asynchronous!



Voltage domain crossing (VDC) between synchronous registers

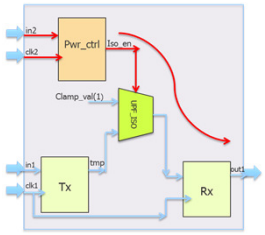
- In addition to level shifters, synchronizers are now needed at the receiver side of voltage domain boundaries



Retention-enabled synchronizer

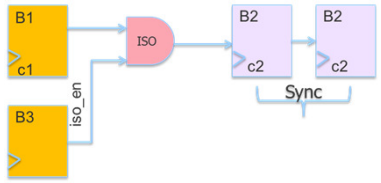
Power Control Logic CDC Issues

- Isolation and retention cells may introduce metastability



Instantiation of isolation cells may introduce new CDC paths and CDC errors

- Isolation cells may reduce the reliability of CDC synchronizers



Instantiation of isolation cells may cause combinational logic violations

Power Aware CDC Verification

- Low-power clock and reset analysis early in the design flow (before synthesis)
- Identification of low-power CDC paths and synchronization structures
- Formal analysis and simulation for protocol assertions on low-power CDC paths
- Metastability delay modeling on low-power CDC paths in simulation

Advanced Low Power CDC Verification

1. Static CDC verification
   - Identify low power CDC paths and synchronization
   - Low power CDC paths include isolation and retention cells
2. Dynamic CDC verification
   - Verify CDC protocol assertions with simulation and formal verification
   - Verify reconvergence with metastability delay models in simulation
3. Verify DVFS voltage domains
   - Model asynchronous clock behavior induced by DVFS voltage domains
   - Verify synchronization on voltage domain crossing (VDC) paths

Results

CPU Core Design

- Single clock design
- No CDC paths
- Voltage domains induce 6 asynchronous clock domains
- 4893 VDC paths analyzed

	Clocks	Voltage Domains	Asynchonrous Clocks	Isolation Cells	Retention Registers	VDC Paths
CPU Core	1	6	6	438	134690	4893
Block 1	10	4	26	439	0	8404
Block 2	10	2	7	142	0	10610

VDC Analysis Requirements

- Identify asynchronous voltage domain clocks
- Verify VDC synchronization
- Verify VDC protocol assertions
- Verify VDC reconvergence using metastability delay models

Summary

- Advanced low power design introduces new CDC risks for SoCs
- Aggressive low power techniques such as DVFS, create new design and verification challenges
- Advanced CDC techniques enable the verification of low power designs
- Successive refinement in UPF 2.1 allows early verification of voltage domain crossing (VDC) paths

Unified Power Format (UPF)

- IEEE standard 1801
- UPF adds isolation cells, retention cells, level shifters
- Specifies power domains and power control logic
- Power intent extracted during synthesis
- Support required for all tools

UPF 2.1 – Successive Refinement

- Successive refinement introduced with UPF 2.0 and UPF 2.1
- Supports System-on-Chip (SoC) design and verification flows
- UPF evolves as it travels from IP design to SoC integration
- UPF updated with additional detail as it travels from front-end design (design and verification) to back-end design (physical implementation)
- UPF power distribution network is available earlier and allows voltage domain-related CDC verification

UPF Power Distribution Network

UPF 1.0 voltage domains require power distribution network

```
# Specify Supply Ports
create_supply_port  VDD1 -domain PD1
create_supply_port  VDD2 -domain PD2
create_supply_port  VSS -domain PD1

# Specify Supply Nets
create_supply_net  VDD1 -domain PD1
create_supply_net  VDD2 -domain PD2
create_supply_net  VSS -domain PD1
create_supply_net  VSS -domain PD2

# Connect Supply Nets to Ports
connect_supply_net VDD1 -ports VDD1
connect_supply_net VDD2 -ports VDD2
connect_supply_net VSS -ports VSS

# Declare power and ground nets for power domains
set_domain_supply_net PD1 -primary_power_net VDD1 \
-primary_ground_net VSS
set_domain_supply_net PD2 -primary_power_net VDD2 \
-primary_ground_net VSS
```

UPF 2.0 voltage domains require only power supply sets

```
# Specify Supply Set
create_supply_set PRIMARY1
create_supply_set  PRIMARY2

# Declare primary power and ground nets for the power domains
associate_supply_set PRIMARY1 -handle PD1.primary
associate_supply_set PRIMARY2 -handle PD2.primary
```