Multimedia IP DMA verification platform

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Abstract

DMA verification is usually done by senior verification engineer because even a single bus protocol violation could hang up the whole SoC.

In this paper, we introduce a DMA verification platform for multimedia IP that could be easily used by verification beginners and could accumulate DMA verification knowledge how of experienced engineers without much effort.

Through this platform, even a novice verification engineer could develop a new DMA testbench in 30 minutes and we could verify several DMA instances at the same time with sufficient verification quality.

Introduction

For many years, DMA verification has been usually carried out by senior verification engineer because it could cause system hang if a bug escape related BUS exists. So one senior verification engineer had to verify up to 1 or 2 multimedia IP DMA simultaneously in SoC project.

But recently, Exynos mobile SoC has embedded various types of multimedia IP in order to provide differentiated multimedia function such as image fusion, TOF(time-of-flight) camera, HDR(High Dynamic Range) and etc. Since the most multimedia IPs have the form shown in figure 1, increasing the number of multimedia IPs leads to increasing the number of DMA to be verified.

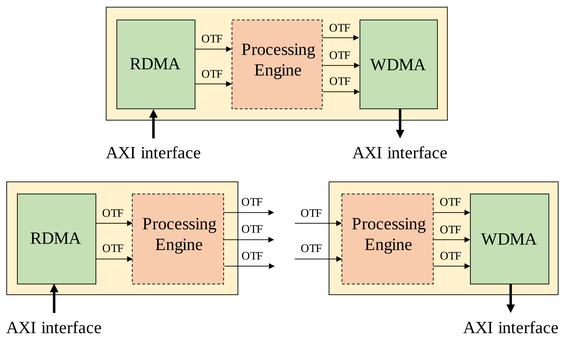


Figure 1: Typical architecture of multimedia IP with DMA

Because of these things, it was difficult to complete the DMA verification on time even if the verification engineer, who had previously verified DMA, worked very hard. So we have thought about 1) how to get the DMA testbench in a short time to reduce development time, 2) how to get enough verification quality even if novice verification engineer do the job.

As a result, we created super set DMA verification environment call as multimedia IP DMA verification platform (MDVP).

What is MDVP

MDVP is UVM based verification platform specialized for multimedia IP DMA. MDVP consists of:

A) Input data generator with compressed data format
B) DMA reference model for multimedia IP DMA
- Total number of supported data format : 48

C) Reusable testbench that can be shared among different DMA instances
D) Configurable UVM testbench according to the specification of the multimedia DMA for Exynos mobile SoC
- Total number of supported OTF interfaces : 16
- Total number of embedded UVCs : 54

Input Data Generation

Generally, the behavior of the multimedia IP DMA does not vary depending on the patterns of data to write or read. So random data is usually used for DMA verification. However, in case of DMA which has data compressor, random data pattern can cause limited behavior of DMA according to the compression algorithm. So in order to make various behavior of DMA which include data compressor, we have to use various natural image as well.

For creating various natural images to test, MDVP randomly selects one of about 10,000 natural image DB and then converts the selected image into an image with a desired format and resolution by ImageMagicK[1].

[1]: ImageMagick 6.7.2-7 [Computer software]. (2017). Retrieved from http://www.imagemagick.org.

DMA reference model

When developing model of multimedia IP, DMA model can be also developed to compare the behavior of hardware exactly. In this case, the DMA model can be used as the DMA reference model in the DMA verification. However, if input or output form of DMA model does not match, modification is required to use the model as DMA reference model.

So we developed newly DMA reference model for DMA verification that supports all kinds of memory format for multimedia IP in Exynos mobile SoC through analyzing every multimedia IP's DMA. This allows verification engineer using MDVP to reduce testbench development time by using a well verified DMA reference model.

The main outputs of DMA reference model in MDVP are valid address information and formatted data using given pixel data and DMA configurations such as base address, stride, pixel format and memory format.

Figure 2 and 3 show how the DMA reference model is used in WDMA and RDMA verification environment.

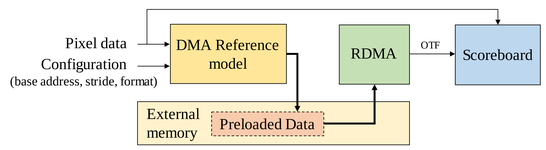


Figure 2: Example of using DMA reference model in RDMA

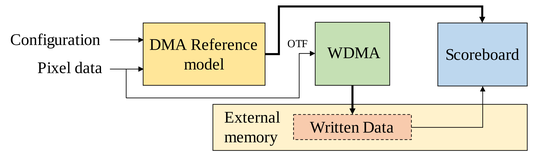


Figure 3: Example of using DMA reference model in WDMA

Reusable testbench

Most of the multimedia IP DMA have a similar structure and the majority of testbench can be reused by using DUT wrapper that instantiates DMA to be verified as shown Figure 4.

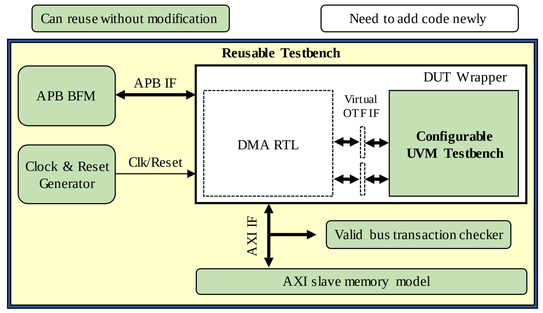


Figure 4: Reusable testbench of MDVP

Valid bus transaction checker

In case of WDMA verification, we defined the role of scoreboard as checking whether there is expected value in the expected address after finishing DMA operation.
In order to detect unintended bus request, we use valid bus transaction checker with valid address information of DMA reference model.

AXI slave memory model

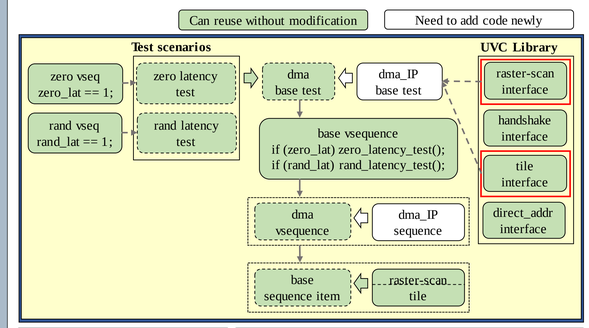
Reducing regression TAT(Turn Around Time) is also important to reduce verification time. So MDVP uses the in-house AXI slave memory model, that is used to verify multimedia IP for more than 10 years, instead of the commercial model provided by the EDA vendor. The in-house model is x2 faster than commercial model. In case of using commercial model, license shortage may cause long regression TAT, but it does not occur when using in-house model.

Configurable UVM testbench

We investigated the specification about all OTF interfaces to create super-set DMA verification environment. Before implementing each UVC corresponding OTF interface, we defined common sequence item for UVC to facilitate the maintenance if it is necessary to modify or create UVC.

As a result, the configurable UVM testbench of MDVP has 54 UVCs that correspond to 16 kinds of OTF interfaces. And it also provides common methods, that is used for all DMA verification such as input data generator / DMA reference model, UVC linking methods between DMA sequence and sequence item of UVC and UVM testbench skeleton.

Therefore even novice verification engineer who is not familiar with UVM can create new and stable DMA testbench based on MDVP quickly without much difficulty.



Test scenario	: Override base vsequence for each scenario
dma base test (dma_IP base test)	: Override default UVC for each OTF interface
base vsequence	: Execute test scenario
dma vsequence (dma_IP sequence)	: Override default sequence for each OTF interface
base sequence item	: Carry random configuration through sequencer to each OTF UVC

Figure 5: Configurable UVM testbench of MDVP

And we created common test scenarios used for each DMA verification while performing several projects with MDVP. So we embedded 13 predefined test scenarios to MDVP so that amount of developing code can be reduce for test scenario.

Conclusion

MDVP has been developed to get a multimedia IP DMA which has sufficient verification quality with small manpower within the project schedule. Since its first release, MDVP has been successfully used for multimedia IP DMA verification of 6 SoC projects so far.

Table 1: The effect of applying MDVP

	Without MDVP	With first MDVP	With latest MDVP
Line counts that need to be newly developed per each DMA to be verified	N/A	Average 1,298 lines	Average 556 lines
Required time to make an initial testbench	1~2 days	Average 1 day	Average 30 minutes
The number of DMA that verification engineer can handle simultaneously	Senior: 2~3 Junior : 1~2	Average 4	Average 5