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Multi-Domain Verification:

When Clock, Power and Reset Domains Collide

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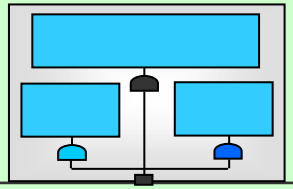
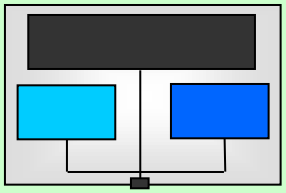
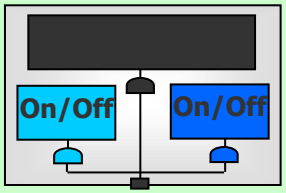
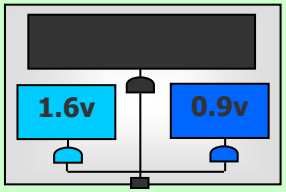
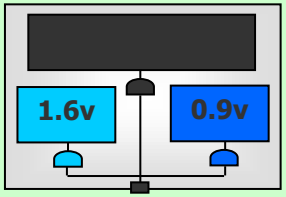
Agenda

- Low Power Design Techniques
- Domain Specific Verification
  - Clock domain crossing
  - Reset domain crossing
  - Power domain crossing
- Multi-Domain Verification
  - Interaction of Various Domains
- Results Multi-Domain Verification
- Summary

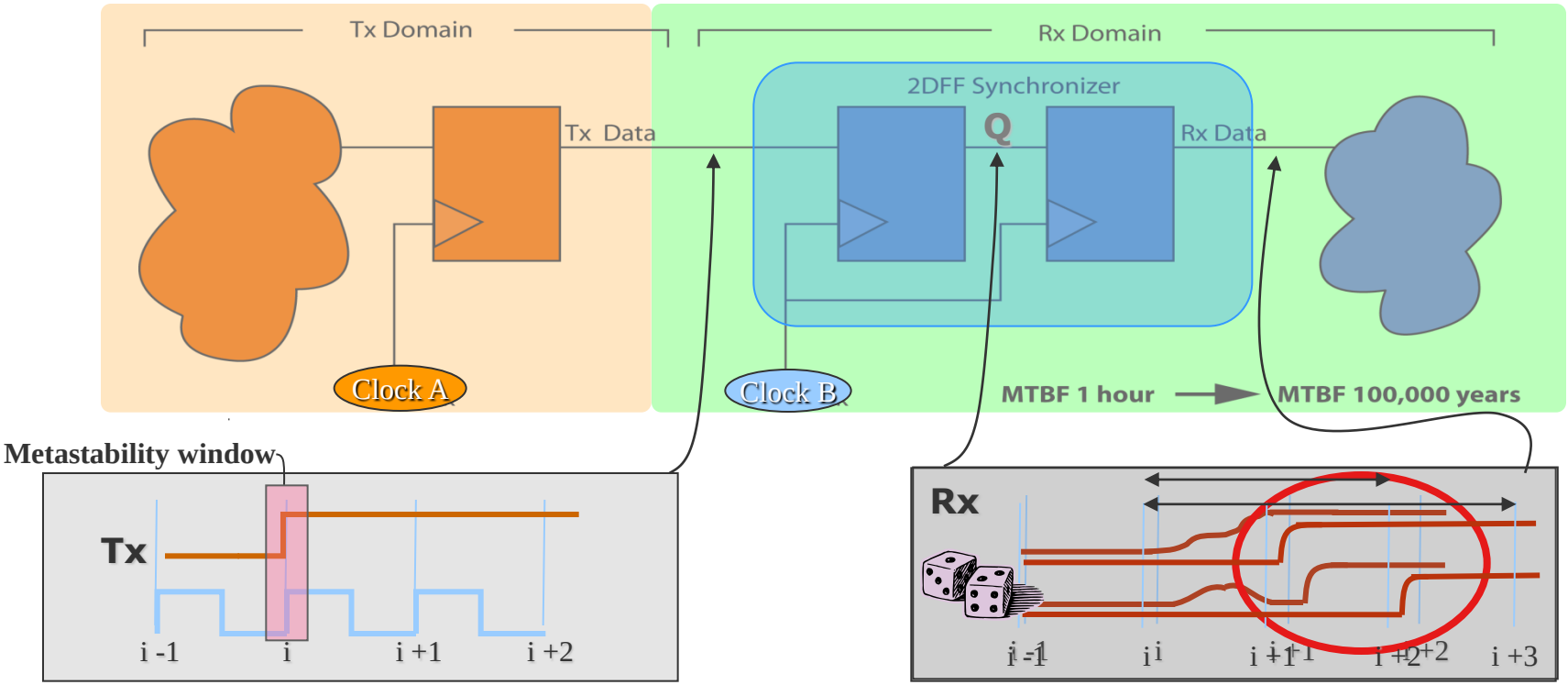
Low Power Design Techniques

Scheme		Impact
Clock Gating		Low effect, Moderate saving, UPF not required (affecting clock)
Multi-Threshold (V_{th}) Optimization		No change to RTL and Verification flow, Moderate saving
Power Gating (PG)		Power architecture, UPF specification, Big saving (affecting power, clock, reset)
Multiple Supply Voltage (MSV)		Power architecture, UPF specification, Big saving (affecting power, clock, reset)
Dynamic Voltage & Frequency Scaling (DVFS)		Power architecture, UPF specification, Big saving, Verification challenging

Domain Specific Verification

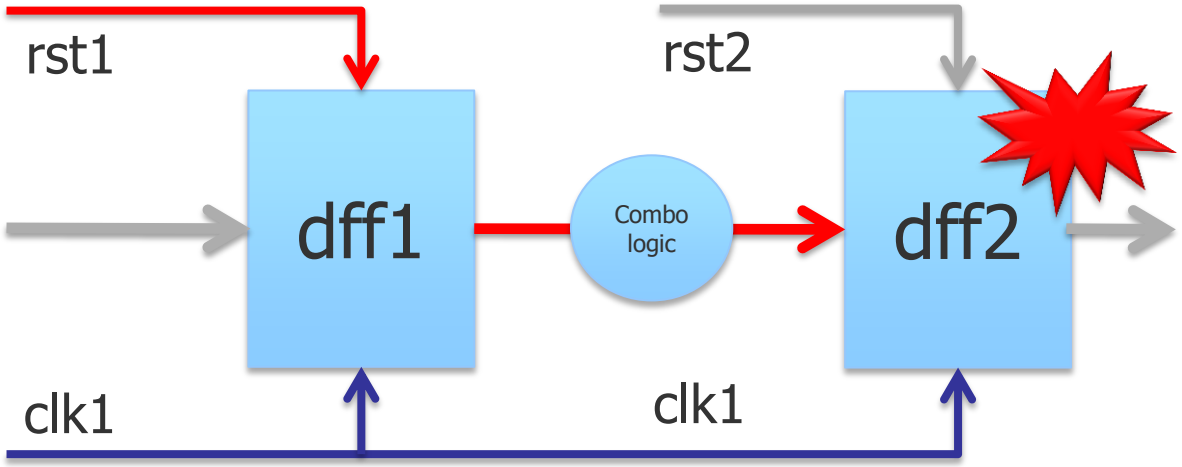
	Domain Structure	Domain Control	Domain Crossing
Power Domain	Power supply nets	Power switching, isolation and retention control	Power domain crossing (PDC) Isolation, Retention, Level shift
Reset Domain	Async and sync reset, tree structure, connectivity	Reset synchronization, polarity, control and gating conditions	Reset domain crossing (RDC)
Clock Domain	Async and sync clocks, tree structure, connectivity	Clock division, control and gating conditions	Clock domain crossing (CDC) Synchronizers, 2DFFs, FIFO and handshake structures

Clock Domain Crossing Issue



Setup Violation : Transition at input of synchronizer will propagate to output after **2 or 3** active edges of Rx clock in silicon

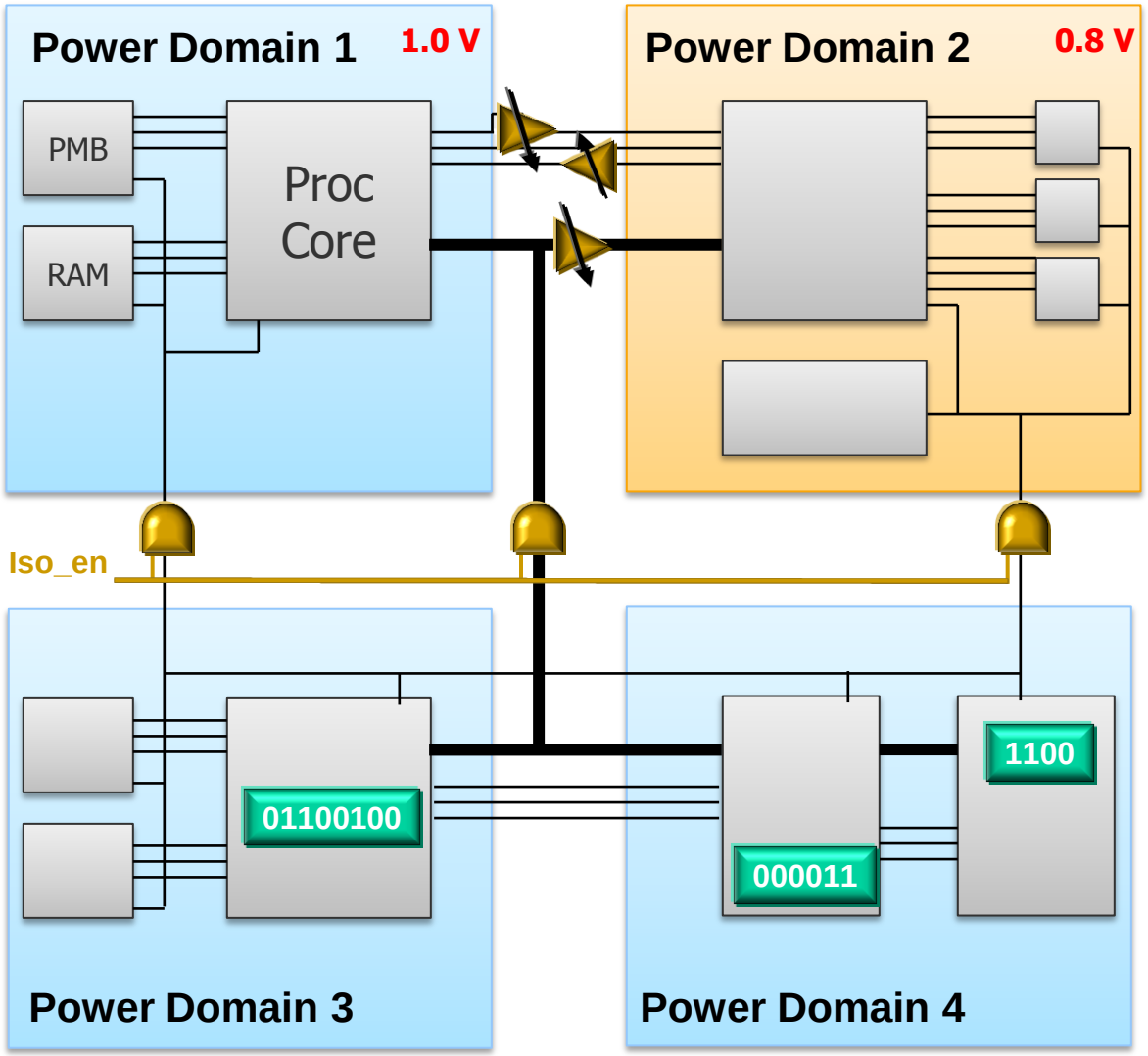
Reset Domain Crossing Issue



- Registers, dff1 and ddf2 are in same clock domain
  - Their reset, rst1 & rst2, are asynchronous
- If rst1 is asserted while rst2 is not asserted
  - the asynchronous output data from dff1 can cause metastability on dff2.

Power Domain Issues

- Power Domains
- Supply Networks
- Power Gating
- Corruption
- Isolation
- Retention
- Multi-Voltage
- Level Shifting
- Power States
- …



Multi-Domain Verification

Domain Structure Verification

- Power supplies
- Clock trees
- Reset trees

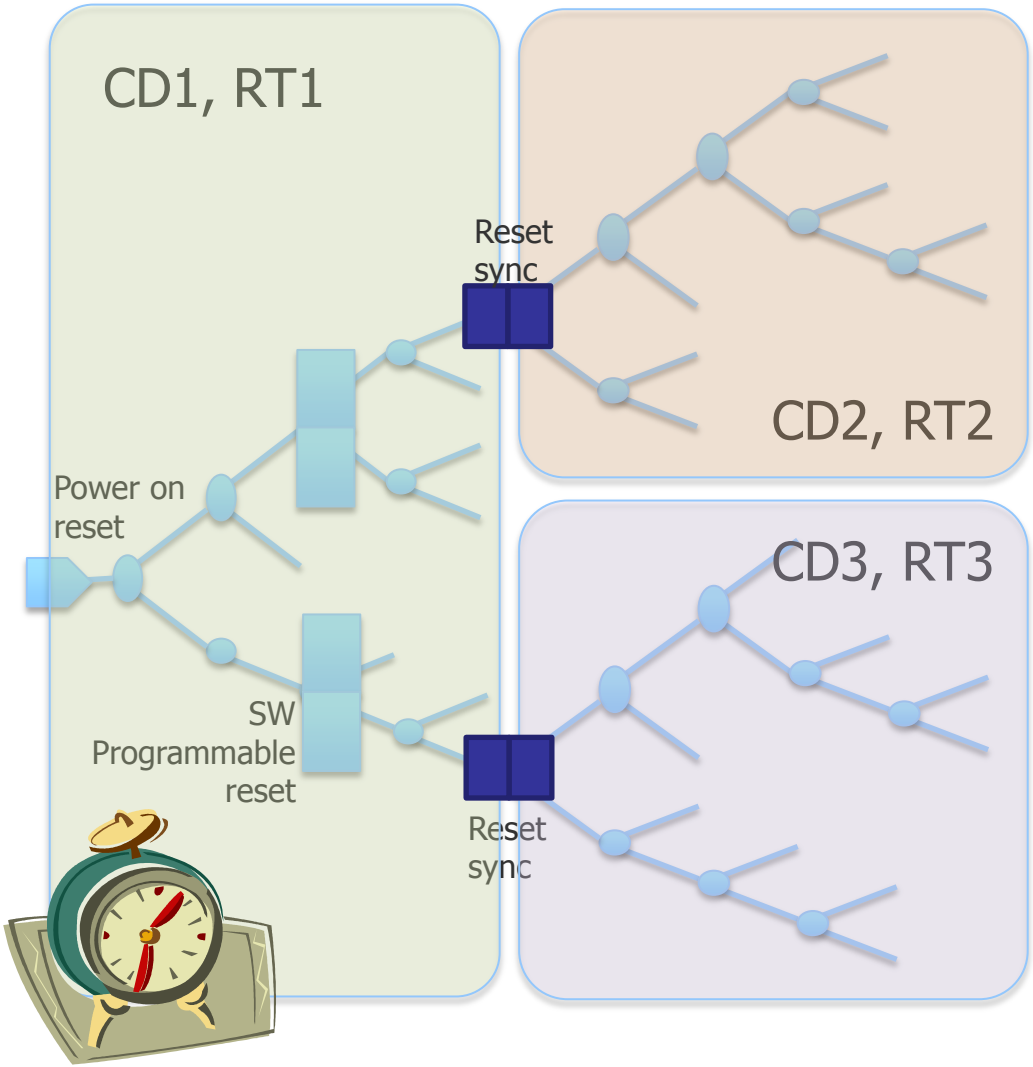
Domain Control Verification

- Power control signals
- Clock select and gating signals
- Reset select and gating signals

Domain Crossing Verification

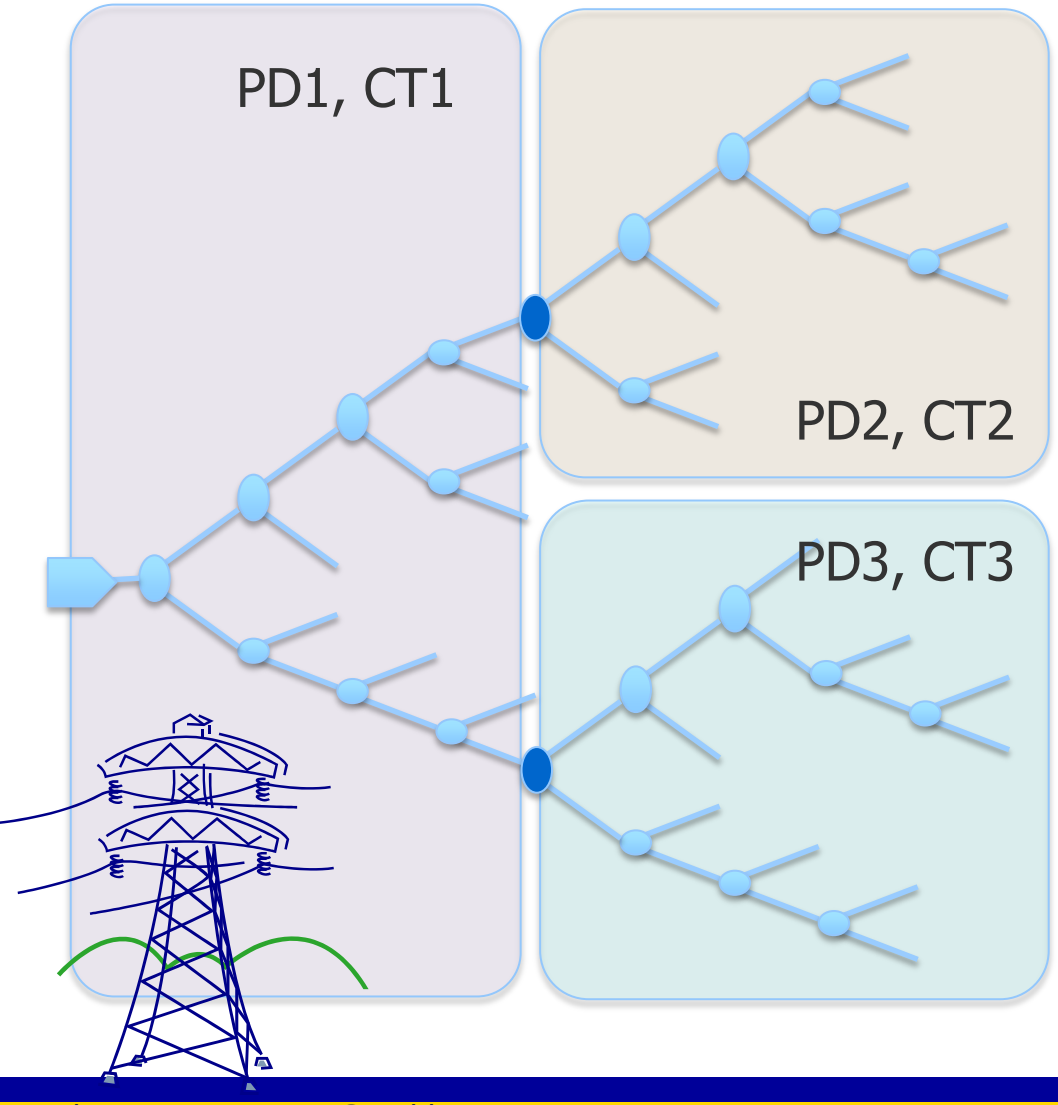
- Power domain crossing
- Clock domain crossing
- Reset domain crossing

Domain Crossing Reset Tree



- The reset tree spans multiple clock domains
- Reset signals need to be synchronized to the target clock domain before used.
- Reset synchronizers need to be used for each clock domain crossing reset signals.

Domain Crossing Clock Tree

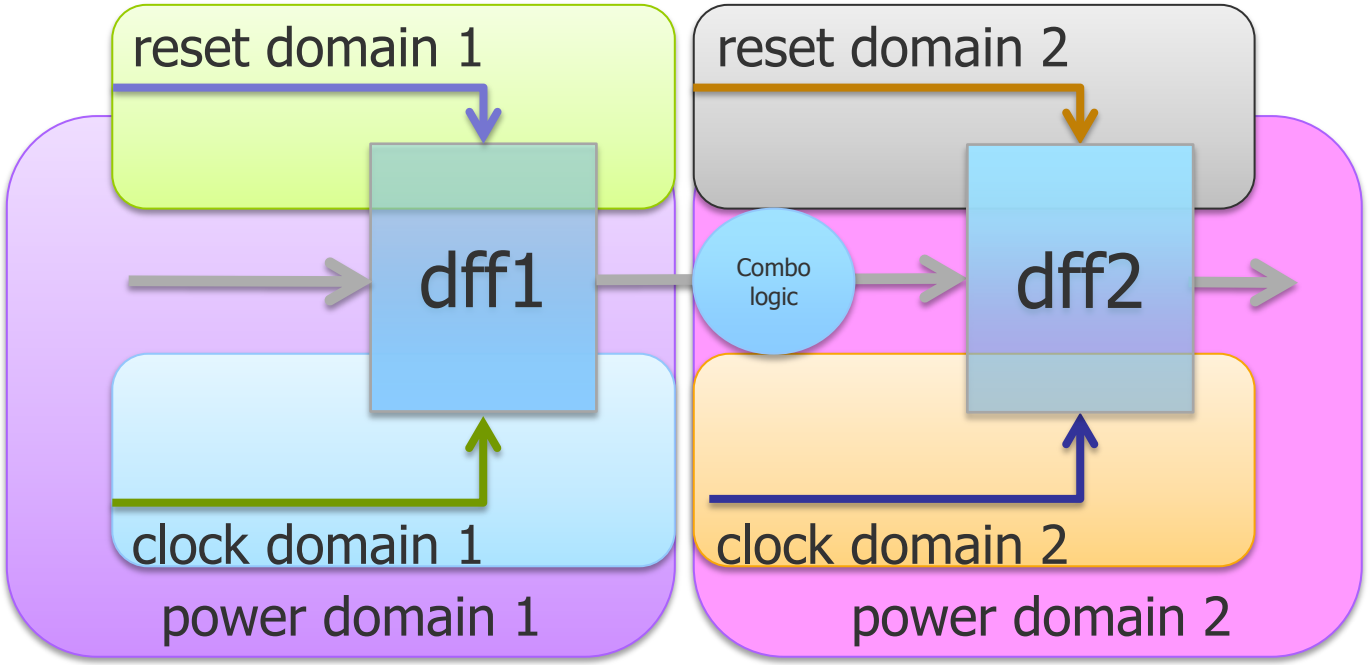


- Although CT2 and CT3 are in the same clock domain, they need to be treated differently because:
  - Different voltage domains
  - Clock switching
- Aynchronous?
- Mesochronous?

Interaction of Various Domains

	Power Supply	Reset Tree	Clock Tree
Power Domain		Reset tree in multiple power domains	Clock tree in multiple power domains
Reset Domain	Power in multiple reset domains		Clock tree in multiple reset domains
Clock Domain	Power in multiple clock domains	Reset in multiple clock domains	

Multi-Domain Verification



- For every register and latch in the design, it is important to know the clock, power and reset domains it belongs to.

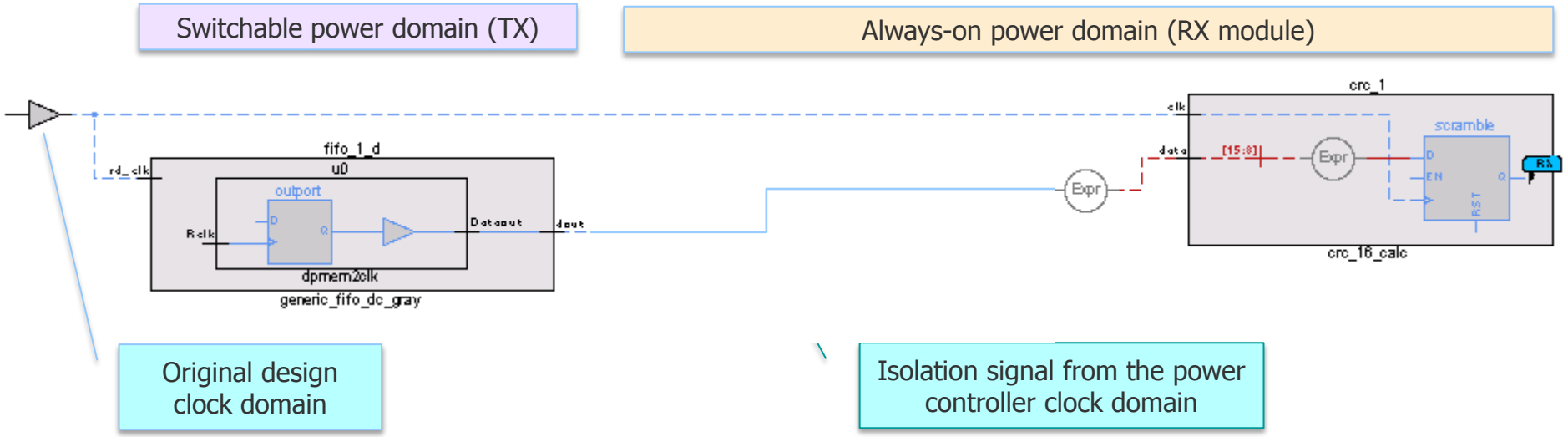
  dff1(pd1,cd1,rd1) → dff2(pd2,cd2,rd2)

Results Multi-Domain Verification

	Block 1	Block 2	Block 3
Power domains	2	3	4
Asynchronous Clock domains	3	4	16
Asynchronous Reset domains	2	11	9

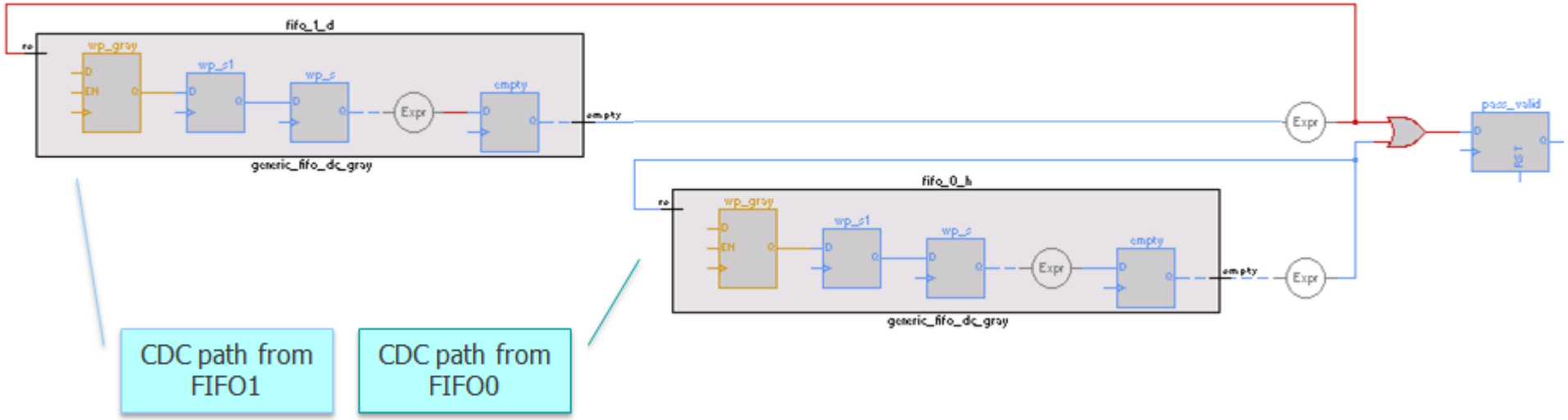
CDC Power Control Signals

- Blocks in different power domains
- Isolation signal introduced a CDC issue



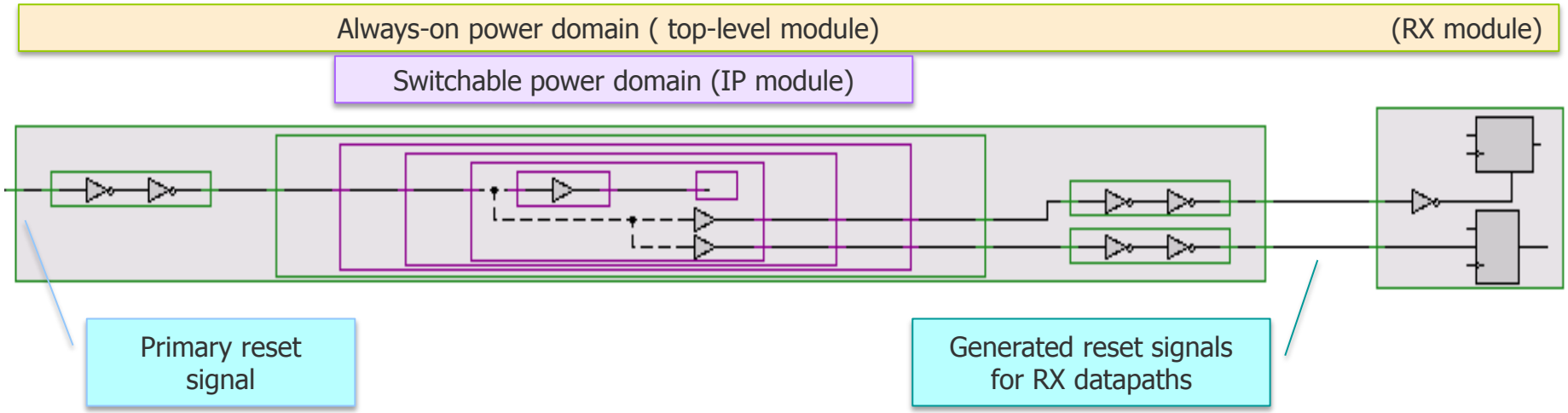
PDC Reconvergence Paths

- Blocks in different power domains
- CDC reconvergence paths depend on timing of power domain on/off



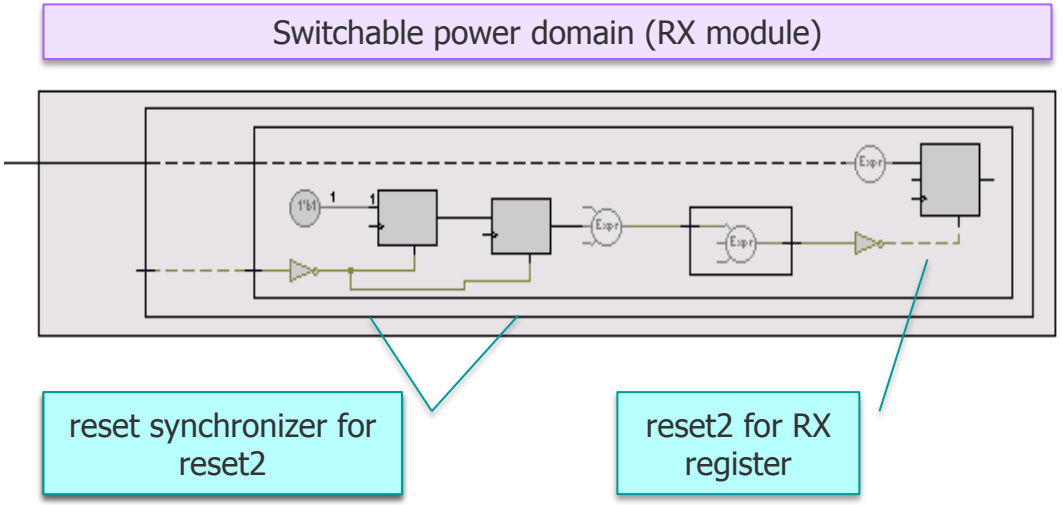
PDC Reset Signals

- Reset signals passed from one module to another
- Reset outputs freeze during power-down



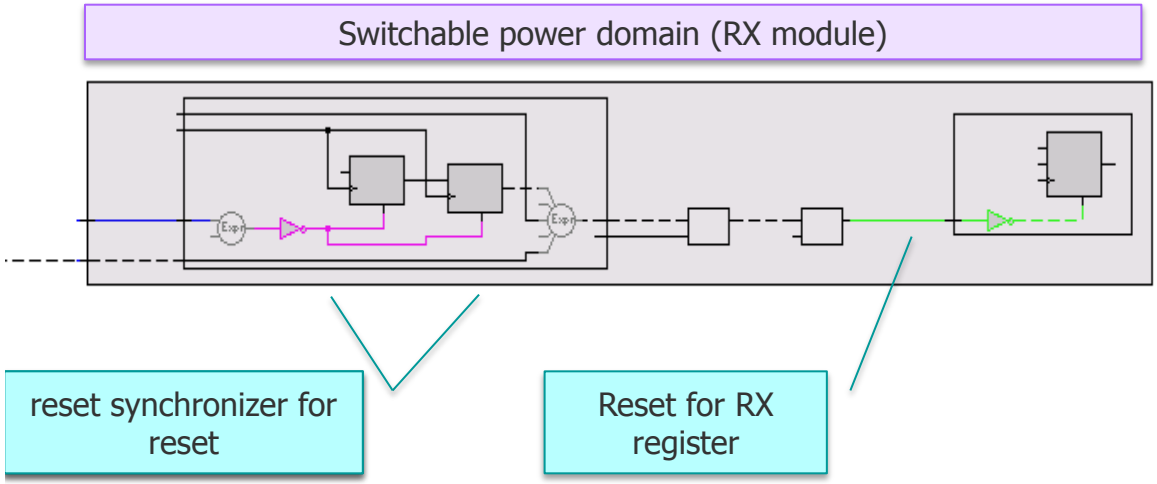
RDC with Power-on Resets

- Reset signal sync'ed for power domain
- Introduce RDC issue with different TX reset



PDC Reset Control Signals

- Reset control signal from another module
- May block initialization after power cycle
- Useful to deploy connectivity verification with simulation and/or formal verification



Summary

- Multi-Domain Verification
  - verifies the power, clock and reset domains together
- 3 phases:
  - domain structure verification
  - domain control verification
  - domain crossing verification
- Prototype environment in place
  - Finding *missed* issues and *interesting* scenarios
- Integrated
  - Formal connectivity verification
  - Simulation with assertions