Multi-Domain Verification: When Clock, Power and Reset Domains Collide

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Agenda

- Low Power Design Techniques
- Domain Specific Verification
  - Clock domain crossing
  - Reset domain crossing
  - Power domain crossing
- Multi-Domain Verification
  - Interaction of Various Domains
- Results Multi-Domain Verification
- Summary
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<th>Scheme</th>
<th>Impact</th>
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<tbody>
<tr>
<td>Clock Gating</td>
<td>Low effect, Moderate saving, UPF not required (affecting clock)</td>
</tr>
<tr>
<td>Multi-Threshold ($V_{th}$) Optimization</td>
<td>No change to RTL and Verification flow, Moderate saving</td>
</tr>
<tr>
<td>Power Gating (PG)</td>
<td>Power architecture, UPF specification, Big saving (affecting power, clock, reset)</td>
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<tr>
<td>Multiple Supply Voltage (MSV)</td>
<td>Power architecture, UPF specification, Big saving (affecting power, clock, reset)</td>
</tr>
<tr>
<td>Dynamic Voltage &amp; Frequency Scaling (DVFS)</td>
<td>Power architecture, UPF specification, Big saving, Verification challenging</td>
</tr>
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# Domain Specific Verification

<table>
<thead>
<tr>
<th>Domain</th>
<th>Domain Structure</th>
<th>Domain Control</th>
<th>Domain Crossing</th>
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<tr>
<td><strong>Power Domain</strong></td>
<td>Power supply nets</td>
<td>Power switching, isolation and retention control</td>
<td>Power domain crossing (PDC)</td>
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<td>Isolation, Retention, Level shift</td>
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<tr>
<td><strong>Reset Domain</strong></td>
<td>Async and sync reset, tree structure, connectivity</td>
<td>Reset synchronization, polarity, control and gating conditions</td>
<td>Reset domain crossing (RDC)</td>
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<tr>
<td><strong>Clock Domain</strong></td>
<td>Async and sync clocks, tree structure, connectivity</td>
<td>Clock division, control and gating conditions</td>
<td>Clock domain crossing (CDC)</td>
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<td>Synchronizers, 2DFFs, FIFO and handshake structures</td>
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Clock Domain Crossing Issue

Setup Violation: Transition at input of synchronizer will propagate to output after **2 or 3** active edges of Rx clock in silicon
Reset Domain Crossing Issue

- Registers, dff1 and ddf2 are in same clock domain — Their reset, rst1 & rst2, are asynchronous
- If rst1 is asserted while rst2 is not asserted — the asynchronous output data from dff1 can cause metastability on dff2.
Power Domain Issues

- Power Domains
- Supply Networks
- Power Gating
- Corruption
- Isolation
- Retention
- Multi-Voltage
- Level Shifting
- Power States
- ...

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Multi-Domain Verification

Domain Structure Verification
• Power supplies
• Clock trees
• Reset trees

Domain Control Verification
• Power control signals
• Clock select and gating signals
• Reset select and gating signals

Domain Crossing Verification
• Power domain crossing
• Clock domain crossing
• Reset domain crossing
The reset tree spans multiple clock domains.

Reset signals need to be synchronized to the target clock domain before used.

Reset synchronizers need to be used for each clock domain crossing reset signals.
Although CT2 and CT3 are in the same clock domain, they need to be treated differently because:

- Different voltage domains
- Clock switching

- Aynchronous?
- Mesochronous?
### Interaction of Various Domains

<table>
<thead>
<tr>
<th></th>
<th>Power Supply</th>
<th>Reset Tree</th>
<th>Clock Tree</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power Domain</strong></td>
<td></td>
<td>Reset tree in multiple power domains</td>
<td>Clock tree in multiple power domains</td>
</tr>
<tr>
<td><strong>Reset Domain</strong></td>
<td>Power in multiple reset domains</td>
<td></td>
<td>Clock tree in multiple reset domains</td>
</tr>
<tr>
<td><strong>Clock Domain</strong></td>
<td>Power in multiple clock domains</td>
<td>Reset in multiple clock domains</td>
<td></td>
</tr>
</tbody>
</table>
For every register and latch in the design, it is important to know the clock, power and reset domains it belongs to.

dff1(pd1,cd1,rd1) → dff2(pd2,cd2,rd2)
## Results Multi-Domain Verification

<table>
<thead>
<tr>
<th></th>
<th>Block 1</th>
<th>Block 2</th>
<th>Block 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power domains</td>
<td>2</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>Asynchronous Clock domains</td>
<td>3</td>
<td>4</td>
<td>16</td>
</tr>
<tr>
<td>Asynchronous Reset domains</td>
<td>2</td>
<td>11</td>
<td>9</td>
</tr>
</tbody>
</table>

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CDC Power Control Signals

- Blocks in different power domains
- Isolation signal introduced a CDC issue
PDC Reconvergence Paths

- Blocks in different power domains
- CDC reconvergence paths depend on timing of power domain on/off
PDC Reset Signals

- Reset signals passed from one module to another
- Reset outputs freeze during power-down
RDC with Power-on Resets

- Reset signal sync’ed for power domain
- Introduce RDC issue with different TX reset
PDC Reset Control Signals

- Reset control signal from another module
- May block initialization after power cycle
- Useful to deploy connectivity verification with simulation and/or formal verification

Switchable power domain (RX module)

reset synchronizer for reset

Reset for RX register

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Summary

- Multi-Domain Verification
  - verifies the power, clock and reset domains together

- 3 phases:
  - domain structure verification
  - domain control verification
  - domain crossing verification

- Prototype environment in place
  - Finding missed issues and interesting scenarios

- Integrated
  - Formal connectivity verification
  - Simulation with assertions