2015 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

Mixed Signal Verification of UPF based designs

A Practical Example

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SYNOPSYS®

Verification for Mobile

- Reducing power consumption is a key design goal
  - Power supply schemes are increasingly complex
  - Additional logic is required e.g. isolation cells, level shifters etc
- Verilog and VHDL do not describe supplies
- An increasing number of designs contain analog IP
- All of the above needs to be thoroughly verified.

Mixed-signal Verification Goals

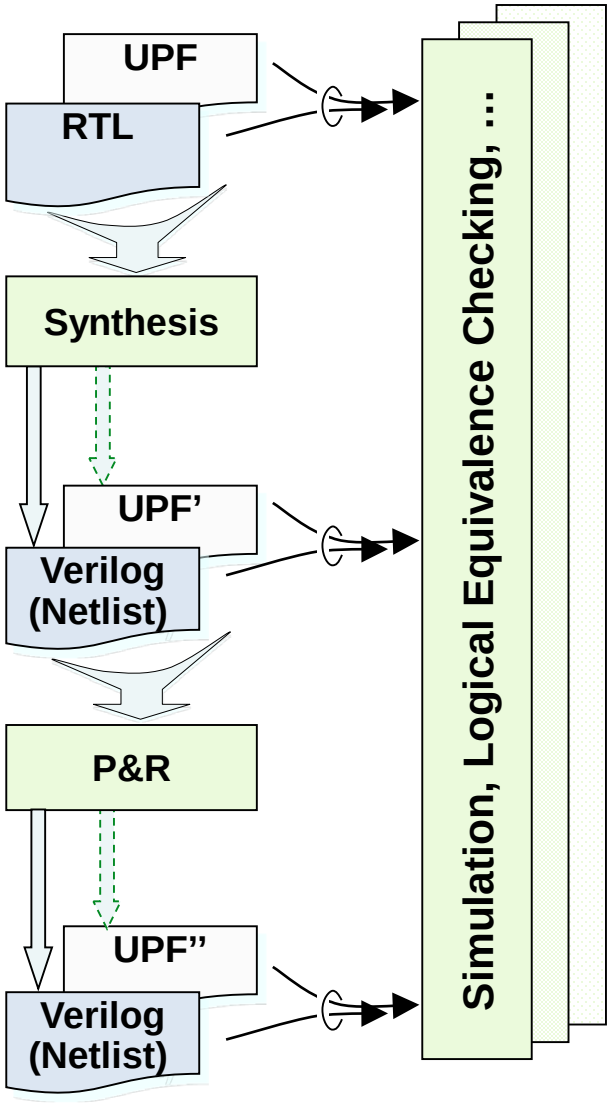
- Verify what you make
  - Avoid ‘hacking’ of netlists
  - Avoid inserting ports/blocks into the simulation that do not exist in the implemented design
- Digital techniques enable a more thorough and automated verification of the mixed-signal system
  - Same SystemVerilog testbench for mixed-signal and “digital” verification
  - SystemVerilog Assertions, functional coverage to avoid ‘eye balling’ of analog results
  - Simulation with UPF to verify power intent

Why Unified Power Format (UPF)?

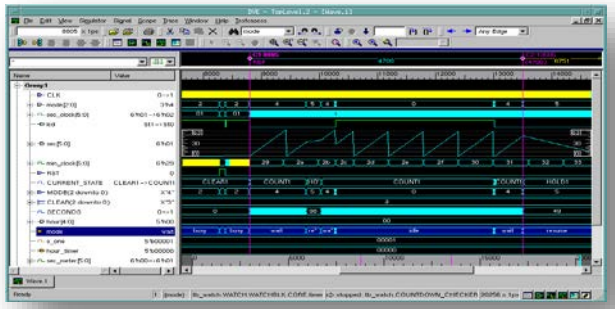
- A dedicated format to describe power intent allows:
  - to keep original RTL unmodified
  - to automatically insert additional logic (isolation, level shifters, switches…)
  - to simulate ‘power effects’ at RTL level (do not wait for Back-end stage)
- UPF is part of the design and should be verified as such

UPF – Used throughout the design flow

- Unified Power Format
  - IEEE standard 1801
- Annotates power intent
- Used by digital engineers in
  - Design
  - Verification
  - Synthesis
  - Layout
- We will focus on verification



Co-simulation in VCS AMS

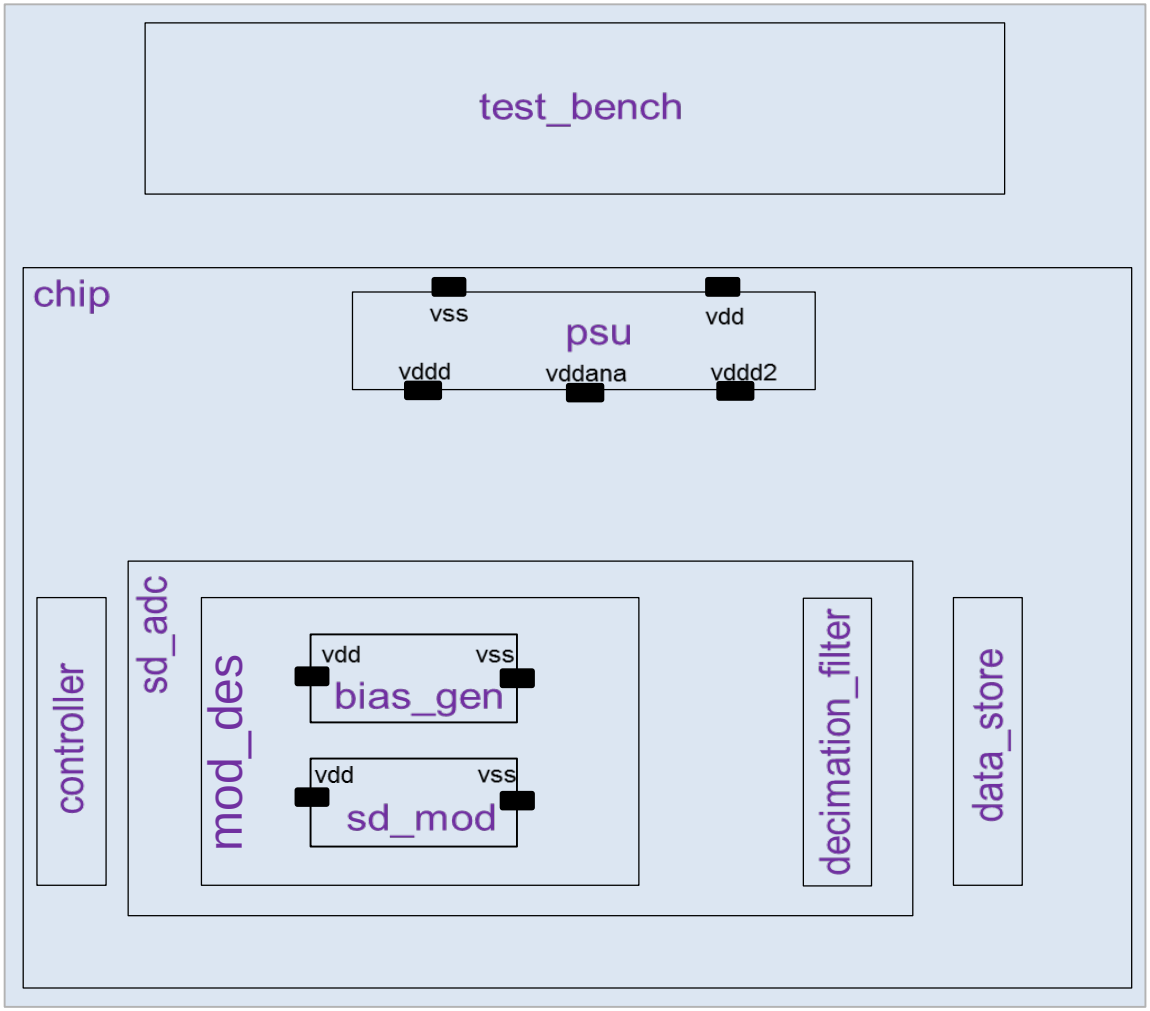


- Combines high performance digital & analog simulation engines
- Direct Kernel Integration
  - Single process, single executable
- Extensive Netlist support
  - Real number models, C-models, SystemVerilog, Verilog-AMS, Verilog-A, Verilog, VHDL, SPICE, DSPF, SDF
- Optimized partitioning of the design
- Automatic insertion of interface elements optimized for accuracy and performance

Digital Design: no power intent defined

Modelling Language

- SPICE
- Verilog



UPF used to define power domains

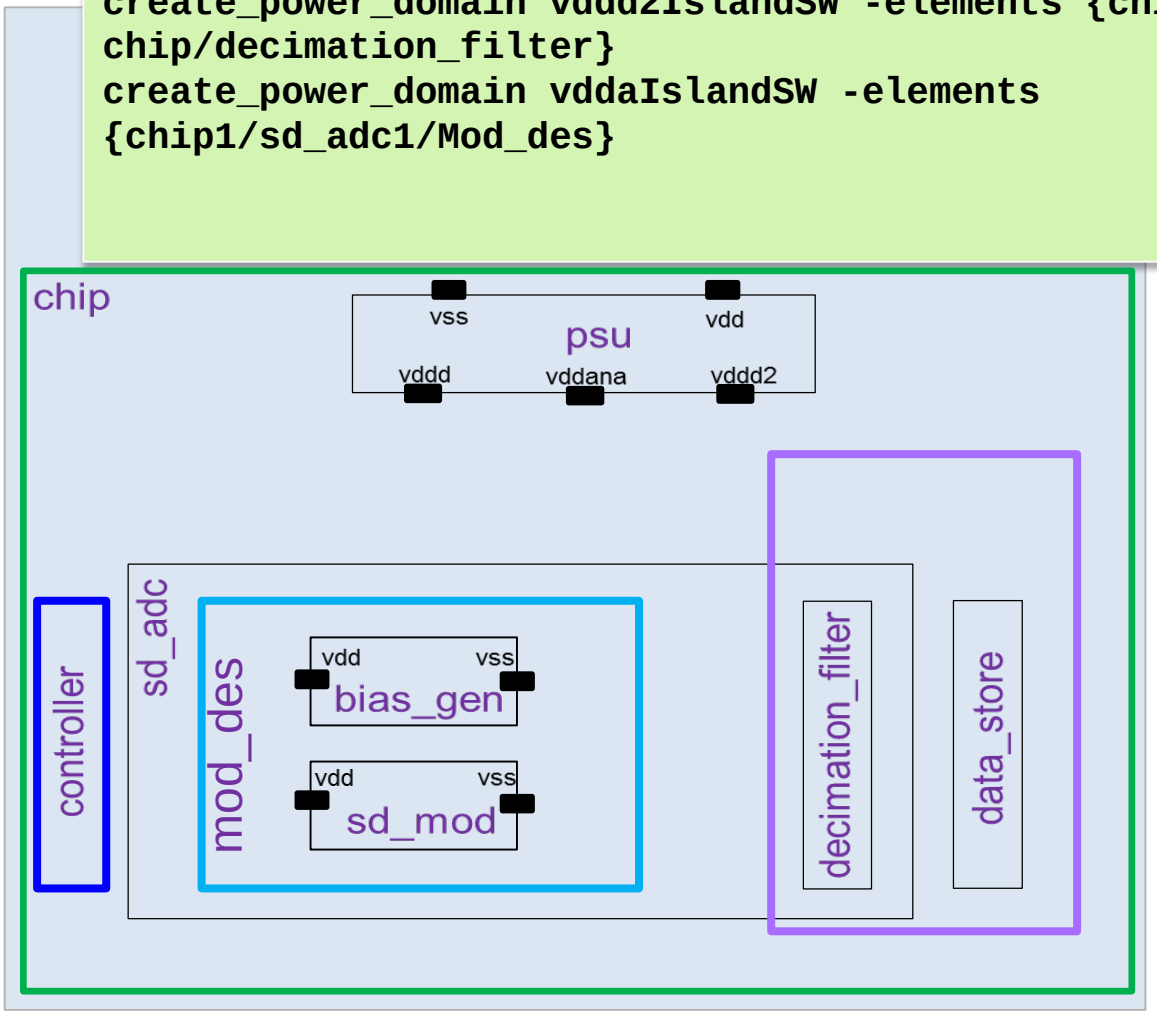
```
create_power_domain PD_TOP –elements {chip}
create_power_domain vdddIsland -elements {chip/control}
create_power_domain vddd2IslandSW -elements {chip/store
chip/decimation_filter}
create_power_domain vddaIslandSW -elements
{chip1/sd_adc1/Mod_des}
```

Modelling Language

- SPICE
- Verilog

Power Domains

- PD_TOP
- vdddIsland
- vddaIslandSW
- vddd2IslandSW



Defi… and …

```
create_supply_port vdd -domain PD_TOP -direction in
create_supply_net vdd -domain PD_TOP
connect_supply_net vdd -ports chip/psu1/vdd
create_power_switch ana -domain PD_TOP -
output_supply_port…
set_isolation iso1 -domain chip1/sd_ …
```

Modelling Language

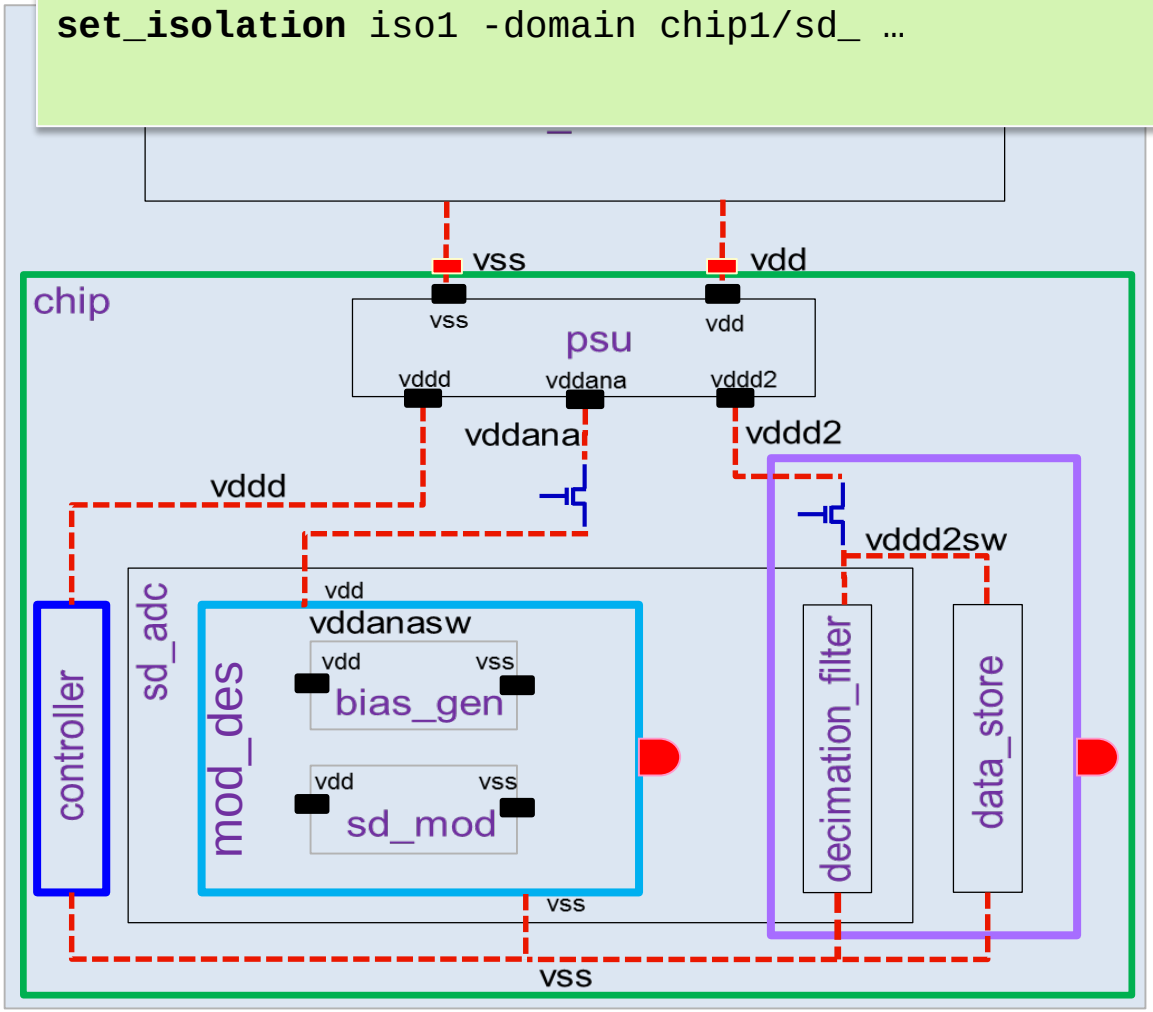
- SPICE
- Verilog

Power Domains

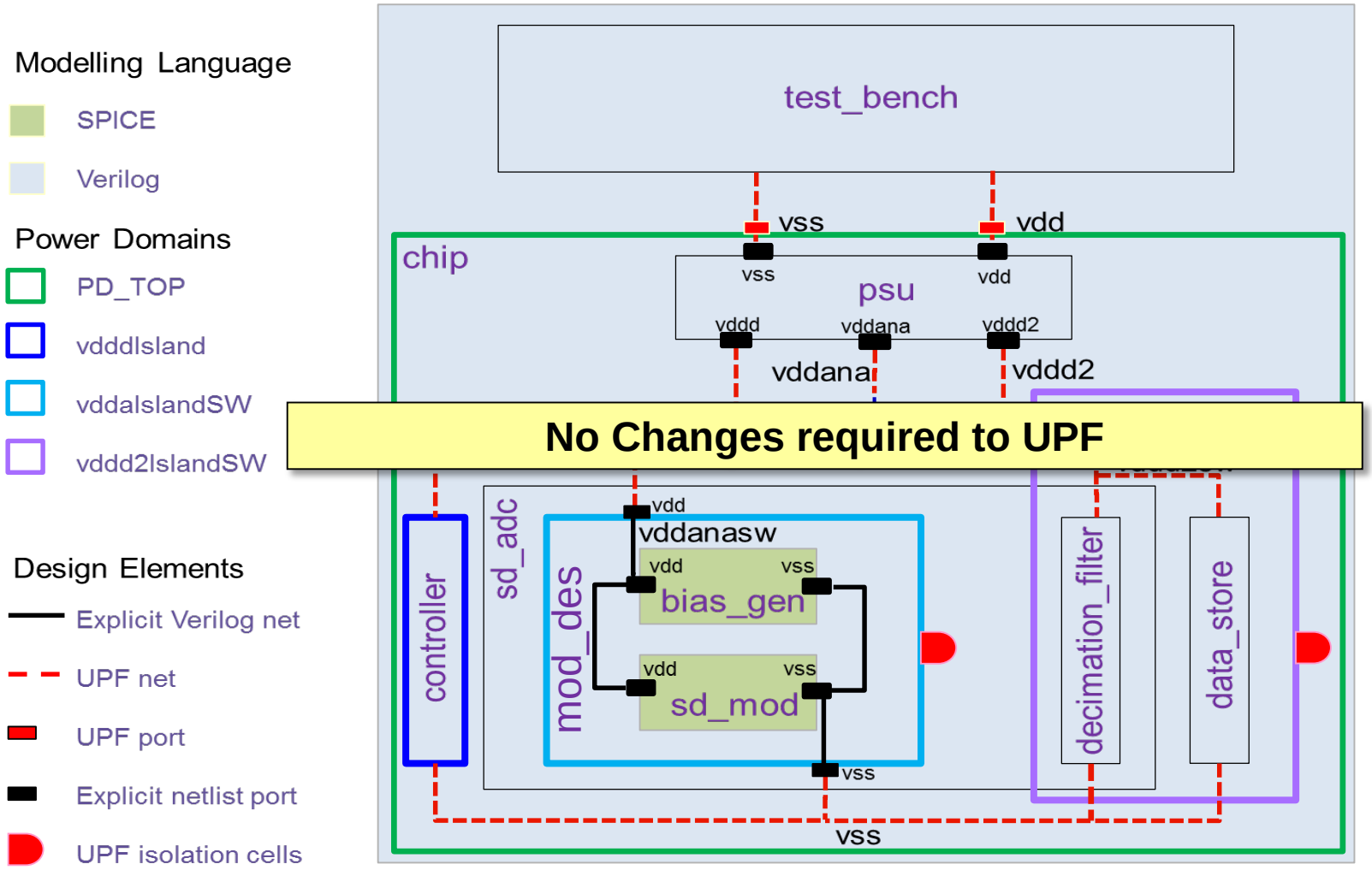
- PD_TOP
- vdddIsland
- vddaIslandSW
- vddd2IslandSW

Design Elements

- Explicit Verilog net
- UPF net
- UPF port
- Explicit netlist port
- UPF isolation cells

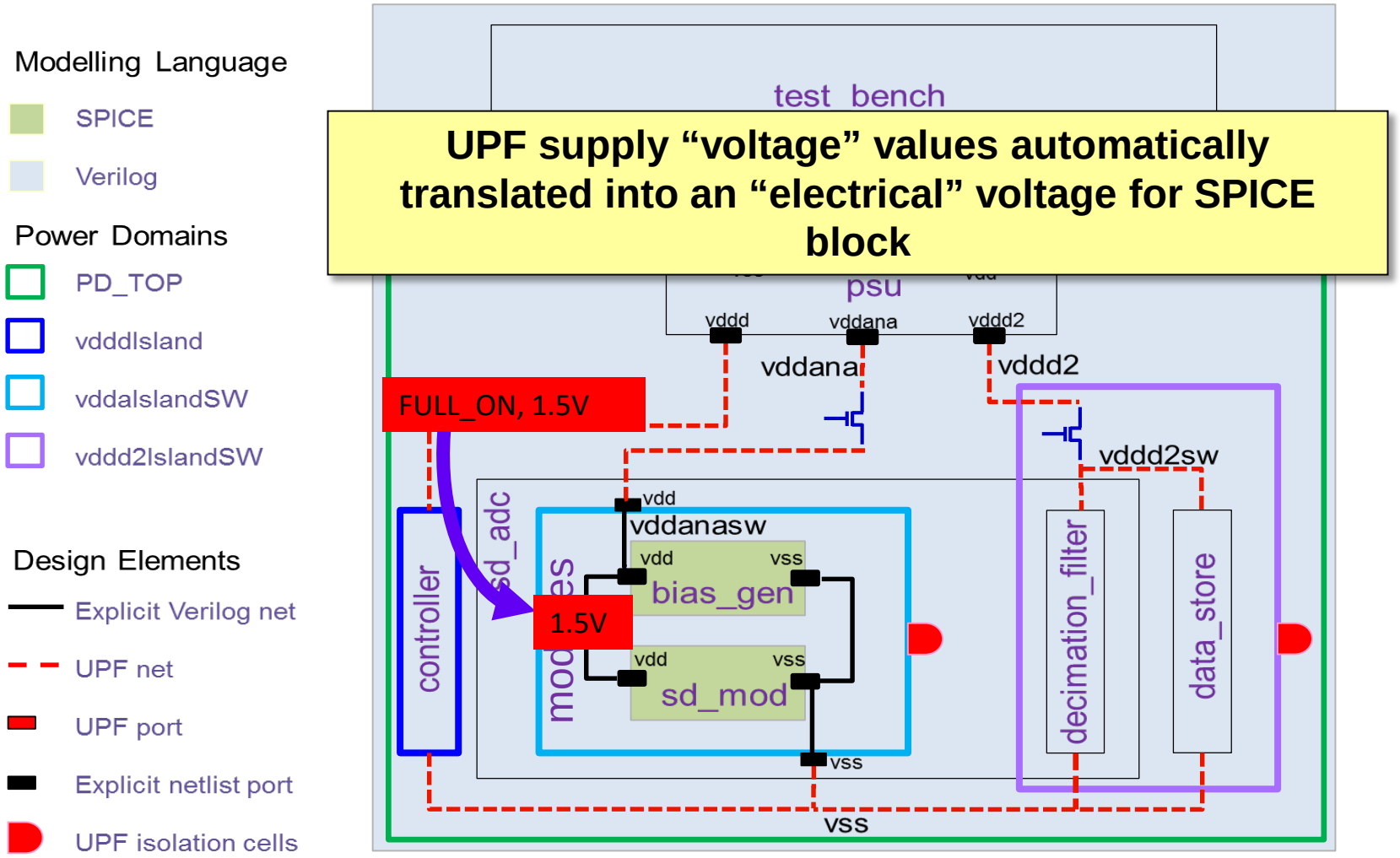


UPF driving SPICE



UPF driving SPICE

UPF supply "voltage" values automatically translated into an "electrical" voltage for SPICE block



Analog supplies can be explicit nets and ports

Modelling Language

- SPICE
- Verilog

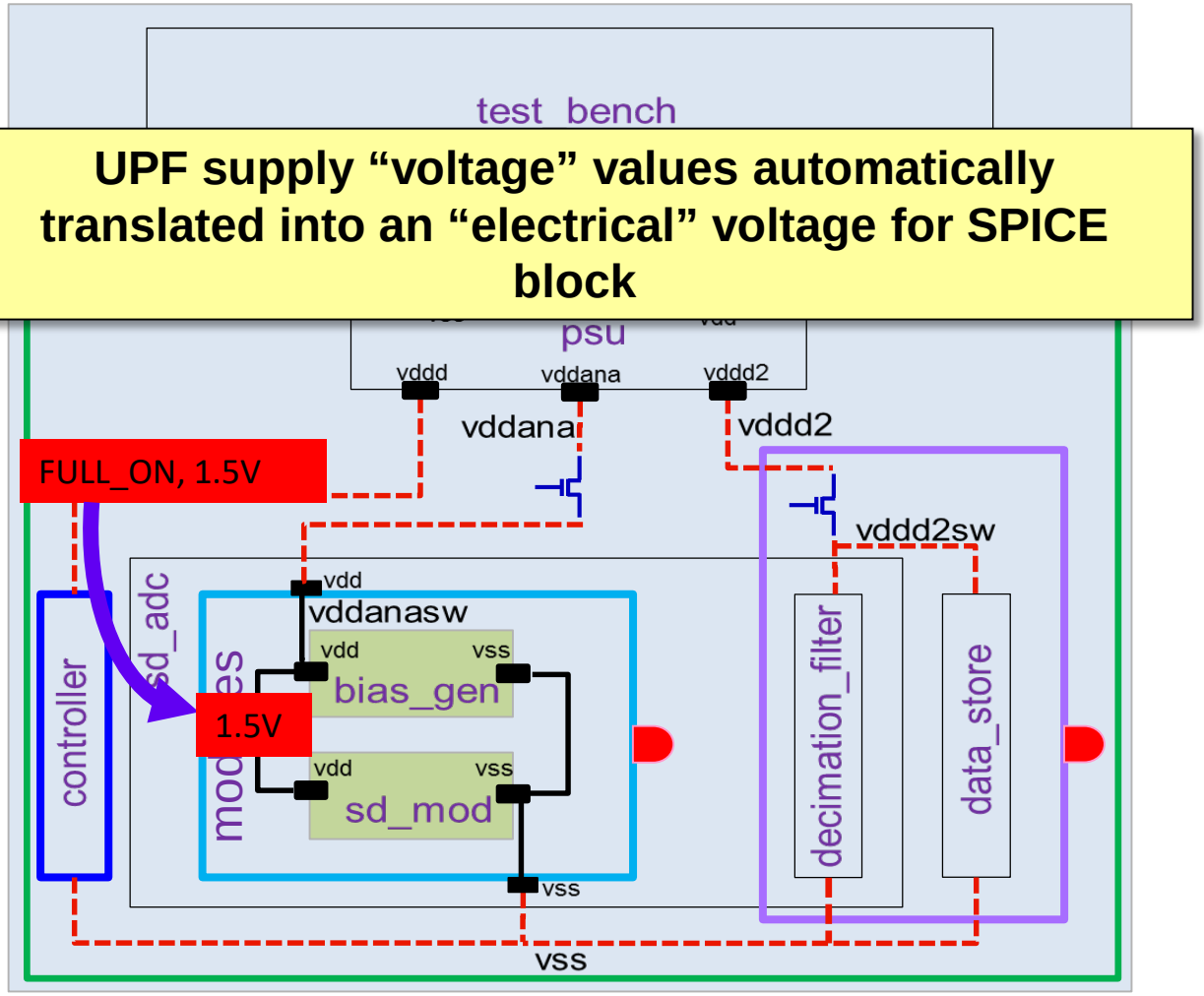
Power Domains

- PD_TOP
- vdddIsland
- vddaIslandSW
- vddd2IslandSW

Design Elements

- Explicit Verilog net
- UPF net
- UPF port
- Explicit netlist port
- UPF isolation cells

UPF supply "voltage" values automatically translated into an "electrical" voltage for SPICE block



Sub-UPF can be used to define analog block supplies

Modelling Language

- SPICE
- Verilog

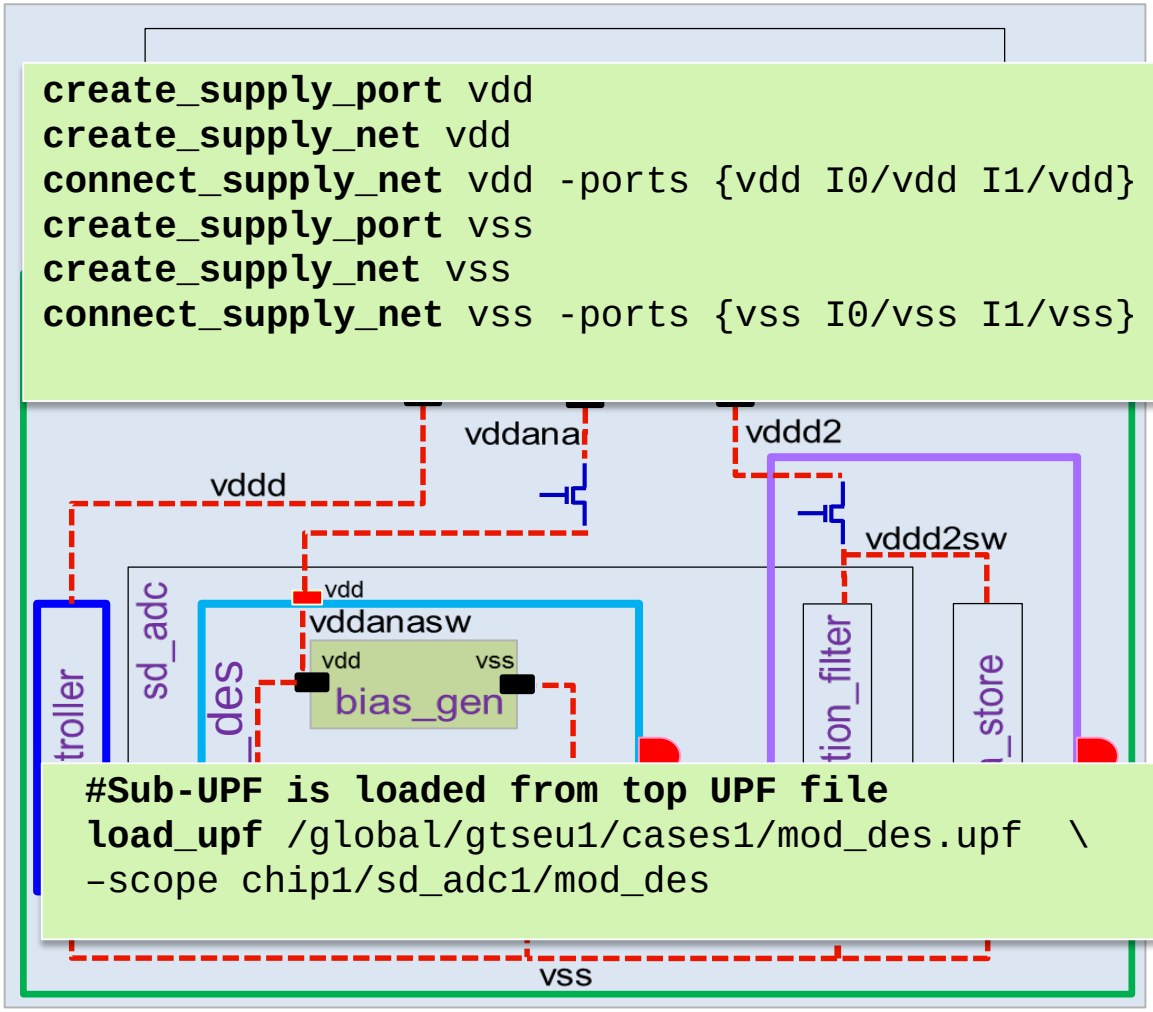
Power Domains

- PD_TOP
- vdddIsland
- vddaIslandSW
- vddd2IslandSW

Design Elements

- Explicit Verilog net
- UPF net
- UPF port
- Explicit netlist port
- UPF isolation cells

```
create_supply_port vdd
create_supply_net vdd
connect_supply_net vdd -ports {vdd I0/vdd I1/vdd}
create_supply_port vss
create_supply_net vss
connect_supply_net vss -ports {vss I0/vss I1/vss}
```




```
#Sub-UPF is loaded from top UPF file
load_upf /global/gtseu1/cases1/mod_des.upf  \
-scope chip1/sd_adc1/mod_des
```

Modeling the PSU

Modelling Language

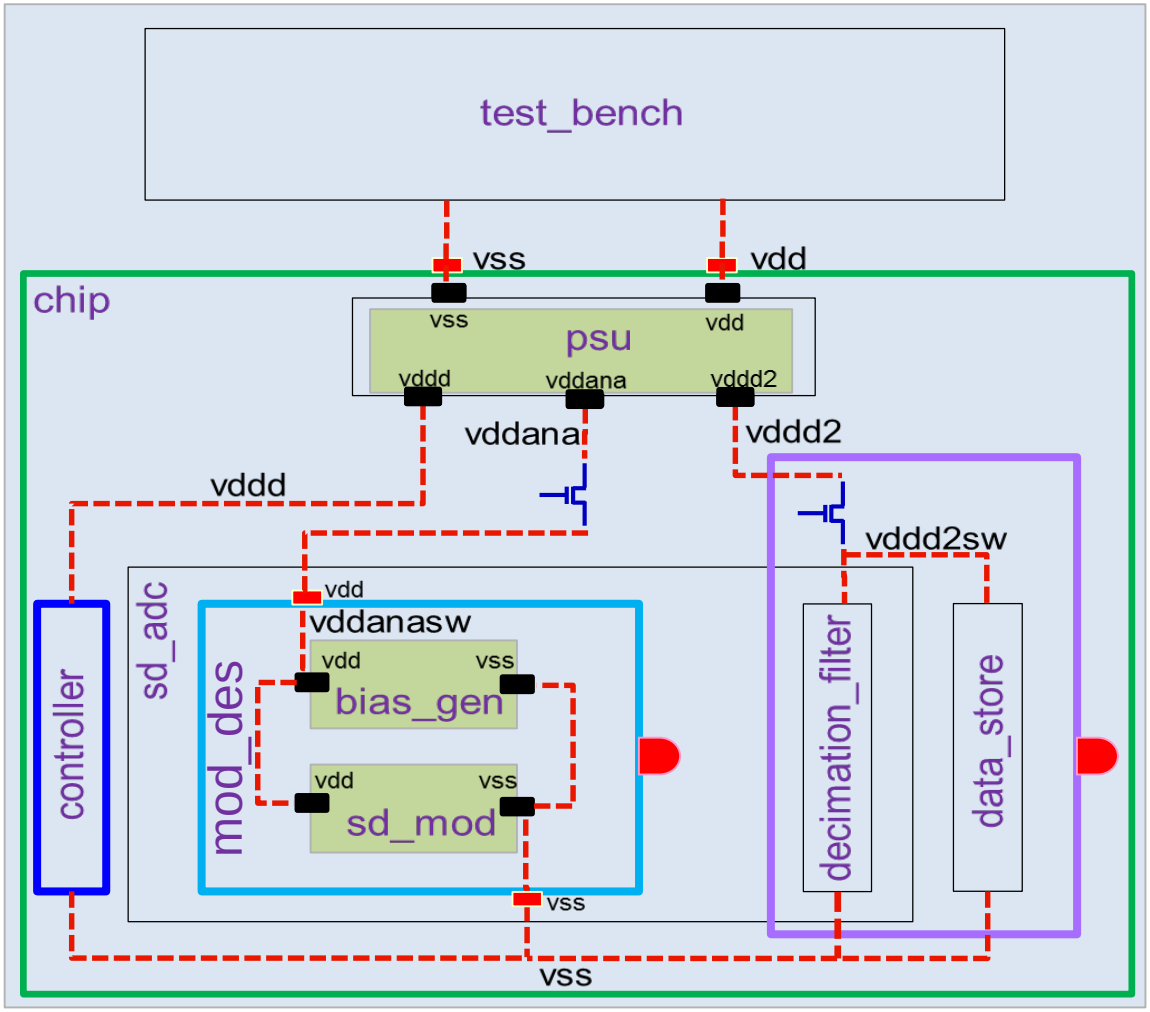
- SPICE
- Verilog

Power Domains

- PD_TOP
- vdddIsland
- vddaIslandSW
- vddd2IslandSW

Design Elements

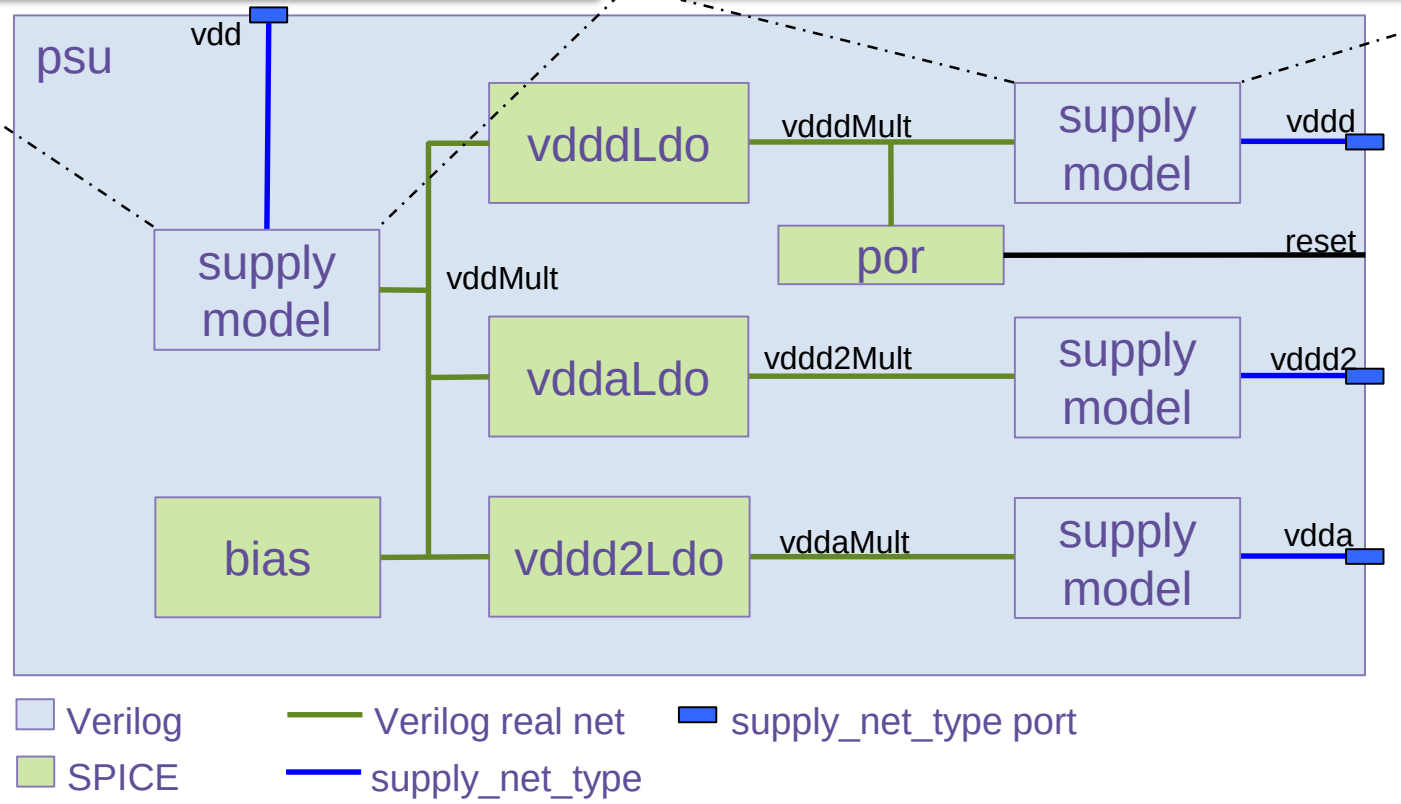
- Explicit Verilog net
- UPF net
- UPF port
- Explicit netlist port
- UPF isolation cells



PSU Block - SPICE driving UPF

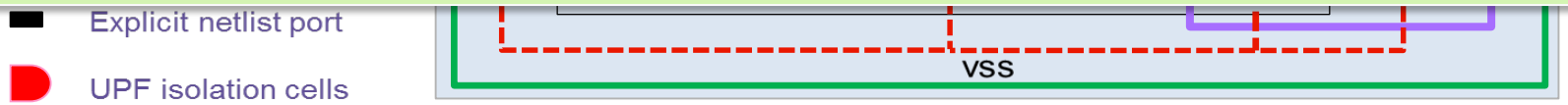
```
always @(vdd.voltage) begin
        vddMult =
vdd.voltage/1e6;
end;
```

```
always @(vdddMult | vdd.state) begin
        vddd.state = vdd.state;
        vddd.voltage = vdddMult*1e6;
end;
```

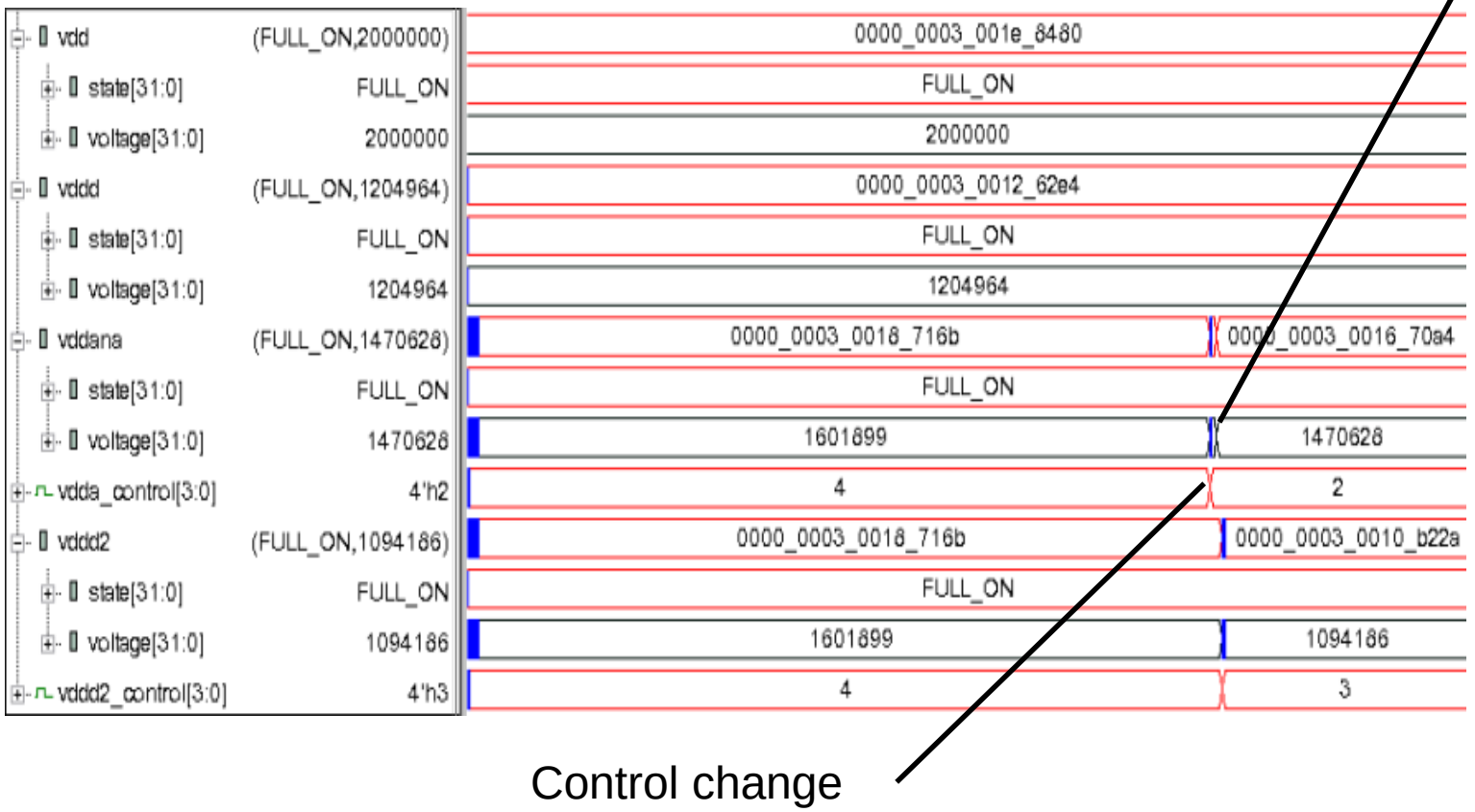


State tables define legal states

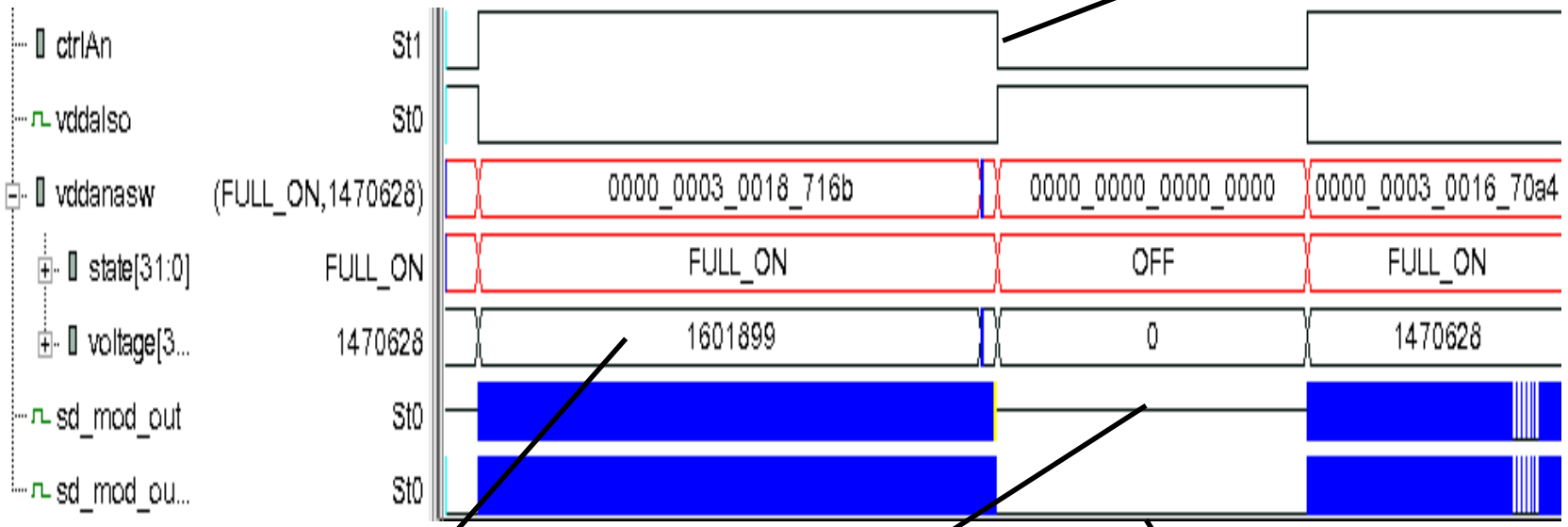
```
add_port_state vdd         -state {highV  1.8 2.1} -state {OFF off}
add_port_state dig/digPout -state {active 1.5 1.8} -state {OFF off}
add_port_state vss         -state {active 0.0}
add_port_state vddd        -state {active 1.0 1.3} -state {OFF off}
add_port_state ana/anPout  -state {active 1.5 1.8} -state {lowV 1.3 1.49} -state
{OFF off}

## CREATE PST
#############
create_pst chiptop_pst -supplies                  {vdd    vddd2sw     vddanasw.}
add_pst_state NormalOp  -pst chiptop_pst -state {highV  active      active...}
add_pst_state StdBy -pst chiptop_pst -state     {highV  OFF         OFF ...   }
add_pst_state PowerSv -pst chiptop_pst -state   {highV  active      lowV ...  }
add_pst_state PowerDwn  -pst chiptop_pst -state {OFF    OFF         OFF  ...  }
```



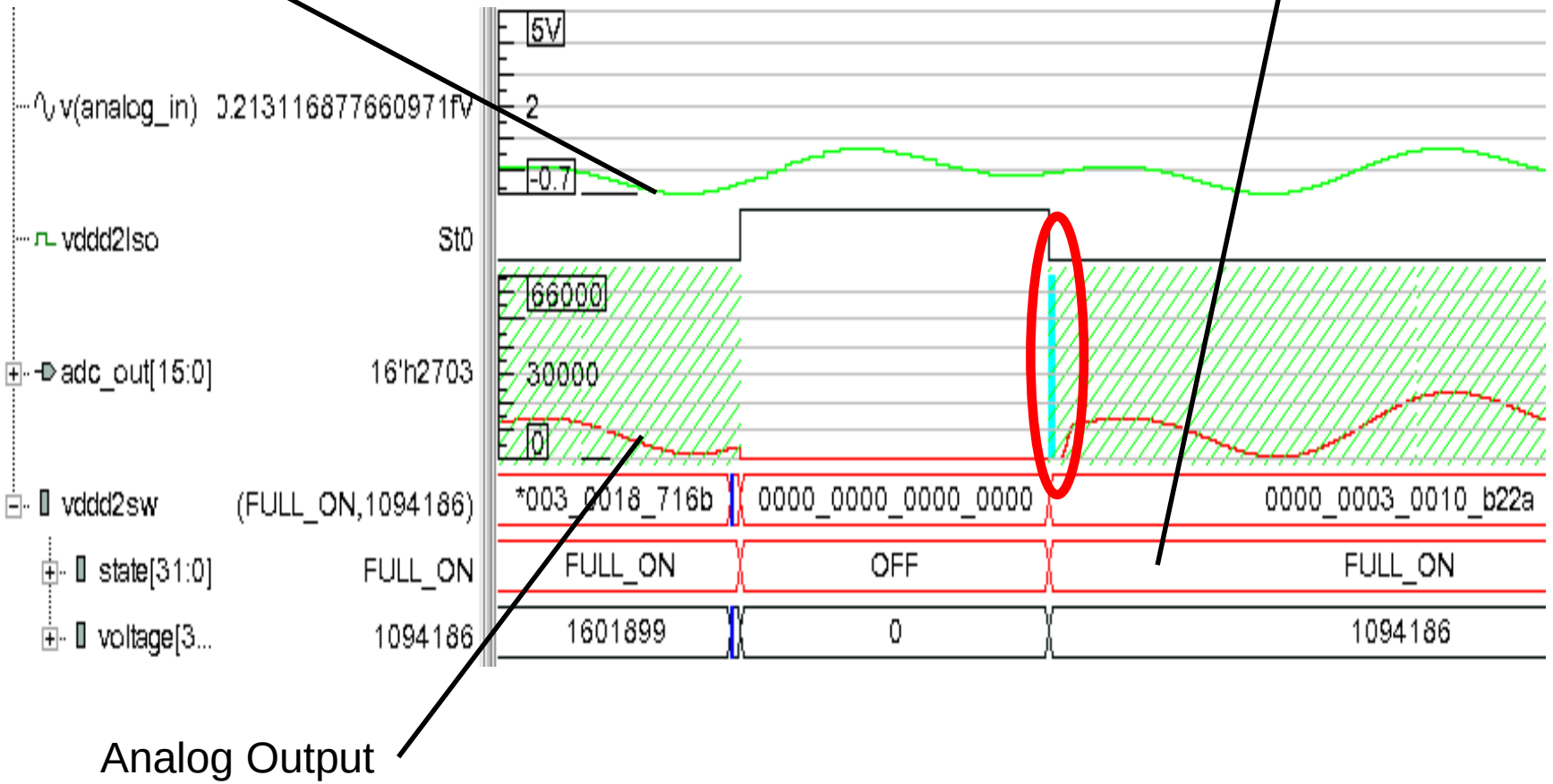
Results: Top level waveforms



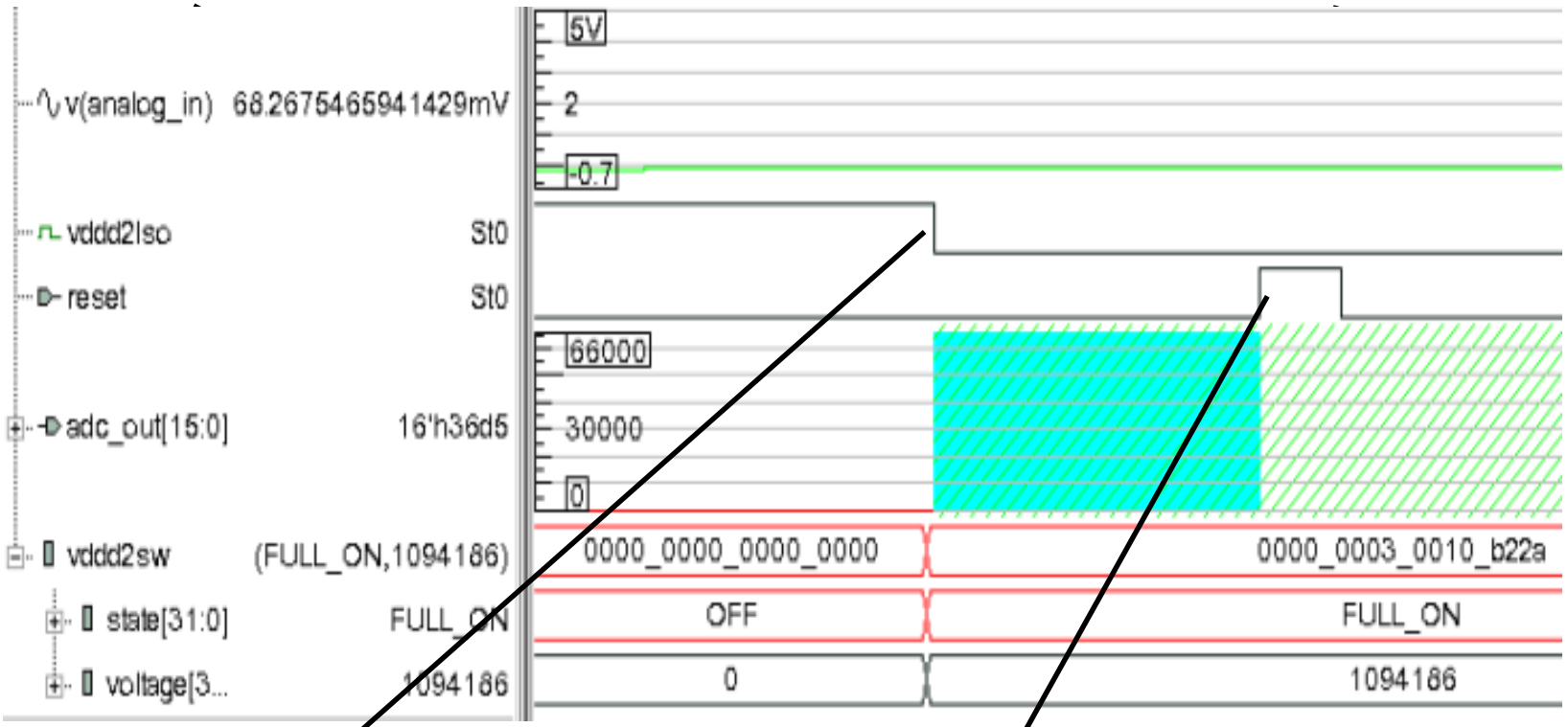
Results: Analog block waveforms



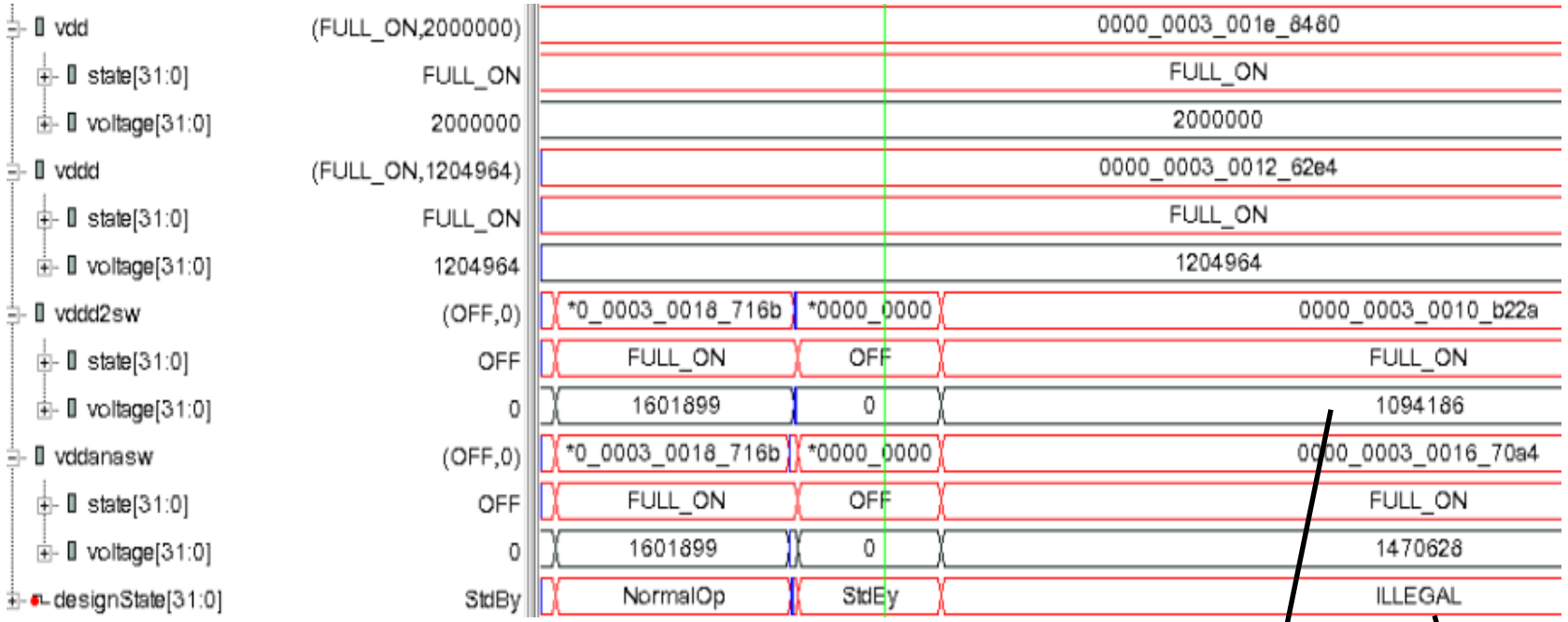
Results: ADC output



Results: Problem!



Results: Power state output



	vdd	vddd2sw	vddanasw	vddd	vss
NormalOp	highV(1.95v)	active(1.65v)	active(1.65v)	active(1.15v)	active(0.00v)
StdBy	highV(1.95v)	OFF(off)	OFF(off)	active(1.15v)	active(0.00v)
PowerSv	highV(1.95v)	active(1.65v)	lowV(1.40v)	active(1.15v)	active(0.00v)
PowerDwn	OFF(off)	OFF(off)	OFF(off)	OFF(off)	active(0.00v)

Low voltage = Illegal state

Conclusions

- Analog blocks can be verified using the “golden” UPF data that will be used for implementation
- Analog blocks can be treated as just another “hard macro”
- UPF based mixed-signal verification can find real design issues
  - Confession: not all of the design errors presented were deliberate

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Thank you

Pierre-Yves Alla

Dave Cronauer

Helene Thibieroz