Mixed-Signal Verification Methodology to Verify USB Type-C

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Abstract

The Universal Serial Bus (USB) Interface has evolved over period of time to become smaller, thinner, easy to use, and an interface of choice for high-speed data transfer. The next-generation USB PHY known as USB Type-C PHY consists of Type-C Power Delivery (TCPD) PHY, USB 3.0 Super-Speed (SS) PHY, and USB 2.0 PHY. USB Type-C PHY supports additional features like plug-orientation/cable-twist detection, Downstream Facing Port (DFP)-to-Upstream-Facing Port (UFP) attach/detach detectio,n and Power Delivery (PD) communication, in addition to existing USB 3.0/2.0 PHY features. USB Type-C PHY features are coupled with analog parameters, necessitating enhancement of conventional digital verification techniques to robustly verify the design.

Here we present a robust mixed-signal verification methodology for USB Type-C PHY using HVL Digital Verification (DV) environment. We demonstrate verification techniques used to verify the plug orientation/cable twist detection, DFP-to-UFP attach/detach detection, and PD communication of TCPD PHY. This methodology has been used to successfully verify the USB Type-C PHY IP in 28nm CMOS technology nodes with first-pass silicon success.

Motivation

- USB interface
  - Standardize the connection of peripheral devices
  - Replace power charger interface
  - More than 100 billion devices in market
    - Ex: Smartphones, pen drives, hard disks, keyboards, etc.

USB 2.0

*Support **High-Speed** data rate of **480 Mbps***

*Delivers up to **2.5W power***

Type-A, Type-B, Mini-A, Mini-B, Micro-A, and Micro-B connectors and cables

USB 3.0

*Support **SuperSpeed** data rate of **5 Gbps***

*Delivers up to **4.5W power***

Micro-A and Micro-B SuperSpeed connectors and cables

Type-C™ USB

*Support **SuperSpeed+** data rate of **10 Gbps***

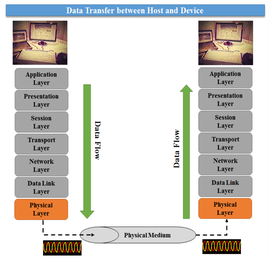
*Delivers up to **100W power***

Robust, Slim connector with Reversible plug orientation and cable Direction

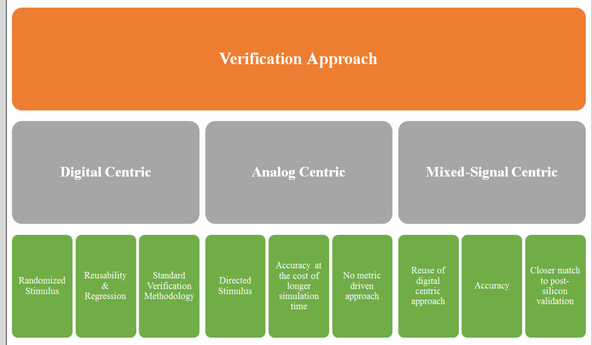
- USB – PHY layer
  - Communicates with physical medium
  - Mixed signal in nature
    - Consists both 'analog' and 'digital' components

- Verification approaches
  - Robust verification methodology
  - Multiple domains verification
    - RTL, gate-level simulation (GLS), and analog/mixed-signal simulation (AMS)
  - Metrics-driven approach
    - Code coverage
    - Functional coverage

Data Transfer between Host and Device

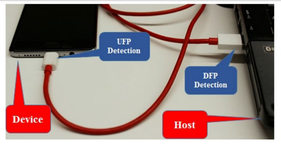


Verification Challenges



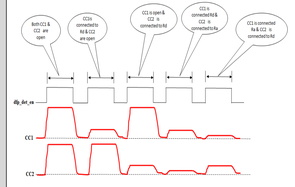
- USB Type-C PHY
  - Plug-orientation/cable-twist detection
  - DFP and UFP detections prior to device enumeration
  - Multiple data rates and voltage domain support
  - Half/full-duplex operation modes
  - Multiple device detection mechanism

Type-C USB Host and Device detection

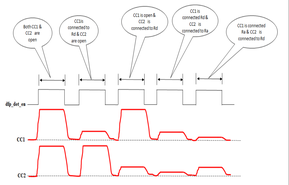


Type-C USB Connector and Plug

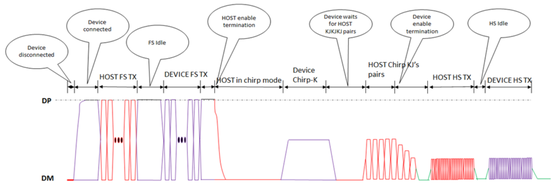
DFP-to-UFP detection at Host side



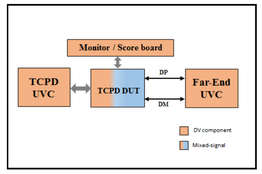
DFP-to-UFP detection at Host side



USB 2.0 enumeration operation



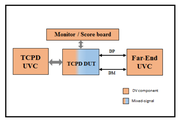
- UVM-based DV environment
  - Digital-centric environment
    - Monitor, scoreboard, functional coverage, and constrained random testcases
  - Difficulties with analog section verification
    - Logical domain representation (Ground - '0', Power Supply – '1')
    - Multiple voltage levels can not be represented

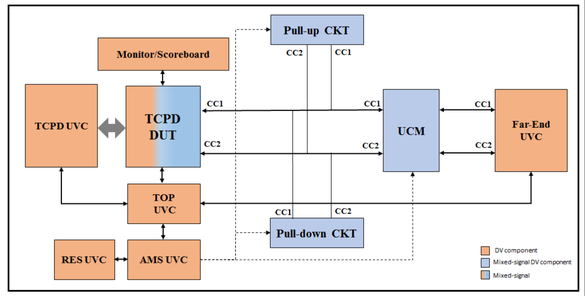


- Impact of using digital-centric verification approach – ***Quality of verification***

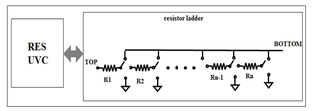
Mixed-Signal Verification Methodology

- Enhancement of digital DV environment
- AMS UVC: Bridge between digital UVCs and mixed-signal components
- Universal connect model (UCM) dynamically converts analog to digital and vice versa

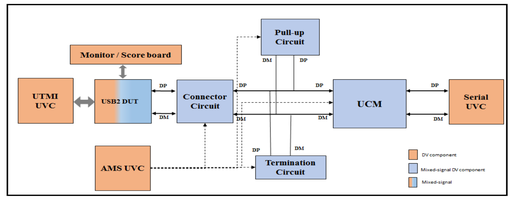


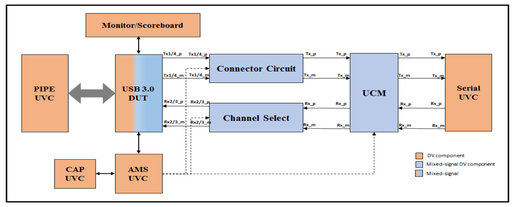


- Pull-up CKT: Represents far-end DFP
  - Dynamically adjust pull-up resistance for different DFP advertisement
- Pull-down CKT: Represents far-end UFP
  - Dynamically adjust pull-down resistance for Ra and Rd connection
- RES UVC: Controls resistance values dynamically during run time
- Functional coverage groups to capture the resistance variation



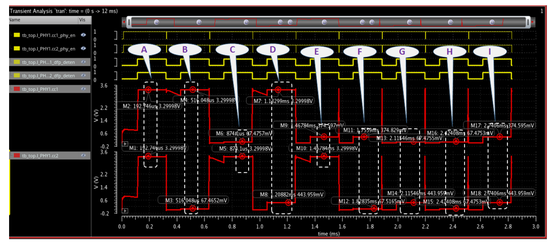
- Enhancements to digital DV environment for USB 2.0 and USB 3.0 PHY verification.



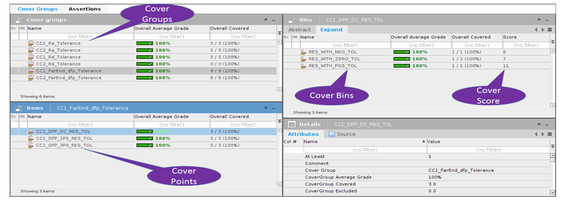


Results and Analysis

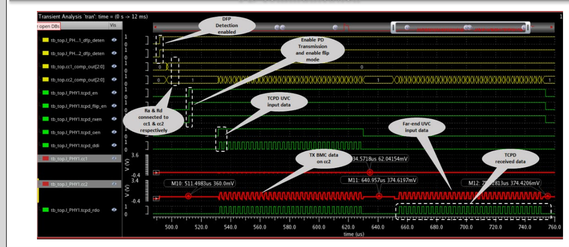
DFP-to-UFP Detection and Cable Orientation Detection



Marker	CC1	CC2	DFP State
A	Open	Open	Nothing connected
B	Open	Ra	Powered cable/No UFP connected
C	Ra	Open	Powered cable/No UFP connected
D	Open	Rd	UFP connected
E	Rd	Open	UFP connected
F	Rd	Ra	Powered cable/UFP connected
G	Ra	Rd	Powered cable/UFP connected
H	Ra	Ra	Debug Accessory Mode connected
I	Rd	Rd	Audio Adapter Mode connected



PD communication



Simulation Runtime Analysis

TCPD Operation modes	DUT configurations (simulation time in minutes)			
	RTL + High Level Behavioral Model	RTL + Detailed Behavioral Model	RTL + Real value model	RTL + SPICE
DFP detection	2	-	-	7
UFP detection	2	-	-	7
PD Communication	3	-	-	9

USB 3.0 Operation modes	DUT configurations (simulation time in minutes)			
	RTL + High Level Behavioral Model	RTL + Detailed Behavioral Model	RTL + Real value model	RTL + SPICE
RX detection	8	8	15	30
TX data transfer	5	8	15	90
RX data transfer	5	10	60	480

USB 2.0 Operation modes	DUT configurations (simulation time in minutes)			
	RTL + High Level Behavioral Model	RTL + Detailed Behavioral Model	RTL + Real value model	RTL + SPICE
Host Disconnection	3	5	-	30
HS data transfer	3	7	-	90
FS data transfer	2	5	-	15
LS data transfer	2	5	-	15

Summary

- Enhanced the HVL DV environment for robust Mixed Signal verification of USB Type-C
- Developed environment components are reusable
- Able to catch mixed signal issues which can not be caught with standard digital simulations
- Can be enhanced to work at sub system level
- Enables confidence in first pass silicon success

Acknowledgment

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