Mixed-Signal Verification Methodology to Verify Type-C USB

Varun R, Vinayak Hegde, Somasunder Kattepura Sreenath

Cadence Design Systems, Inc., Bangalore

Abstract- The Universal Serial Bus (USB) Interface has evolved over period of time to become smaller, thinner, easy-to-use and an interface of choice for high speed data transfer. The next generation USB PHY known as Type-C USB PHY consists of Type-C Power Delivery (TCPD) PHY, USB 3.0 Super-speed(SS) PHY and USB 2.0 PHY. Type-C USB PHY supports additional features like Plug orientation/cable-twist detection, Down-stream Facing Port (DFP)-to-Upstream Facing Port (UFP) attach/detach detection and Power Delivery (PD) communication in addition to existing USB 3.0/2.0 PHY features. Type-C USB PHY features are coupled with analog parameters, necessitating enhancement of conventional digital verification techniques to robustly verify the design.

In this paper, we present a robust mixed-signal verification methodology for Type-C USB PHY using HVL DV environment. We demonstrate verification techniques used to verify the Plug orientation/cable twist detection, DFP-to-UFP attach/detach detection and PD communication of TCPD PHY. This methodology has been used to successfully verify the Type-C USB PHY IP in 28nm CMOS technology nodes with first pass silicon success.

I. INTRODUCTION

Type-C USB provides smaller, thinner and lighter form factors, thus eliminating the challenges of large size and internal volume constraint of the existing Standard-A and Standard-B versions of USB connectors. Type-C USB also standardizes receptacle, cable and plug designs. Thus, it enhances ease-to-use by being plug-able, in either normal or flipped orientation, and in either direction between DFP and UFP. Figure 1 shows the block diagram of USB Type-C System.

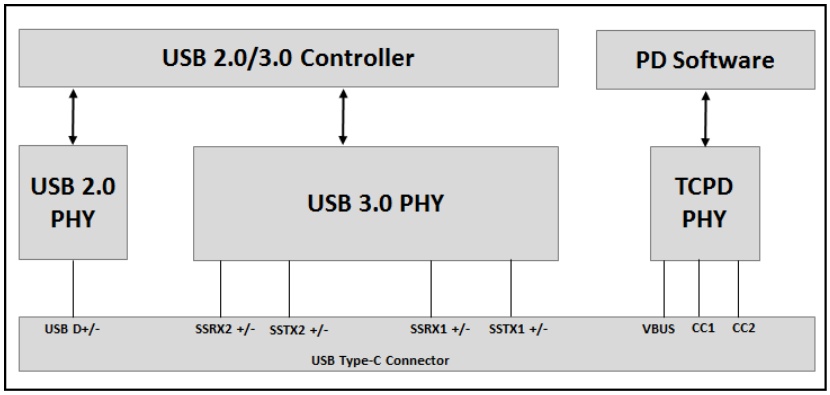

Figure 1. Block diagram of USB Type C System

The Type-C USB PHY supports multiple data rates, power-down modes, half/full communication modes and other additional features. TCPD PHY section performs the plug Orientation/Cable Twist detection, DFP-to-UFP attach/detach detection and power relationship detection prior to the normal USB enumeration process [1]. It provides two paths to deliver power, which can be between 2.5W to 100W depending on the USB PD communication [2]. USB 2.0 PHY provides the data rate of 480 Mbps in High-Speed (HS), 12 Mbps in Full-Speed (FS), and 1.5 Mbps in Low-Speed (LS) modes [3]. It uses half-duplex mode for communication. UBS 3.0 provides the data rate of 5 Gbps in SuperSpeed mode. It uses full-duplex mode of communication [4].

UVM-based HVL DV environment has been developed to verify the Type-C USB PHY. This DV environment provides reusability, well developed constraint random stimulus, protocol checkers, scoreboard, and functional coverage groups. Type-C USB PHY is predominantly analog domain with embedded digital domain. It supports multiple voltage domains, cable orientation detection, multiple connection & disconnection mechanisms, and needs multiple termination setups. These supporting features makes the digital DV environment incapable for

verification sign-off. It is very important and necessary to verify the analog behavior across the all operating modes. In this paper, the mixed-signal verification methodology to verify the Type-C USB PHY is described. This mixed-signal methodology effectively and efficiently reuses the UVM-based DV environment with additional UVCs and mixed-signal components. The verification quality and confidence of the Type-C USB PHY design is improved by implementing mixed-signal verification methodology. Section 2 of the paper explains in detail the verification environment used for verification of Type-C USB PHY. Simulation results are covered in Section 3.

In this paper we have emphasized the verification techniques needed for verifying new features of the USB which are specific to Type-C architecture. Details of mixed signal verification techniques used for verifying USB 3.0 PHY and USB 2.0 PHY are out of scope of this paper and are not covered. We have selectively covered the simulation results of the USB 3.0 PHY and USB 2.0 PHY in results section for the completeness of the paper.

II. VERIFICATION INFRASTRUCTURE

UVM-based HVL verification environment is used for the mixed signal verification of Type-C USB PHY. Verification environment is divided into sub-level verification environments for TCPD, USB 2.0 and USB 3.0 PHYs.

A. TCPD PHY Verification Environment:

Figure 2 shows the block diagram of the mixed signal verification environment used for TCPD-PHY verification.

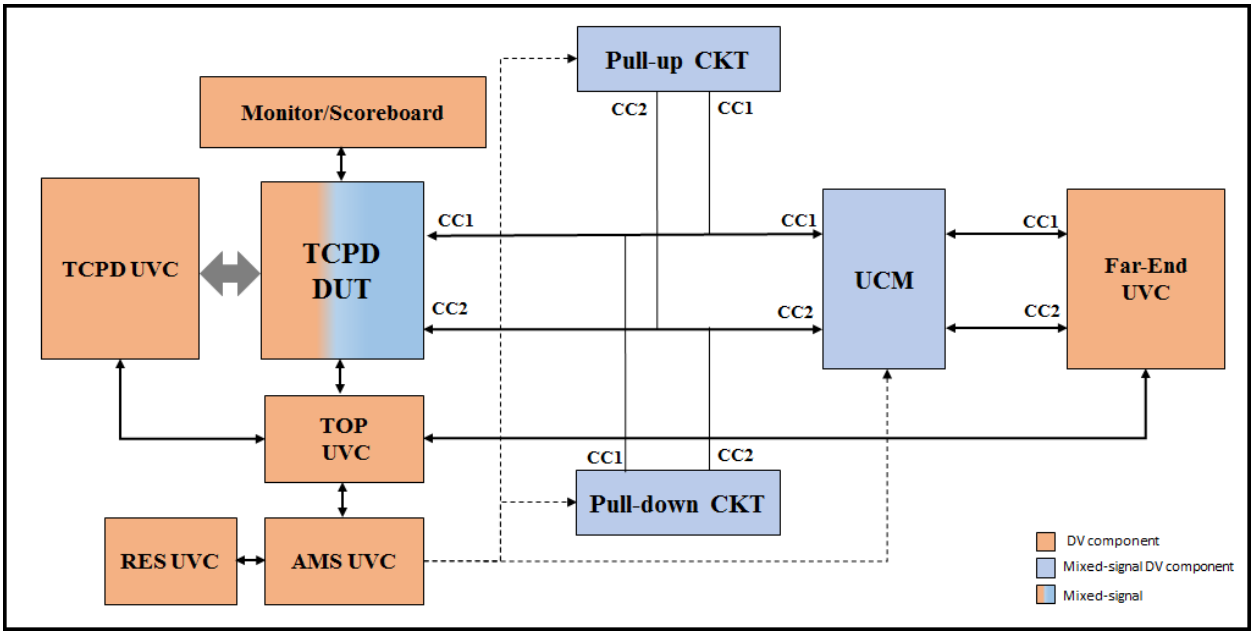

Figure 2. TCPD PHY Verification Environment

The *TCPD UVC* and *Far-End UVC* are used to enable orientation detection, DFP-to-UFP attach/detach detection and PD communication. *TOP UVC* controls both the *TCPD UVC* and *Far-End UVC*. Protocol checks and data integrity checks are accomplished in the *Monitor* and *Scoreboard* respectively. *Pull-up CKT* block is used to pull-up CC1 and/or CC2 pins, in order to represent Far-End DFP. *Pull-down CKT* is used to pull-down CC1 and/or CC2 pins, in order to represent to Far-End UFP. Universal Connect Model (UCM) block is used to convert logic to electrical and vice-versa during PD communication. *AMS UVC* is the bridge between digital UVC and mixed-signal components. *AMS UVC* controls the resistance values dynamically in both *Pull-up CKT* and *Pull-down CKT* through *RES UVC*. *AMS UVC* also controls the U*CM* with different range of rise-time, fall-time and amplitude attenuation during *Far-End UVC* data transmission.

A novel digital verification component – *RES UVC*, has been developed to control the resistance values dynamically during runtime. The block diagram of the RES UVC and resistor ladder is shown in Figure 3. The

Resistor ladder can be configured with different values in *Pull-up CKT* and *Pull-down CKT*. The *RES UVC* dynamically controls the resistance within tolerance limit during DFP or UFP detection. The new functional coverage groups are added to capture the resistor resistance variations.

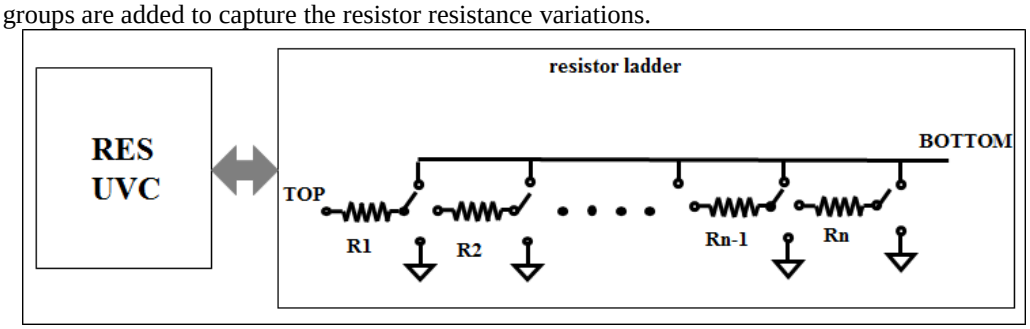

Figure 3. The block diagram of the RES UVC and resistor ladder

a) Pull-up CKT:

Figure 4 shows the block diagram of Pull-up CKT. Purpose of this block is to represent the FarEnd DFP. This block will be controlled by the *AMS UVC* and *RES UVC*. *AMS UVC* controls the default current advertisement of FarEnd DFP. *RES UVC* controls the resistor values of the block.

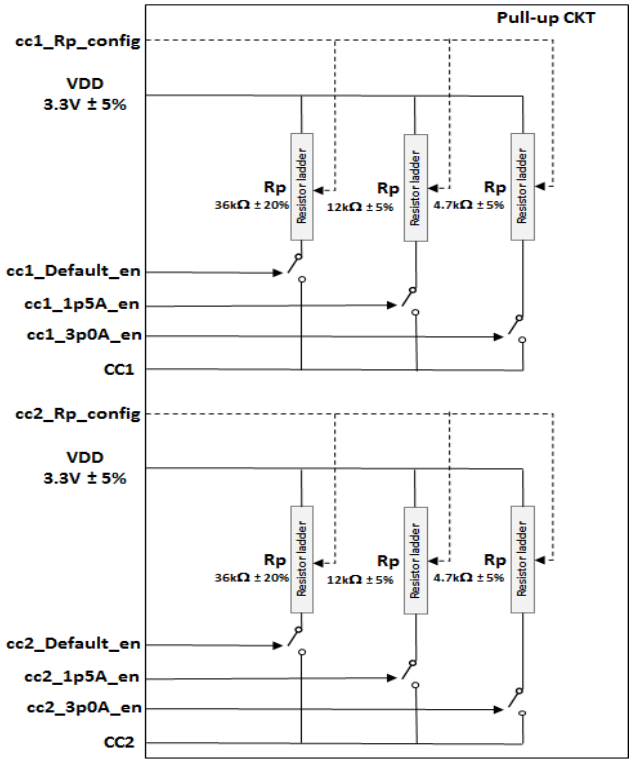

Figure 4. The block diagram of the Pull-up CKT

b) Pull-down CKT:

Figure 5 shows the block diagram of Pull-down CKT. This block is used to represent the FarEnd UFP. *RES UVC* controls the resistor values of the block to represent *Ra* and *Rd* terminations.

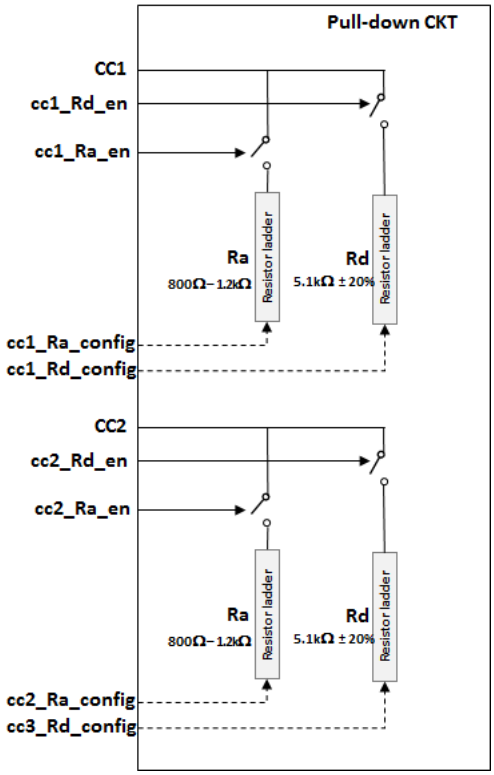

Figure 5. The block diagram of the Pull-down circuit

c) UCM

As the verification environment is made up of HVL, it becomes necessary to have dynamic and effective analog-to-digital and vice versa conversion. This conversion is taken care by a universal connect model (UCM) in the environment. UCM is controlled by *AMS UVC*. During transmission mode, analog data received on the CC1/CC2 line are converted to logic domain and transmitted to verification component to check the data integrity. Similarly during the receive mode of DUT, data being driven from the environment are converted to analog domain before passing to DUT. The threshold voltages, rise time, fall time, maximum amplitude, and minimum amplitude are parameterized and are controlled by the *AMS UVC*. The new functional coverage bins can be added for these parameter values during regression.

d) Digital Verification Components

Verification environment contains multiple verification components. *AMS UVC*, *TCPD UVC* and *Far-End UVC* are three major UVCs used in mixed-signal verification.

The AMS UVC is the bridge between digital UVCs and mixed-signal components in the environment. It controls the pull-up circuit, pull-down circuit, and CM. *AMS UVC* also monitors the *TCPD UVC* and *Far-End UVC* transmission modes and enables electrical-to-logical or logical-to-electrical conversion, respectively.

The *TCPD UVC* enables orientation detection, DFP-to-UFP attach/detach detection and PD communication. It drives the randomized Bi-phase Mark Coding (BMC) data to DUT input during transmission mode. It monitors the CC1/CC2 data from DUT during *Far-End UVC* transmission mode. It has protocol-specific checkers and functional coverage.

The *Far-End UVC* drives the randomized BMC data to CC1/CC2 during Far-End UVC transmission mode. It monitors the CC1/CC2 data from DUT during *TCPD UVC* transmission mode. It also has protocol-specific checkers and functional coverage.

The monitor/scoreboard are part of the digital verification environment. They perform the data integrity checks and protocol checks.

B. USB 2.0/3.0 PHY Verification Environment:

Figure 6 shows the mixed signal verification environment of USB 2.0 PHY. HVL DV environment has been enhanced to use for using in mixed signal verification.

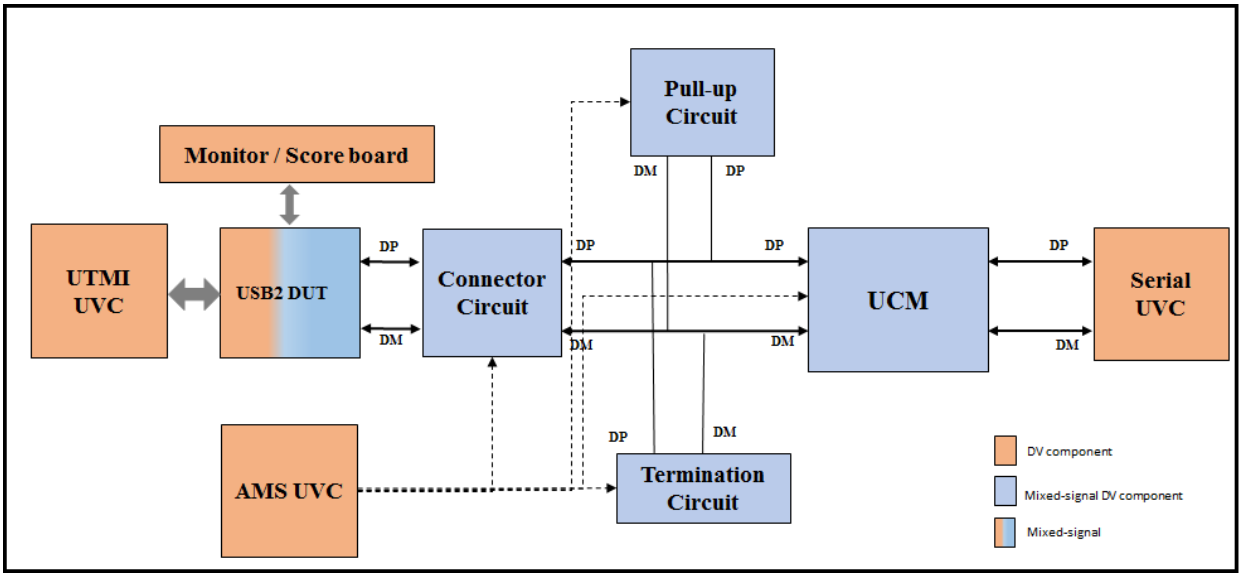

Figure 6. USB 2.0 PHY Verification Environment.

The *UTMI UVC* drives and monitors the digital UTMI parallel data whereas *Serial UVC* drives and monitors the digital data on serial line. The *AMS UVC* is the bridge between digital UVCs and mixed-signal components of environment. It controls Pull-up Circuit, Termination Circuit, Connector Circuitry and 'Universal-Connect-Model (UCM)'. *Pull-up Circuit* enables a pull-up resistor on DP or DM depending on FS or LS mode, respectively. Termination Circuit enables 45Ω termination on both DP and DN in the HS mode. UCM is used to convert logic to electrical and vice versa in different modes of operation. Connector circuit provides the far-end device connection with transmission line having propagation delay of 30 HS bit time [3]. It is modeled to dynamically control the reflection co-efficient of the transmission line by adjusting both characteristic impedance and termination impedance [8].

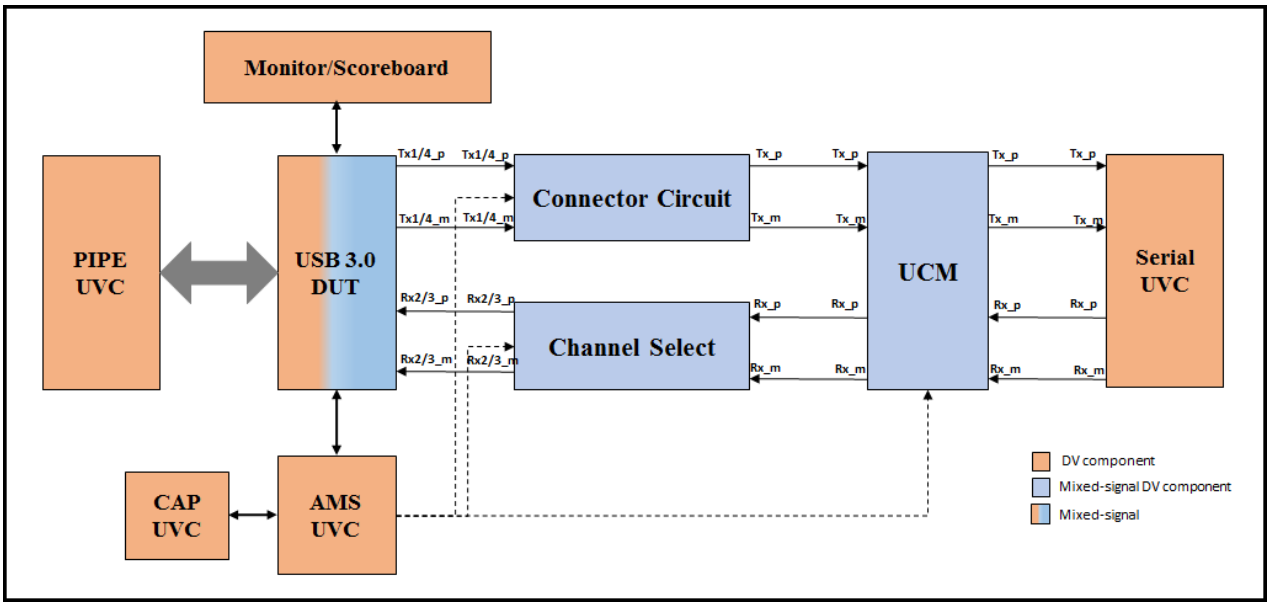

Figure 7. USB 3.0 PHY Verification Environment

Figure 7 shows the mixed signal verification environment of USB 3.0 PHY. The *PIPE UVC* drives and monitors the digital PIPE parallel data whereas *Serial UVC* drives and monitors the digital data on serial line. The *AMS UVC* is the bridge between digital UVCs and mixed-signal components of environment. It controls *Connector Circuit*, *Channel Select* block and 'Universal-Connect-Model (*UCM*)'. *Connector Circuit* provides a far-end RX termination of 50 ohm and coupling capacitor of 75nF – 200nF [4]. It also helps in selection of proper TX differential pair depending on the cable orientation. *Channel Select* block is used to provide multiple channels with different channel attenuation for robust verification of RX data path. UCM is used to convert logic to electrical and vice versa, depending on the Margin/Swing/De-emphasis of the transmitted data. The capacitance of the coupling capacitor can vary dynamically during simulation runtime for the efficient verification of receiver detection feature.

A novel digital verification component – *CAP UVC*, has been developed to control the capacitance values dynamically during runtime. Figure 8 shows the block diagram of the *CAP UVC* and Capacitor ladder. The Capacitor ladder can be configured with different values in *Connector Circuit*. The *CAP UVC* dynamically controls the capacitance within tolerance limit. The new functional coverage groups are added to capture the resistor capacitance variations.

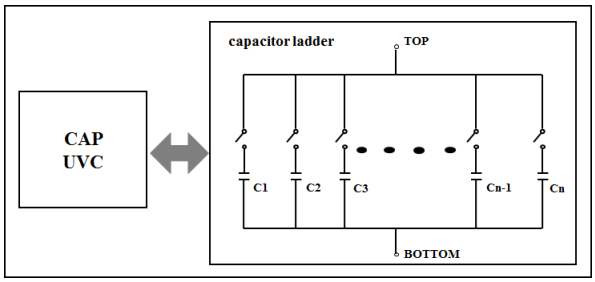

Figure 8. The block diagram of the CAP UVC and capacitor ladder

III. Results and Analysis

This section describes the results obtained from the mixed-signal verification.

A. TCPD PHY Verification

a) DFP-to-UFP valid connection detection and Cable Orientation/Twist detection:

The valid connection is detected by monitoring proper termination at CC1/CC2 pin. The Figure 9 and Figure 10 show the valid connection between DFP-to-UFP – first DUT as a DFP and next DUT as a UFP.

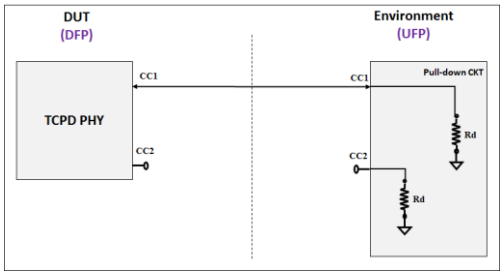

Figure 9. The valid connection - DUT as a DFP

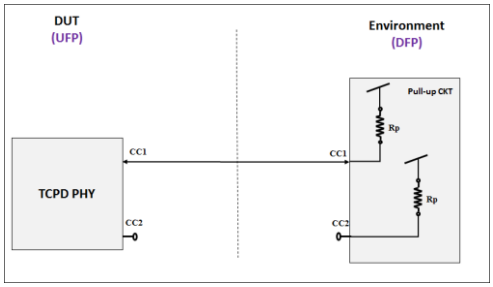

Figure 10. The valid connection - DUT as UFP

When DUT is in DFP detection mode, it monitors both CC1 and CC2 pins for proper termination by sensing the voltage lower than the unterminated voltage across CC1 and CC2 pins. In this mode DUT has the ability to detect and differentiate *Ra* and *Rd*.

When DUT is in UFP detection mode, it senses the valid VBUS voltage before the UFP detection. Once the valid VBUS voltage is detected, DUT monitors both CC1 and CC2 pins for a voltage greater than its local ground voltage.

Figure 11 shows the cable orientation detection setup. If the DUT detects valid connection between *Rp* and *Rd* at CC1 pin, it indicates "*Normal*" orientation. Similarly, if the DUT detects valid connection between *Rp* and *Rd* at CC2 pin, it indicates "*Flipped*" orientation.

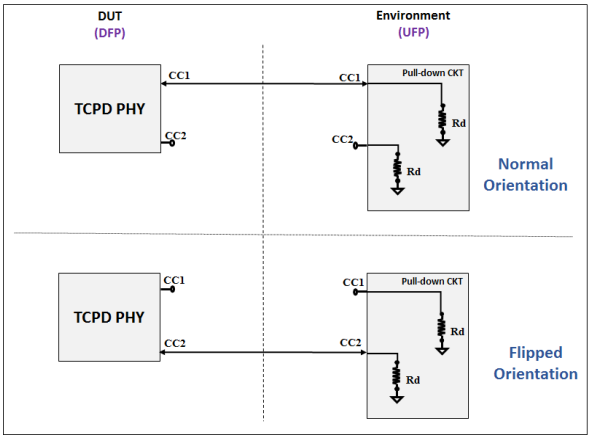

Figure 11. Cable orientation/twist detection

AMS UVC controls the *Pull-down CKT* with proper *Ra* or *Rd* resistance values. It enables all the combinations (*Ra* and *Rd*) of connections on both CC1 and CC2 pins. *RES UVC* configures the *Ra* resistance from 800Ω to 1.2kΩ and *Rd* resistance within 5.1kΩ±10%. When DFP detection is activated, DUT pulls-up both CC1 and CC2 pins to 3.3V. If *Rd* is connected to CC pin, the CC voltage drops to approximately 400mV. Similarly if *Ra* is connected to CC pin, the CC voltage drops to approximately 71mV-106mV. Figure 12 shows the sequence of the DFP detection for all combinations of connections. Table 1 shows the sequence of the DFP detection for all the combinations of connections with respect to the result shown in Figure 12.

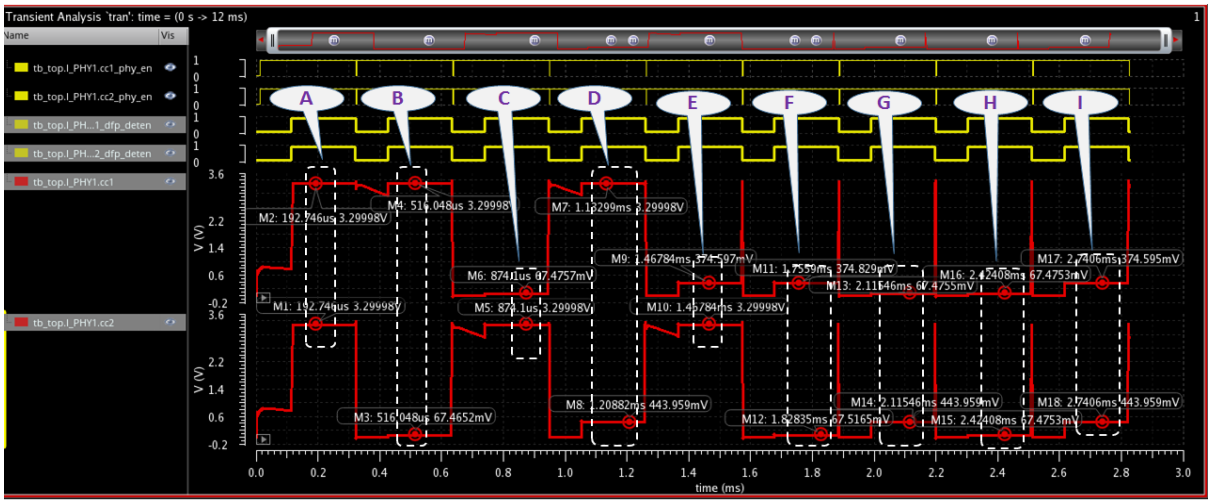

Figure 12. DFP detection operations

Table 1. The DFP detection for all combination of connections

Marker	CC1	CC2	DFP State
A	Open	Open	Nothing connected
B	Open	Ra	Powered cable/No UFP connected
C	Ra	Open	Powered cable/No UFP connected
D	Open	Rd	UFP connected
E	Rd	Open	UFP connected
F	Rd	Ra	Powered cable/UFP connected
G	Ra	Rd	Powered cable/UFP connected
H	Ra	Ra	Debug Accessory Mode connected
J	Rd	Rd	Audio Adapter Mode connected

When DUT is working as an UFP, it validates VBUS and senses both CC pins for the voltage greater than its local ground voltage. The DUT senses 400mV, 984mV and 1.17V voltages when far-end DFP advertises default USB power, 1.5A @ 5V, and 3.0A @ 5V respectively. The *AMS UVC* controls the *Pull-up CKT* with proper *Rp* values. The *RES UVC* configures the resistor ladder in *Pull-up CKT* with the resistance of 36kΩ ± 20%, 12kΩ ± 5%, and 4.7kΩ ± 5% in order to mimic the far-end DFP with the current advertisements. Figure 13 shows the result of the UFP detection operations for different conditions.

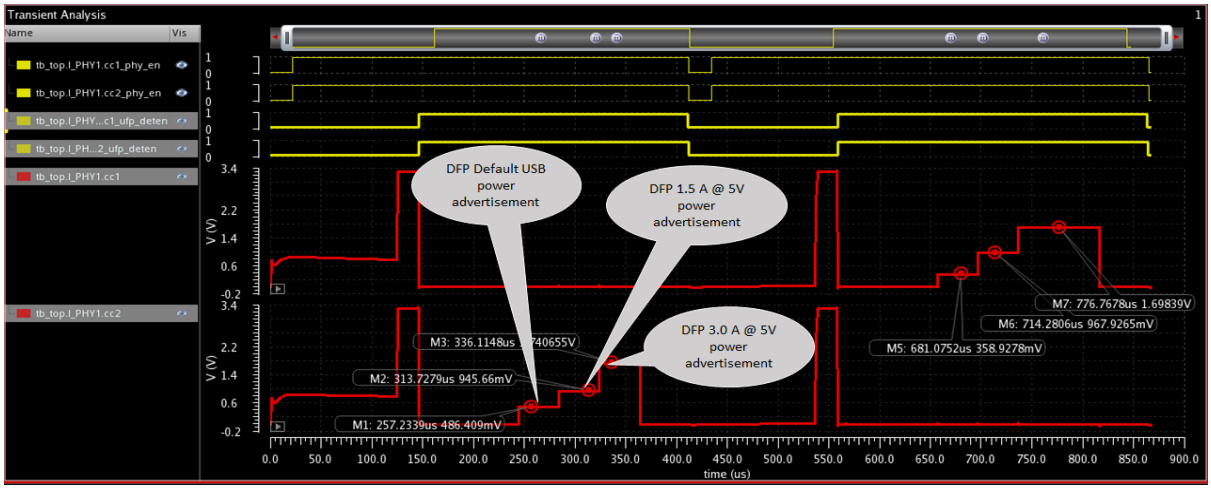

Figure 13. The UFP detection operations

b) PD communication:

The PD communication is initiated by the DFP after detecting valid DFP-to-UFP connection and cable orientation. The DUT consists of transmitter and receiver that communicate across a signal CC wire depending on the cable orientation. PD communication uses half-duplex mode and Bi-phase Mark Coding (BMC) data transfer between DFP and UFP. The *TCPD UVC* and *FarEnd UVC* generate randomized data packet and transmit across the CC wire. The *Scoreboard* checks the data integrity across the CC wire.

Figure 14 and Figure 15 show the PD communication with "*Normal*" orientation and "*Flipped*" orientation respectively.

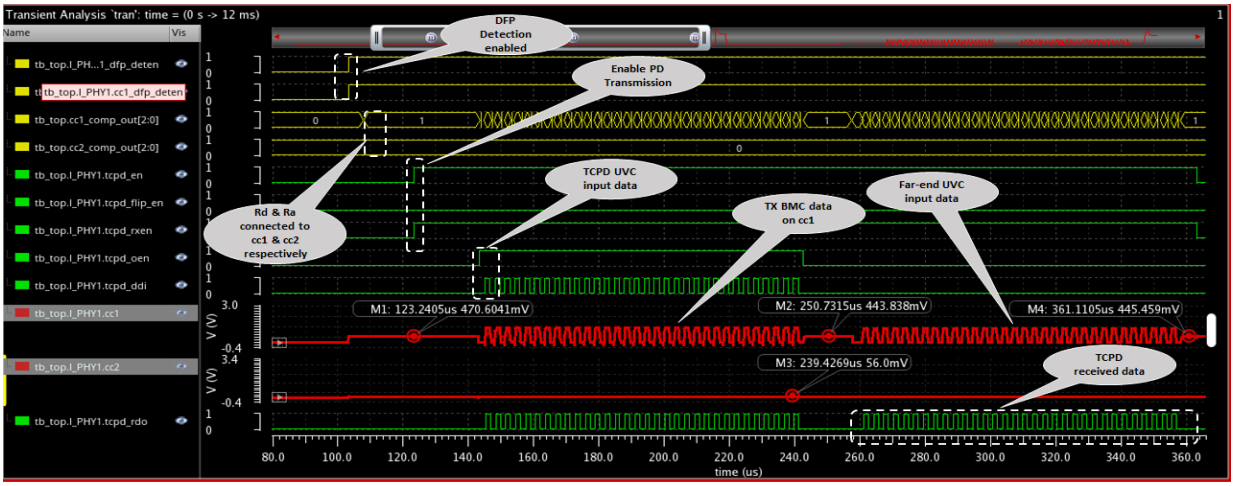

Figure 14. The PD communication with "Normal" orientation

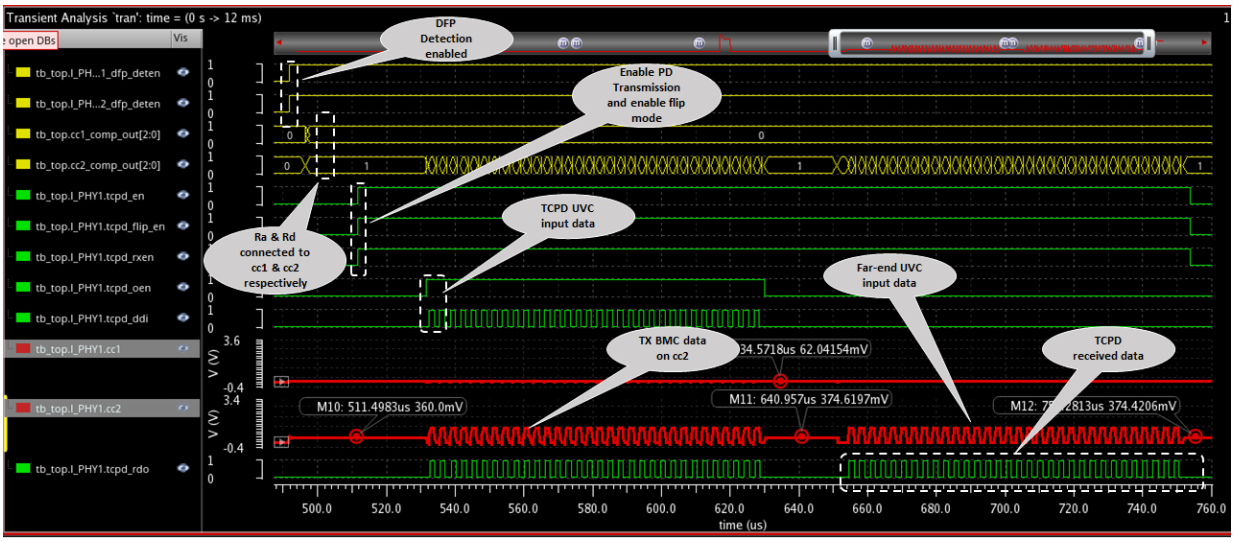

Figure 15. The PD communication with "Flipped" orientation

Functional coverage groups are added in mixed-signal verification environment for the resistor ladder configuration for *Ra*, *Rd* and *Rp*. *RES UVC* captures the resistance variation on both CC1 and CC2 pins as a functional coverage. Figure 16 shows the functional coverage status for *Ra*, *Rd* and *Rp* resistance variation.

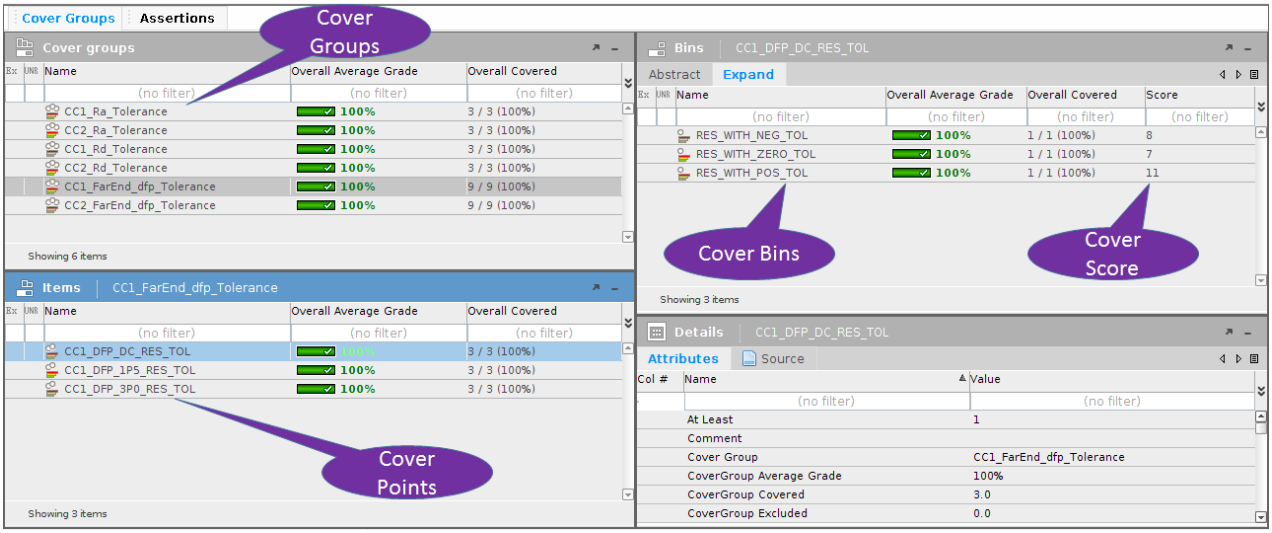

Figure 16. Functional coverage status for *Ra*, *Rd* and *Rp* variation

B. USB 2.0/3.0 PHY Verification

In USB 2.0 PHY, HS host-disconnect is detected when the differential voltage is ≥ 625mV. Figure 17 shows the host disconnect detected by HOST DUT. The *AMS UVC* configures the connector circuit such that it enables the transmission line with characteristic impedance of 45Ω, termination impedance of ~95Ω, and turnaround delay of 60ns. In this configuration, the reflected wave amplitude is reduced to provide differential amplitude of ≥ 625mV. Initial the DUT senses differential amplitude is ~466mV during the start of the (Start of frame) SOF packet. The reflection effect is seen on the line due to non-termination after 60ns. At end of the SOF, the 'hostdisconnect' signal is asserted as the DUT senses the differential amplitude is greater than 625mV at the end of the SOF packet.

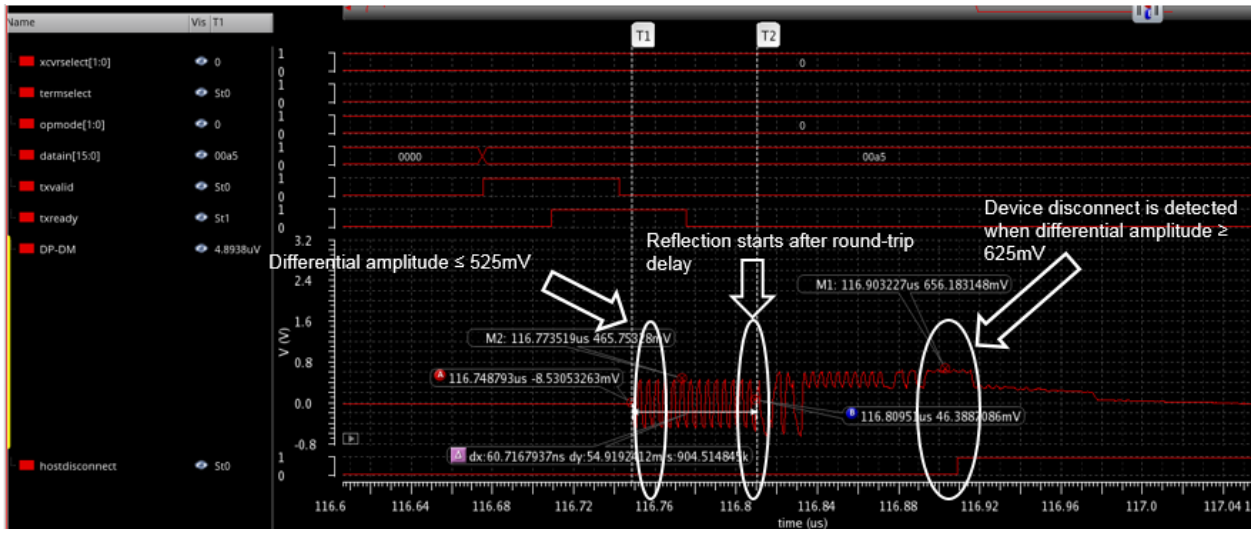

Figure 17. HS Host-Disconnect Detection, when Differential Amplitude ≥ 625mV

HS reception, followed by HS transmission, is shown in Figure 18. During HS reception, *Serial UVC* drives data through *UCM*. *UCM* adds channel attenuation to data before driving the DUT. During HS transmission, the analog output from DUT is digitized by *UCM* before feeding to the scoreboard.

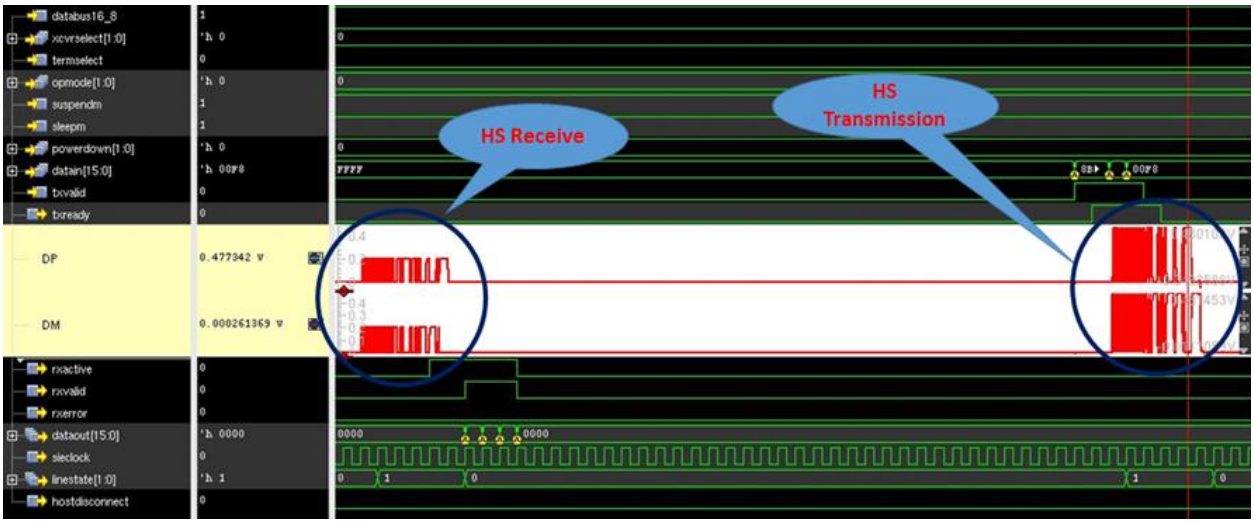

Figure 18. HS Reception and HS Transmission

Functional coverage groups are added in mixed-signal verification environment for the termination impedance during HS hostdisconnect detection mechanism. *AMS UVC* captures the impedance variation Zterm as a functional coverage. Figure 19 shows the functional coverage status for differential voltage variation from 450mv to 900mv during HS hostdisconnect detection mechanism.

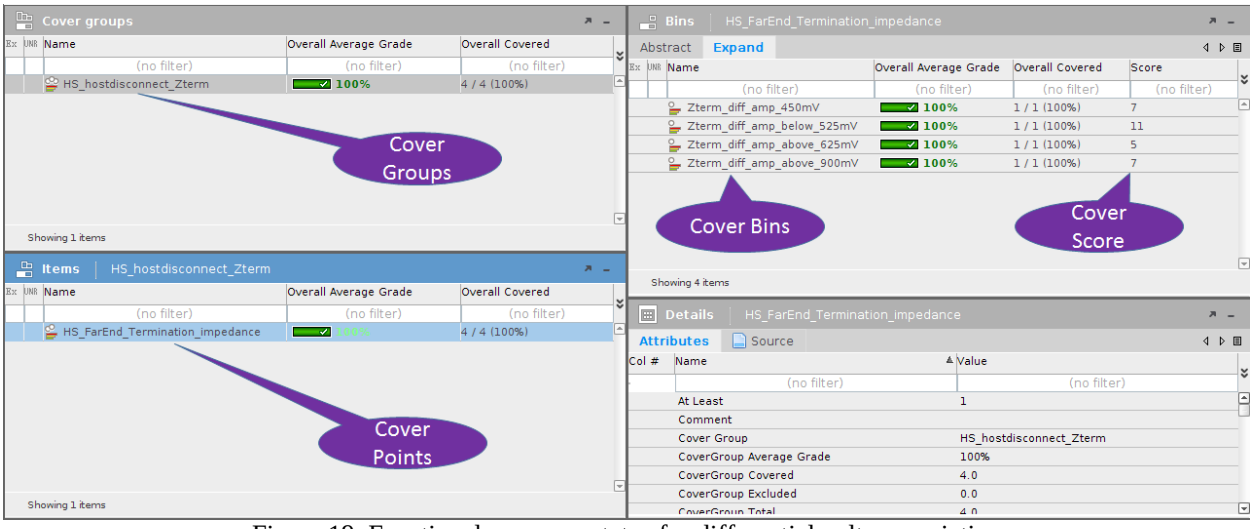

Figure 19. Functional coverage status for differential voltage variation

Figure 20 shows the receiver detection mechanism of USB 3.0 PHY. In this test, far-end receiver connection/dis-connection is mimicked. This mechanism of connection/dis-connection of far-end receiver is enabled by *AMS UVC*.

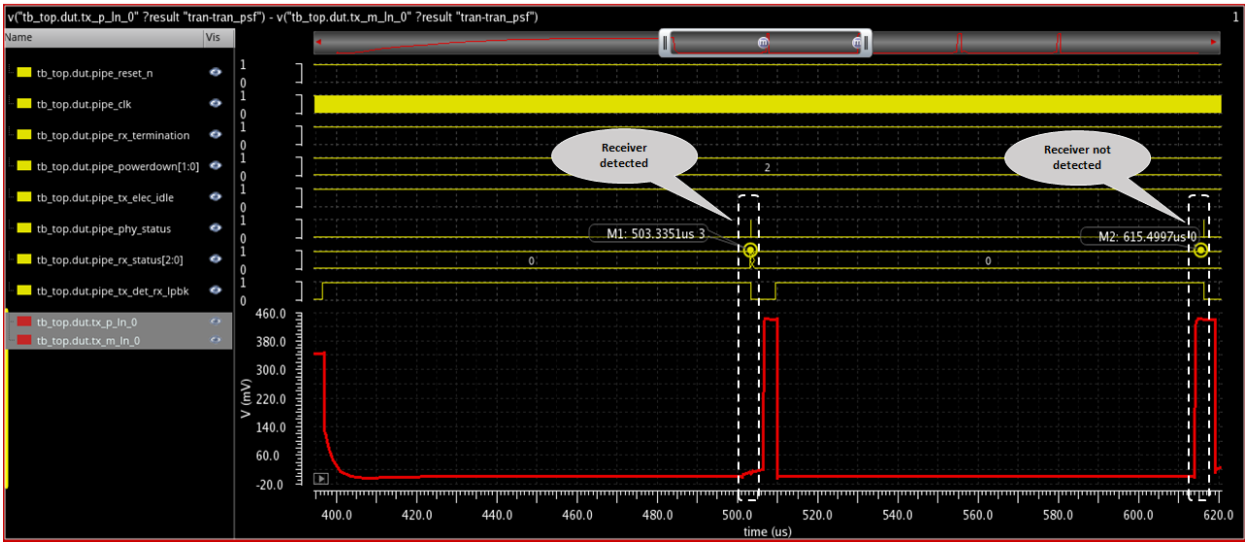

Figure 20. The receiver detection for both “receiver is present” case and “receiver is absent” case

Figure 21 shows the PIPE data transmission with 3.5dB de-emphasis. The *PIPE UVC* generates the parallel random data and drives to the USB 3.0 PHY. The DUT serializes the parallel data and feeds to *UCM* via *Connector Circuit*. The *UCM* converts electrical to logic depending on the Margin/Swing/De-emphasis. The *Scoreboard* and *Monitor* verify the data integrity and protocol checks.

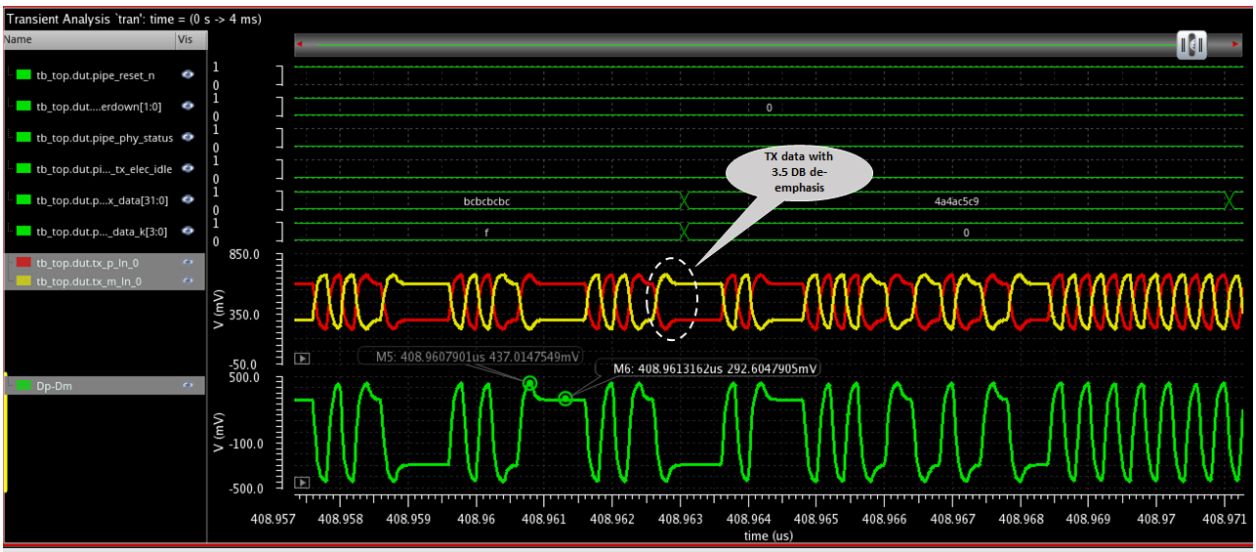

Figure 21. The PIPE data transmission with 3.5 dB de-emphasis

Figure 22 shows the functional coverage for the capacitor ladder configuration used for coupling capacitance. *CAP UVC* captures the capacitance variation during the receiver detection as a functional coverage.

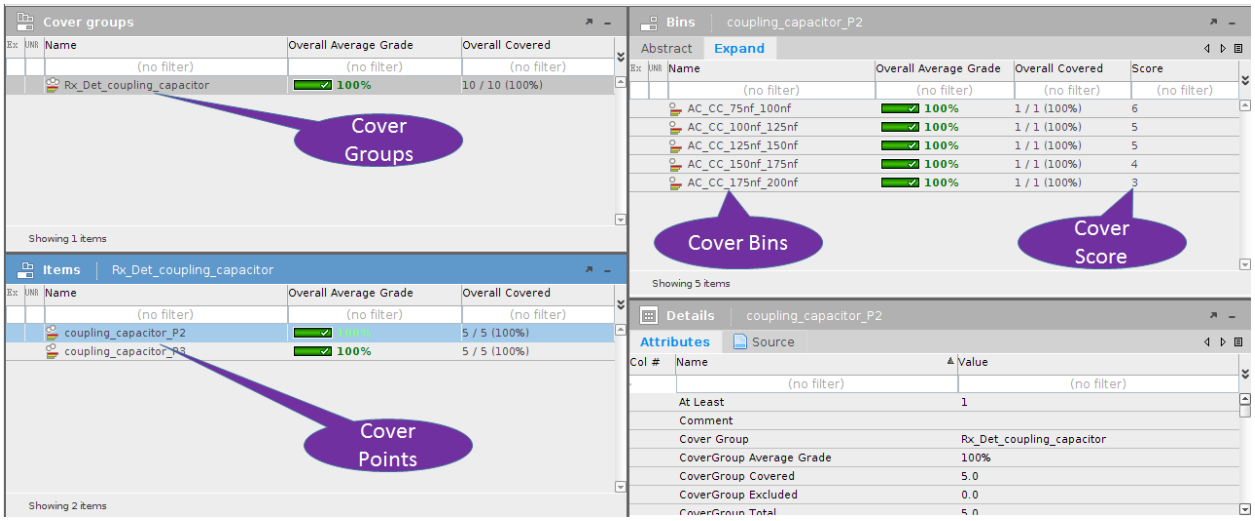

Figure 22. Functional coverage status for capacitance variation

Table 2 shows the simulation runtime with respect to multiple DUT configurations for verification of Type-C USB PHY.

Table 2. The simulation runtime with respect to DUT configurations

Operation modes	DUT configurations (simulation time in minutes)			
	RTL + High Level Behavioral Model	RTL + Detailed Behavioral Model	RTL + Real value model	RTL + SPICE
DFP detection	2	-	-	7
UFP detection	2	-	-	7
PD Communication	3	-	-	9
USB 2.0 Host Disconnection	3	5	-	30
USB 2.0 HS data transfer	3	7	-	90
USB 2.0 FS data transfer	2	5	-	15
USB 2.0 LS data transfer	2	5	-	15
USB 3.0 RX detection	5	8	15	30
USB 3.0 TX data transfer	5	8	15	90
USB 3.0 RX data transfer	5	10	60	480

IV. Summary and Conclusion

The UVM-based HVL verification environment of the Type-C USB PHY used for digital verification has been effectively reused for the mixed-signal verification. The scoreboard and protocol checkers are enabled in mixed-signal verification. Additional tests and functional coverage were added to the existing digital environment for robust verification of the Type-C USB PHY. The overall functional coverage is improved by merging digital regression data with mixed-signal regression data. Thus, this mixed-signal verification methodology improves the verification quality and confidence in the design.

Acknowledgment

We would like to thank Parag Lonkar, Sumanth Chakkirala, Raju Pudota, and Digital/AMS verification team members for their input and valuable feedback during the implementation.

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